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CMOS-SOI-MEMS Uncooled Infrared Security Sensor With Integrated Readout

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ABSTRACT A new generation of uncooled passive infrared (PIR) security sensors based on a suspended thermal transistor MOS (TMOS), fabricated in standard CMOS-SOI process, released by post-etching, and wafer level packaged achieving a vacuum of <4 Pa, has been developed at the Technion. One of the important features of TMOS is very low power consumption (in this case, ∼2–4 nWatt) due to its subthreshold operation requiring ∼10 nA at 0.2 V, enabling wide range of battery applications. This paper focuses on the analog design of monolithically integrated readout for the electronic system, formed by the PIR sensor, its front-end analog interface and the processing circuitry. The measured signal-to-noise ratio of this system is 100–200, depending on the operation point, at the black-body temperature of 50° C, while the total input referred noise is ≤1 μVrms and the total system current consumption is no more than 20 μA. The sensors and read-out are processed with the same CMOS-SOI technology.

INDEX TERMS Infrared detectors, thermal sensors, integrated circuits, sensor arrays, semiconductor devices.

I. INTRODUCTION: CMOS-SOI-NEMS TRANSISTORS FOR UNCOOLED PASSIVE IR SENSORS

A new generation of low-cost uncooled passive thermal sensors based on a suspended transistor fabricated in standard CMOS-SOI process and released by dry etching, has been developed at the Technion [1]–[4] . It is currently under development for commercial exploitation [5]. The uncooled IR sensing is based on a floating in vacuum thermal transistor MOS (TMOS), which is thermally isolated by nanomachining, converting small temperature changes to electrical signal via the transistor I-V characteristics. The silicon-based technology is implemented in CMOS-SOI technology and Wafer Level Processing in standard CMOS Fab [6]. Furthermore, the silicon technology at a standard CMOS FAB enables Smart Wafer Level Packaging (WLP) (with vacuum, integrated optical window and filters and Wafer Level Optics) at a considerable and exceptional cost reduction.

The CMOS-SOI-NEMS technology enables monolithic integration of the readout (ROIC) with the TMOS on the same wafer. Using the transistor as an active sensing element has advantages in terms of internal gain, multiplexing within the sensor and high temperature sensitivity. Since the TMOS may be operated in subthreshold, consuming very low power, it may be powered by a battery, enabling wide range of applications related to mobile phones, smart homes, Internet of Things (IOT) and additional security applications. This low power feature of the TMOS is a great advantage in comparison to the passive bolometers, which currently dominate the market [7], [8].

II. THE TMOS INTRUDER SENSOR (OVERALL ARCHITECTURE)

The intruder sensor is a very common consumer electronic device usually found in commercial security systems and other applications where motion detection is required. The detection is performed by differentiating the signals from two sensors, where the field-of-view (FOV), the detecting area, is divided into two areas – so each sensor is exposed to half of the scenery. When an object is crossing the FOV, it is emitting thermal radiation that is converted by the sensors

into electrical signals that are then processed by the electrical circuit to produce a response to that change (Fig. 1).

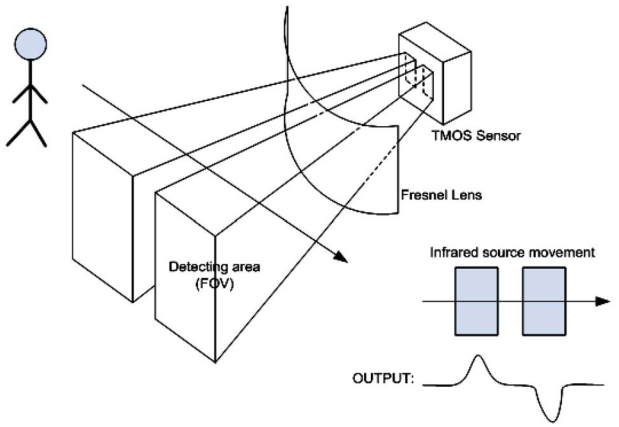


FIGURE 1. **Intruder sensor principle of operation [9].**

In order to obtain large FOV sensing area, sensor size has to be in the range of 1 millimeter square. When utilizing the TMOS pixel as the sensing element, the size of the pixel has significant impact on the thermal time constant of the pixel. Assuming a step function behavior of the incoming radiation, the pixel temperature change is given by:

$$\Delta T\,(t) = \frac{\varepsilon_s P_R}{G_{th}}\left[1 - \exp\left(-\frac{t}{\tau_{th}}\right)\right]$$
$$\tau_{th} = \frac{C_{th}}{G_{th}} \tag{1}$$

where ε_s is the effective emissivity of the TMOS, P_R [W] is the incident radiation power, G_{th} [W/K] is the thermal conductance (heat loss), C_{th} [Joul/K] is the heat capacity of the TMOS suspended element (stage) and ΔT is he temperature rise above the ambient temperature.

A typical intruder movement is estimated to be no faster than 1/5 of a second. Requiring that the pixel settles to 90% of its final temperature value within this time, sets the value of the thermal time constant (τ_{th}) required from the sensors to be

$$\tau_{th} = \frac{C_{th}}{G_{th}} < 86m\,\text{sec} \tag{2}$$

In order to meet the above thermal time constant requirement in Eq.(2), an array of thermally isolated but electrically shorted TMOS sub-pixels is used to construct each sensor (Fig. 2). This configuration allows maintaining a sensor thermal time constant that is equivalent to that of a single sub-pixel.

The arrays are constructed from densely aligned N - TMOS sub-pixels organized in rows and columns to fill the required area of each sensor. Readout may be based either on current or voltage mode approaches.

III. ELECTRICAL ANALYSIS OF THE TMOS ARRAY

Fig. 3 depicts the electrical connection of TMOS sub-pixels operating in voltage-mode readout architecture.

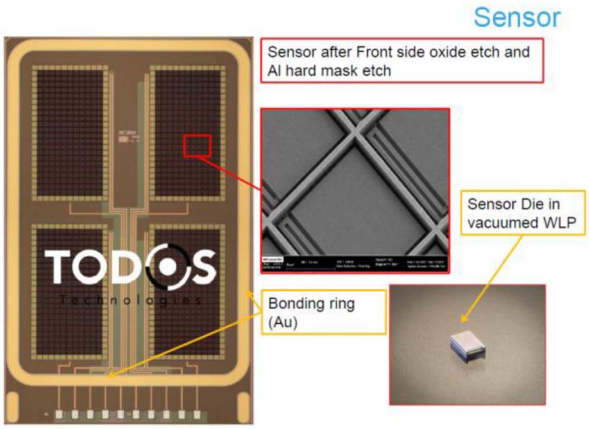


FIGURE 2. **TMOS array sensor test chip on the left, depicting also a microscope photo of a post-processed pixel and the final package after WLP.**

Each TMOS is designed in a diode-like connection to reduce the output impedance of the array. A current source is biasing the pixels and a single voltage output is sent to the readout circuit.

In order to calculate the output signal, we model each transistor as shown in Fig. 4, where "i_{sig}" represents the change in the channel current due to the device temperature change $(\Delta T)_{pixel}$ caused by the incoming thermal signal absorption.

We can approximate the expression for "i_{sig}" by calculating the derivative of the channel current I_{ds} over the temperature:

$$i_{sig} \approx \frac{dI_{DS}\,(T)}{dT} \cdot (\Delta T)_{pixel} \tag{3}$$

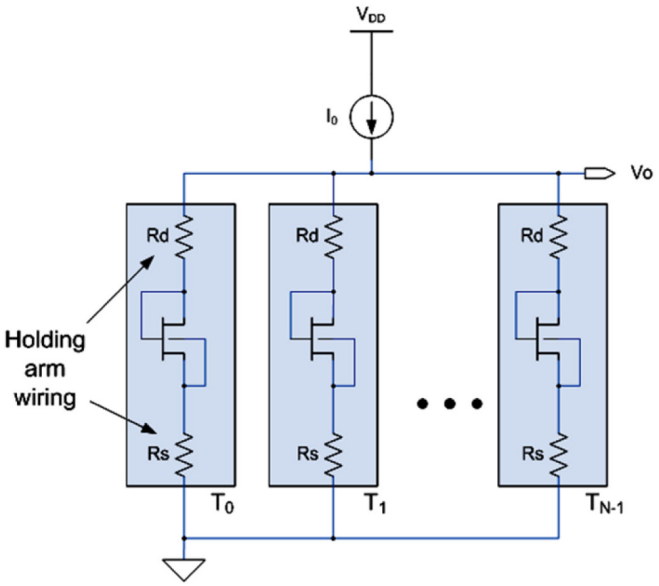


FIGURE 3. **TMOS array electrical model – voltage mode readout.**

We examine the transistor in two operating regions – saturation and subthreshold [10].

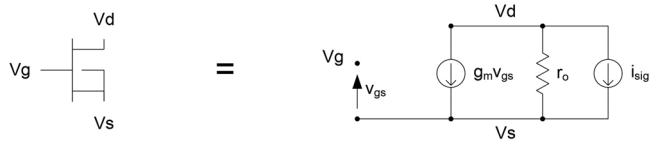


FIGURE 4. **TMOS device small signal model.**

Saturation long channel current is given by:

$$I_{DS}(T) = \frac{C_{ox}\mu(T)}{2}\frac{W}{L}(V_{GS} - V_T(T))^2 \tag{4}$$

and subthreshold channel current (for V_{DS}=V_{GS}>3kT/q):

$$I_{DS}(T) = \mu(T)\, C_{ox}\frac{W}{L}\left(\frac{kT}{q}\right)^2 (n-1)\, e^{\frac{q}{nkT}(V_{GS}-V_T(T))} \tag{5}$$

The inversion layer effective mobility depends on temperature according to [10]:

$$\mu_{eff} = \mu_0\left(\frac{T_0}{T}\right)^b \tag{6}$$

where coefficient "b" is typically close to 2 at room temperature.

For a TMOS operating in saturation region we get:

$$\left.\frac{dI_{DS}(T)}{dT}\right|_{SAT} = -2I_{DS}\left[\frac{1}{T} + \frac{1}{V_{GS}-V_T}\frac{dV_T}{dT}\right] \tag{7}$$

For a TMOS operating in subthreshold region we get:

$$\left.\frac{dI_{DS}(T)}{dT}\right|_{Sub-Vt} = -I_{DS}\frac{q}{nkT}\left[\frac{(V_{GS}-V_T)}{T} + \frac{dV_t}{dT}\right] \tag{8}$$

Summing all sub-pixels contributions in the array to the output signal by means of Norton-Thevenin conversion, we get:

$$v_o = N\cdot \underbrace{\frac{-\frac{i_{sig}}{g_m}}{R_D + \frac{1}{g_m} + R_S}}_{\substack{\text{Single pixel output}\\ \text{signal current}}} \cdot \underbrace{\frac{R_D + \frac{1}{g_m} + R_S}{N}}_{\text{Array output impedance}} = -\frac{i_{sig}}{g_m} \tag{9}$$

The output signal of the array is the same as that of a single sub-pixel. The expression for the transconductance g_m is given by:

$$g_m = \frac{dI_{DS}}{dV_{GS}} = \begin{cases} \dfrac{2I_{DS}}{V_{GS}-V_T}, & \text{Saturation} \\ \dfrac{q}{nkT}I_{DS}, & \text{Subthreshold} \end{cases} \tag{10}$$

Therefore the output signal is:

$$v_o = \begin{cases} \left(\dfrac{V_{GS}-V_T}{T} + \dfrac{dV_T}{dT}\right)\cdot(\Delta T)_{pixel}, & \text{Saturation} \\ \left(\dfrac{V_{GS}-V_T}{T} + \dfrac{dV_T}{dT}\right)\cdot(\Delta T)_{pixel}, & \text{Subthreshold} \end{cases}$$
$$= \left(\frac{V_{OV}}{T} + \frac{dV_T}{dT}\right)\cdot(\Delta T)_{pixel} \tag{11}$$

In the CMOS-SOI process under study [6] dV_T/dT is measured to be -1mV/°C. The signal expression is the same for both operating regions, making the overdrive level V_{OV} of the transistor the only control to obtain the required signal level at the output.

The noise at the output is the sum of all the noise sources in the circuit since there is no correlation between them. The noise from each of the holding arm conductors is thermal noise, and the noise from TMOS transistor comprises thermal (shot in subthreshold) and flicker noises.

$$\overline{v_{o,n}^2} = N\cdot \underbrace{\frac{\frac{\overline{i_{n,1/f}^2}+\overline{i_{n,S}^2}}{g_m^2} + 4kT(R_s+R_d)}{\left(R_D + \frac{1}{g_m} + R_S\right)^2}}_{\substack{\text{Single pixel output}\\ \text{noise current}}} \cdot \underbrace{\frac{\left(R_D + \frac{1}{g_m} + R_S\right)^2}{N^2}}_{\text{Array output impedance}}$$
$$= \frac{\frac{\overline{i_{n,1/f}^2}+\overline{i_{n,S}^2}}{g_m^2} + 4kT(R_s+R_d)}{N} \tag{12}$$

The signal-to-noise ratio is an important merit because the sensor's SNR is setting the minimum SNR of the entire system. Using known expressions for the flicker and thermal noises [10], [11] we get:

$$SNR \equiv \frac{\left(\frac{v_o}{\Delta T_{pixel}}\right)^2}{\int_{f_1}^{f_2}\overline{v_{o,n}^2}df}$$
$$= \begin{cases} \dfrac{N\cdot\left(\frac{V_{OV}}{T}+\frac{dV_T}{dT}\right)^2}{4kT\left(R_D+R_S+\frac{V_{OV}}{3I_{ds}}\right)(f_2-f_1)+\frac{K_{f,sat}}{C_{OX}WL}\ln\left(\frac{f_2}{f_1}\right)}, & \text{Saturation} \\ \dfrac{N\cdot\left(\frac{V_{OV}}{T}+\frac{dV_T}{dT}\right)^2}{4kT\left(R_D+R_S+\frac{2(kTn)^2}{qI_{ds}}\right)(f_2-f_1)+\frac{K_{f,sub}}{C_{OX}WL}\left(\frac{f_2}{f_1}\right)}, & \text{Subthreshold} \end{cases} \tag{13}$$

where $K_{f,sat}$=q^2N_{ot}/C_{ox}, $K_{f,sub}$=$(C_{inv}/(C_{OX}+C_d))^2q^2N_{ot}/C_{ox}$ are noise coefficients for saturation and subthreshold regions, correspondingly [11], f_1 and f_2 define the frequency band of interest, which is 0.5Hz and 5Hz, correspondingly, for the intruder sensor.

Maximizing SNR by reducing the noise and/or increasing the signal level is key in achieving a sensitive system that detects very small temperature fluctuations at the target. Fig. 5 depicts the array SNR based on typical device and parameter values, supposing ΔT_{pixel}=1K.

At low bias currents, SNR in the deep subthreshold region is higher than in saturation. Increasing the bias current increases SNR in both operating regions, however after 100nA, the improvement in SNR is negligible.

There is one bias point, at saturation, known as Zero Temperature Coefficient (ZTC) where the pixel is "blind" to the incoming radiation ($dv_o/dT = 0$) and is not producing an output signal.

IV. READOUT DESIGN

The readout is processing a subtraction of the voltage signals coming from the two TMOS arrays, and is therefore insensitive to any common mode signals such as the biasing

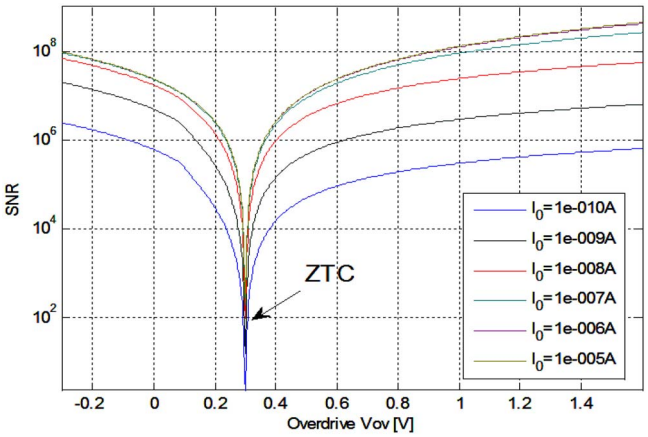


FIGURE 5. **TMOS sensor SNR as a function of overdrive level and the bias current. Zero-Temperature-Coefficient (ZTC) operating point is marked at V_{OV}≈300mV.**

level which is impacted by the process variation, sensor temperature, supply level, etc.

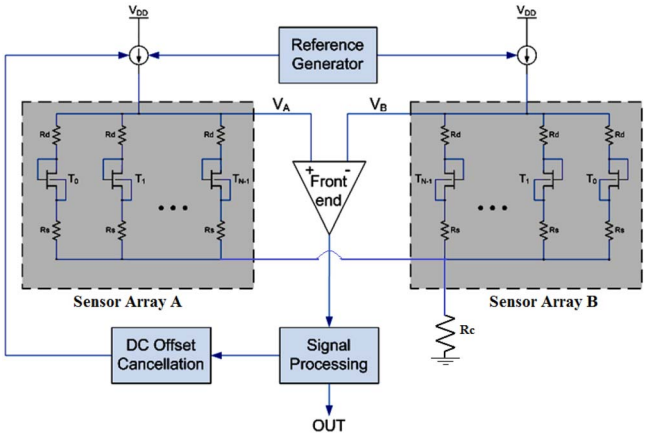


FIGURE 6. **Intruder sensor system.**

The first stage of the readout (Fig. 6) is a low-noise front end differential amplifier which conditions the weak signal coming from the TMOS arrays. Two sensor arrays are connected to inputs "A" and "B", where R_C is common mode resistor. A signal processing unit is then filtering the signal within the frequency band of interest to reduce noise and increase sensitivity. Since the signals coming from the sensors are very weak (microvolt level), the readout has very high gain, and in order to prevent the system from saturating due to mismatch between the sensors or DC offset in the front end amplifiers a DC Offset Calibration block is used. The calibration block is creating a very high gain analog feedback loop from the output of the front-end to the bias currents of the sensors, adding the required small DC current (tens of nano-amps) needed to bring the front-end output to mid-supply level. Calibration is performed once at power up and also within constant time intervals as needed.

A. FRONT-END AMPLIFIER

The front-end stage is implemented as an instrumentation amplifier that has very high input impedance and high common-mode rejection (CMRR).

The first stage of the instrumentation amplifier (Fig. 7) includes two single ended low noise amplifiers (LNA) with moderate closed-loop gain. The connection of the feedback resistors with R2 eliminates the need for a reference source to bias the negative input of each LNA, setting the common mode at the (-) inputs of both LNAs to be almost the same as the common mode of the inputs.

The LNA's first stage (Fig. 8) is setting the noise level of the OpAmp and therefore designed to produce very little noise while still having moderate level of gain. Second stage is providing most of the gain of the OpAmp. Stage-3 is a low current buffer for driving the resistive loads of the LNA. This design consumes less than 5μA, and has an input referred noise level of 0.8μVrms (0.5-5Hz).

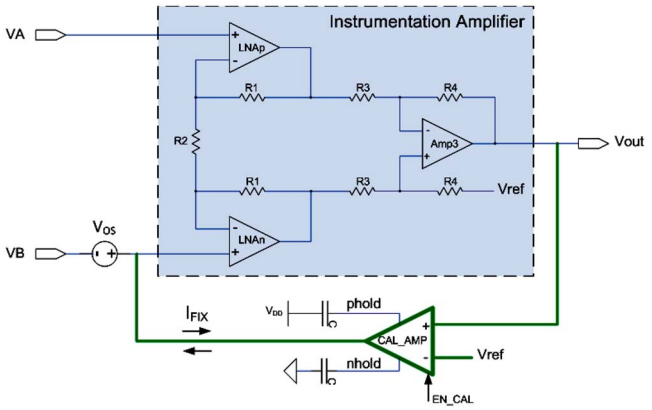


FIGURE 7. **Front-end readout instrumentation amplifier with the calibration loop.**

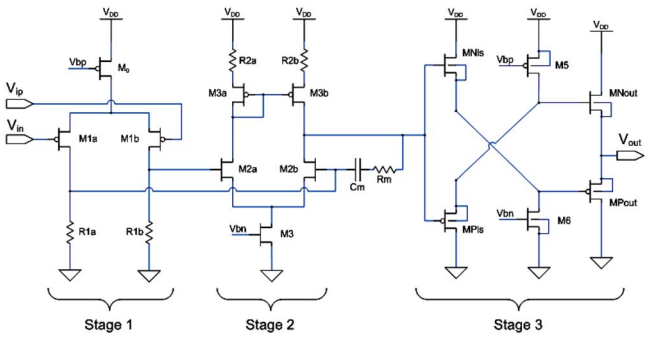


FIGURE 8. **Front-end readout LNA circuit.**

"Amp3", the subtracting stage of the instrumentation amplifier, has to further amplify the signal to meet the minimum level requirement of the post-processing circuit of 1LSB≈1mV. Assuming that the input noise level is ∼1μVrms, the front-end amplifier has a total gain of 1000.

"Amp3" OpAmp (Fig. 9) can produce high output swings to enable high dynamic range of the system. It is small and consumes about 1μA, since it has no stringent noise or accuracy requirements.

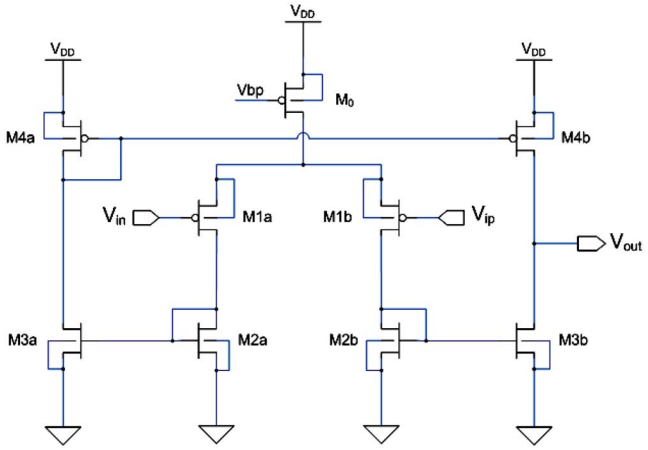


FIGURE 9. Front-end readout "Amp3" circuit.

B. CALIBRATION AMPLIFIER

Using statistical models provided by the FAB [6], a random variation simulation (Monte-Carlo) of the sensors and the readout was performed showing standard deviation of 214μV and 391mV at the readout input (V_A-V_B) and output respectively. In order to obtain high dynamic range, the offset should be corrected to about the noise level of the system, ~1μV at the input. To perform this, a high gain calibration loop is enabled (Fig. 7, marked in bold green line), producing the small current (I_{FIX}) needed to bring the output of the readout to the level of voltage *Vref*. After calibration, external caps connected to *nhold* and *phold* nodes maintain the calibration information for long time (depending on cap size and system leakages).

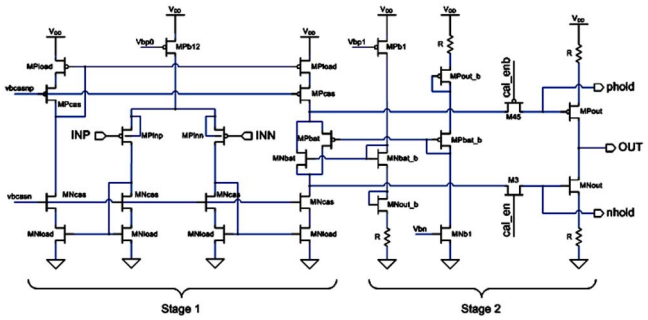


FIGURE 10. Calibration amplifier circuit.

The first stage of the calibration amplifier (Fig. 10) is a high gain, low offset current mirror OTA. The second stage is a low-noise, high output impedance class-AB OTA. Switches are added to disconnect the output branch from the rest of the circuit when calibration is finished, to "lock" the calibration value using the external caps. The entire loop has a gain of above 100dB (no load) and phase margin of 51.8°, with the dominant pole set by the output capacitors. The output noise level is 69μVrms (0.5-5Hz), which allows reaching the desired calibration accuracy set by the 1mVrms noise.

V. CHARACTERIZATION AND MEASUREMENTS

A. SENSOR TEST-CHIP CHARACTERIZATION

I-V curve presented in Fig. 11 and thermal time constant measurements show good matching to simulations and analytical calculations for array of 180 sub-pixels "B3", where the transistor dimensions within each sub-pixel are W/L=4.9μm/190μm. Array thermal time constant was measured from 85msec to 95msec, which is close to the calculated 88msec.

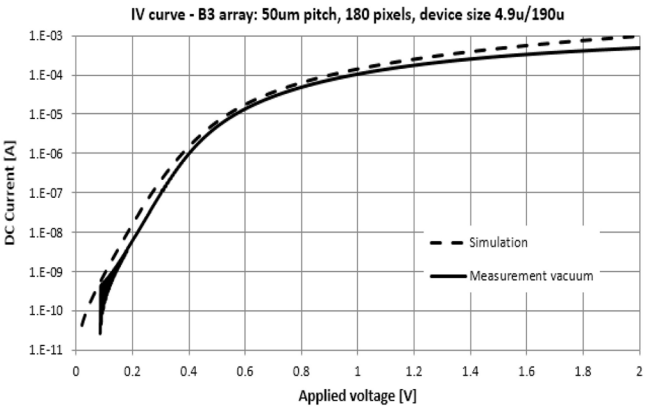


FIGURE 11. Sensors array (B3) I-V measurements in vacuum.

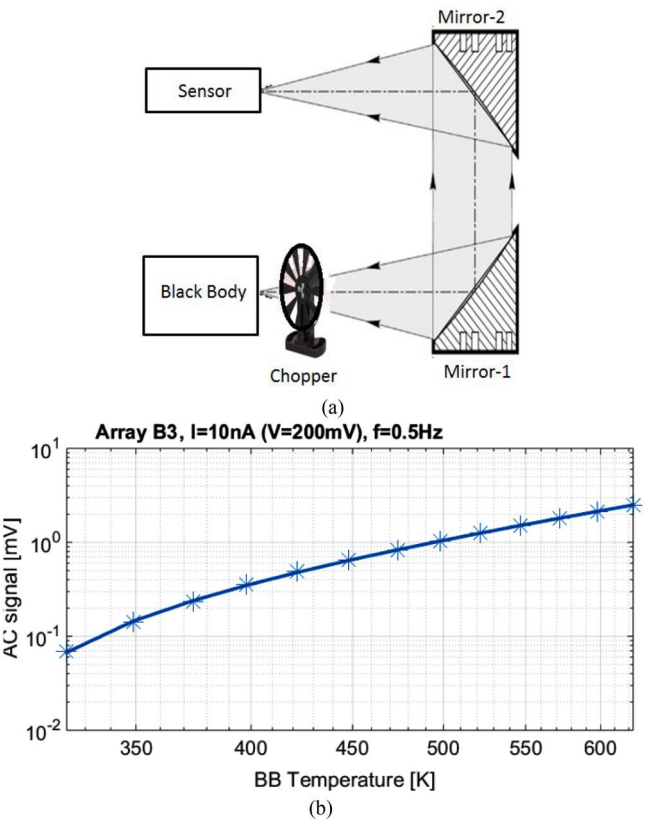


FIGURE 12. Optical characterization of the array: (a) measurement setup, (b) measured output current signal vs. BB temperature, while the temperature of 323K corresponds to the signal of ~0.06mV.

Sensor optical characterization has been performed by means of the setup exhibited in Fig. 12(a), consisting of

Black Body (BB), two mirrors and chopper. The optics is based on two gold parabolic mirrors with F#=1.66. The BB radiation, modulated by the chopper causes the sensor alternating current, has been measured by lock-in amplifier in Volt-rms units. The sensor response is shown in Fig. 12(b) as a function of BB temperature, exhibiting AC signal of ∼0.06mV at the temperature of 323K (50°C). The measurement has been performed at the chopper frequency of 0.5Hz, corresponding to the application (intruder sensor) requirements, and DC voltage applied to the sensors of 200mV.

Fig. 13 exhibits result of noise characterization of the sensor array given in units of variance measured within the frequency interval of 0.5-5 Hz, while Fig. 14 presents measured Signal-to-Noise Ratio (SNR) as a function of operation point for the same array. One can see that that the maximum SNR (∼100-200) corresponds to the applied voltages of ∼200-450mV.

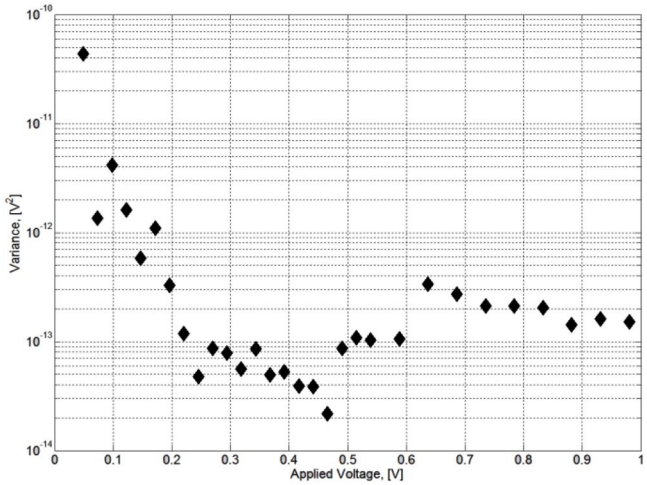


FIGURE 13. Noise variance contributed by the sensors array (B3), measured within the frequency interval of 0.5-5 Hz, vs. the applied voltage.

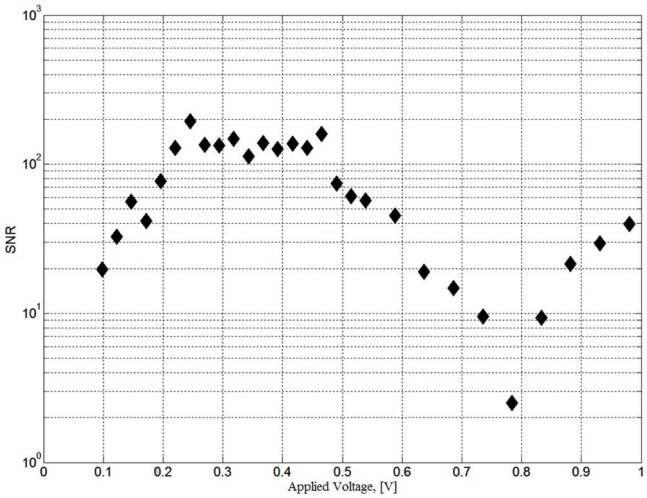


FIGURE 14. SNR vs. the voltage applied to the array (B3) measured at BB temperature of 50°C.

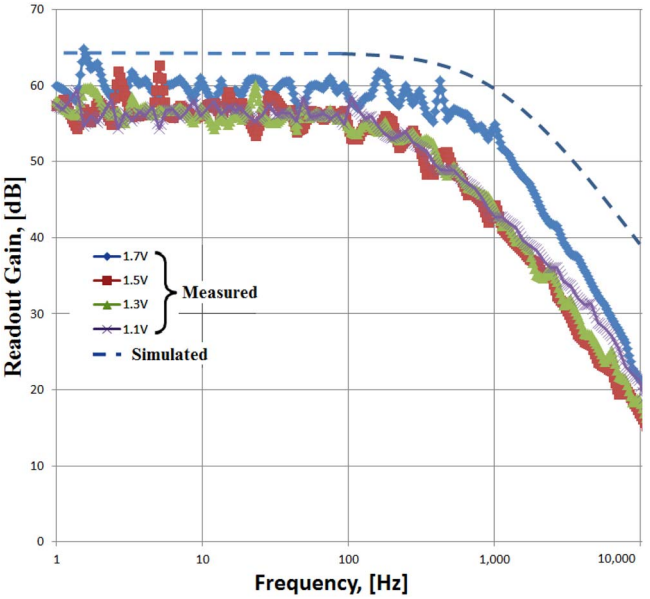


FIGURE 15. Readout circuit gain vs. frequency showing slightly attenuated measurement compared to simulation (∼4dB lower).

B. READOUT CIRCUIT CHARACTERIZATION

The readout circuit includes the amplifiers (Fig. 7) and reference circuits (bandgap, current source to bias the sensors etc.). Fig. 15 exhibits both measured and simulated readout circuit gain as a function of frequency for the several DC input voltages, showing good matching (up to ∼4dB difference) between the measured and simulated results. Fig. 16 shows comparison between the simulated and measured output noise PSD, resulting in input referred noise of ∼0.8μVrms. It should be noted that there is good fitting between the measured and simulated noise. In addition, one can see from comparison of Figs. 13, 16 that the noise contributed by the readout circuit is the dominant one for any voltage higher than 0.2V applied to the sensors (B3).

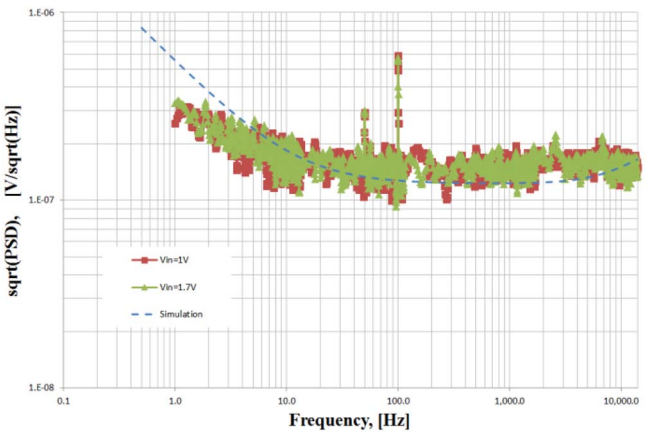


FIGURE 16. Square root of input referred noise PSD of the readout circuit vs. frequency: both measured and simulated.

C. INTRUDER SENSOR SYSTEM TESTING

Using the above-mentioned data about the sensor array response (∼0.06mV) to BB radiation modulated by chopper, when BB temperature is 50°C, and readout circuit *total* input referred noise (∼1μVrms), we can obtain SNR for the whole intruder sensor system detailed in Fig. 6 system: ∼60. This value is in good correlation with Fig. 14.

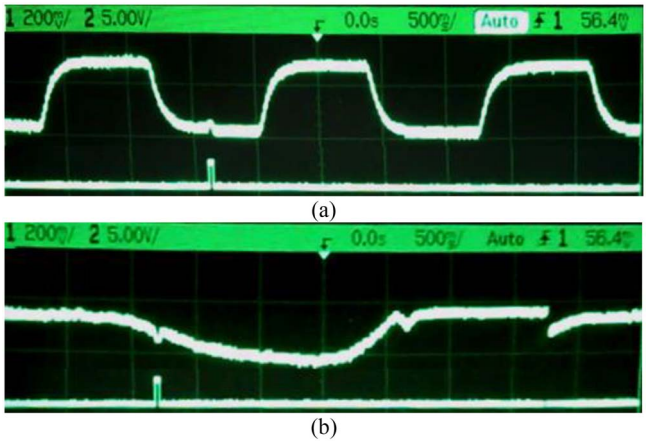


FIGURE 17. Response of the intruder sensor system to: (a) BB radiation (BB temperature of 50°C) modulated by chopper, (b) hand motion.

Fig. 17 exhibits the time response of the intruder sensor system to BB radiation modulated by chopper (Fig. 15(a)) and to hand motion (Fig. 15(b)), while BB temperature was 50°C. Measurements have been performed at room temperature 20°C.

The upper line in Fig. 15(a) presents the output voltage vs. time, while the bottom line corresponds to the calibration pulse. The output peak-to-peak voltage is ≈300mV, corresponding to input referred signal of ≈100μVrms (while gain was 1000), which is in good agreement with Fig. 12.

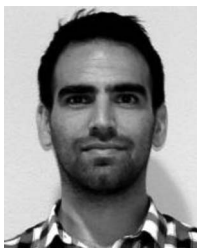
Fig. 15(b) presents the same in case of hand motion. The output peak-to-peak voltage is ≈180mV, corresponding to input referred signal of ≈60μVrms (while gain was 1000). Taking into account that hand temperature is less than 50°C, the results are consistent.

VI. CONCLUSION

A new generation of low-cost uncooled passive thermal sensors (dubbed TMOS) based on a suspended transistor fabricated in standard CMOS-SOI process and released by dry etching has been developed and is currently under production [1]–[6]. In this work we demonstrate a design of monolithically integrated IR sensor system formed by the TMOS sensor and the electronic readout circuitry. This level of integration enables significant cost reduction, reduced power consumption and highly adaptable configurations using the TMOS sensor, even beyond the intruder sensor application.

REFERENCES

[1] L. Gitelman *et al.*, "CMOS-SOI-MEMS transistor for uncooled IR imaging," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 1935–1942, Sep. 2009.
[2] A. Svetlitza, I. Brouk, S. Stolyarova, and Y. Nemirovsky, "Nanometric CMOS-SOI-NEMS transistor for uncooled THz sensing," *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1575–1583, May 2013.
[3] A. Zviagintsev, I. Brouk, I. Bloom, and Y. Nemirovsky, "Voltage and current integrated readout for uncooled passive IR sensors based on CMOS-SOI-NEMS technology," presented at the IEEE 28th Conv. Elect. Electron. Eng. Israel, Eilat, Israel, Dec. 2014, pp. 1–5.
[4] A. Zviagintsev, I. Brouk, I. Bloom, and Y. Nemirovsky, "Self-heating effects in CMOS-SOI-NEMS transistors for uncooled passive IR sensors," in *Proc. IEEE Int. Conf. Microwaves Commun. Antennas Electron. Syst. (COMCAS)*, Tel Aviv, Israel, Oct. 2015, pp. 1–5.
[5] Company, "Todos Technologies Ltd.," Kinneret st.12, Airport City, Israel.
[6] Company. *STMicroelectronics*. [Online]. Available: http://www.st.com
[7] R. A. Wood, "Monolithic silicon microbolometer arrays," in *Uncooled IR Imaging Arrays and Systems* (Semiconductors and Semimetals), vol. 47, P. Kruse and D. Skatrud, Eds. New York, NY, USA: Academic Press, 1997.
[8] U. Mizrahi *et al.*, "Large-format 17μm high-end VO_x μ-bolometer infrared detector," in *Proc. SPIE*, vol. 8704, Baltimore, MD, USA, Jun. 2013, Art. no. 87041H. [Online]. Available: http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=1697161
[9] *Infrared Parts Manual*, Glolab Corporat., 307 Pine Ridge Drive, Wappingers Falls, NY, USA, 12590. [Online]. Available: http://www.glolab.com./pirparts/pirmanual.PDF
[10] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge, U.K.: Cambridge Univ. Press, 2001.
[11] Y. Nemirovsky, D. Corcos, I. Brouk, A. Nemirovsky, and S. Chaudhry, "1/f noise in advanced CMOS transistors," *IEEE Instrum. Meas. Mag.*, vol. 14, no. 1, pp. 14–22, Feb. 2011.



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