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Realizing Efficient Volume Depletion in SOI Junctionless FETs

SHUBHAM SAHAY AND MAMIDALA JAGADESH KUMAR (Senior Member, IEEE)

Department of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi 110016, India

CORRESPONDING AUTHOR: S. SAHAY (e-mail: eez142401@ee.iitd.ac.in)

ABSTRACT In this paper, we provide a simple and effective solution to realize efficient volume depletion and therefore, significantly reduce the OFF-state leakage current of a junctionless FET (JLFET) by replacing the SiO_2 by HfO_2 in the buried oxide (BOX). Using calibrated 2-D simulations, we show that the JLFET with a high-k BOX (HB JLFET) exhibits a considerably high I_{ON}/I_{OFF} ratio of $\sim 10^6$ even for a channel length of 20 nm. Further, we demonstrate that the use of a high-k BOX leads to a reduction in both gate capacitance C_g and gate-to-drain feedback (Miller) capacitance C_{gd}.

INDEX TERMS Junctionless transistor (JLFET), OFF-state leakage current, ON-state to OFF-state current ratio.

I. INTRODUCTION

The stringent requirement of an ultra-steep doping profile at the metallurgical junctions restricts the scaling of the conventional MOSFETs. Therefore, field effect transistors having no metallurgical junctions at the source-channel and channel-drain interface were proposed [1]–[7] to overcome the constraint of ultra-sharp doping profiles and higher thermal budgets to activate the dopants. Junctionless FETs (JLFETs), thus, exhibit an easier fabrication process and a low thermal budget which enables flexibility in the choice of materials for the gate electrode and gate oxide [1]–[4]. Therefore, JLFETs appear to be a promising alternative to the conventional MOSFETs. However, the SOI JLFETs require ultra-thin SOI films of thickness ≤ 5 nm [2] and gate work functions in excess of 5.5 eV to achieve volume depletion in the OFF-state for highly doped n-channel devices. Uniform ultra-thin (5 nm) SOI substrates are difficult to manufacture and add to the fabrication cost. Such structures are impractical to fabricate. Recently, a bulk junctionless device [3] was proposed which solves some of these problems but suffers from the process complexity of a trigate architecture and the limitation of a high gate electrode work function (5.5 eV).

In this paper, we demonstrate a simple and effective means of overcoming the aforementioned limitations of SOI junctionless FETs by using a high-k BOX along with a heavily doped ground plane. The proposed JLFET with a high-k BOX (HB JLFET) facilitates the depletion of the active device layer from the bottom reducing the effective active device layer thickness. As a result, volume depletion is achieved even for a SOI film thickness of 10 nm leading to a significantly reduced leakage current. It may be noted that to realize volume depletion in a 10 nm thick active device layer in a JLFET, either a gate electrode with a very high work function (in excess of 5.93 eV) or a large negative gate bias or substrate bias (both in excess of V_{dd}) is needed, therefore, demanding an additional power supply or a charge pump circuitry which results in an enhanced area overhead and routing complexity for the circuit designers. However, the main purpose of our work is to demonstrate that without using such a large negative gate/substrate bias or a practically unfeasible high gate work function, effective volume depletion can be achieved even at $V_{GS} = 0$ V when the SOI thickness is 10 nm. Using calibrated 2-D simulations, we demonstrate that the HB JLFET shows a reduction in the OFF-state leakage current by six orders of magnitude even for a channel length of 20 nm when the high-k (HfO_2) thickness is 10 nm and the ground plane is heavily doped. Further, we show that the gate capacitance C_g and the gate-to-drain feedback (Miller) capacitance C_{gd} are also reduced in the HB JLFET compared to the conventional SOI JLFET.

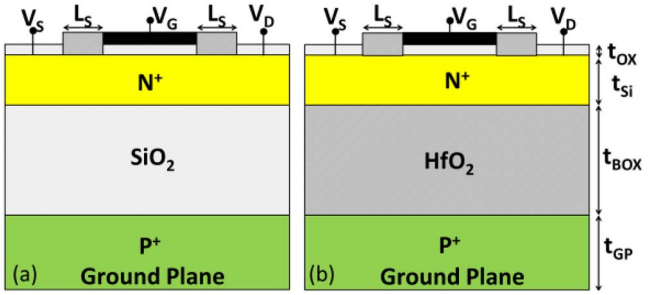

FIGURE 1. Schematic view of (a) the conventional SOI JLFET and (b) the JLFET with a high-k BOX (HB JLFET).

II. DEVICE STRUCTURE AND SIMULATION PARAMETERS

Fig. 1 shows the schematic view of the conventional SOI JLFET and the JLFET with a high-k BOX (HB JLFET). The only difference between the two structures is that the latter has a high-k dielectric (HfO_2) BOX compared to the SiO_2 BOX in a conventional SOI JLFET. Earlier publications and [8] in particular, have described various fabrication methods to obtain SiO_2 BOX wafers but there is no experimental evidence of SOI wafers with any high-k dielectric replacing the SiO_2 BOX. Further, the possibility of using a buried high-k dielectric has not even been explored by simulation. Therefore, the concept of SOI wafers with HfO_2 BOX is completely new. Since the SiO_2 BOX wafer manufacturing is well established [8], realizing HfO_2 BOX wafers using the smart-cut method should not encounter any unexpected difficulty. Using the detailed information about the various processes used for fabricating SiO_2 BOX wafers in [8], we have proposed a process flow for the fabrication of HfO_2 BOX wafers using the smart-cut process as shown in Fig. 2. Using the smart-cut process, it is possible to realize a 10 nm silicon film thickness [8]. The suggested process steps to realize a high-k BOX SOI wafer are as follows:

Step 1: HfO_2 is deposited on the "seed" wafer. This HfO_2 becomes the buried oxide (BOX).

'**Step 2:** Hydrogen ions are implanted into the "seed" wafer through the oxide with a dose that is typically $> 5\times10^{16}$ cm^{-2} [8].

Step 3: The "seed" wafer is transferred on to the "handle" wafer.

Step 4: The two wafers are bonded using a fusion process.

Step 5: By heating the bonded wafer pair at a temperature of 400–600 °C, the wafers can be split along the hydrogen implanted plane. The as-split wafer surface is polished using CMP to achieve a smooth surface.

The parameters used for the devices in our simulations are listed in Table 1. It may be noted that the doping concentration of the ground plane is higher than the one commonly used in ultra-thin BOX (UTB) devices.

III. SIMULATION RESULTS AND DISCUSSION

The simulations were carried out using Sentaurus tool [9]. Lombardi mobility model and Philips unified mobility model were used to consider both the doping dependent mobility and the transverse-field dependent mobility. Shockley-Read-Hall (SRH), Auger recombination model and Fermi-Dirac statistics were also enabled. Further, the electron and the hole lifetimes were changed to 10^{-7} s which corresponds to the carrier lifetime at a doping concentration of $\sim10^{19}$ cm^{-3}. Bandgap narrowing (BGN) model was included to account for the highly doped device regions. No tunneling models were included in our simulations. The ground plane is at the same potential with respect to the source which is grounded. The simulation models were calibrated by reproducing the results reported for the bulk planar junctionless transistor (BPJLT) in [5] by using the same device structure and parameters (i.e., by using $N_D = 1.5\times10^{19}$ cm^{-3}) as shown in Fig. 3(a). Further, the results reported in [5] were calibrated by replicating the experimental results of [1]. Then, these calibrated models were used for performing

TABLE 1. Parameters used for the device simulation.

Parameter	HB JLFET	JLFET
Silicon film doping (N_D)	1 x 10^{19} cm^{-3}	1 x 10^{19} cm^{-3}
SOI film thickness (t_{Si})	10 nm	10 nm
BOX thickness (t_{BOX})	10 nm (HfO_2)	10 nm (SiO_2)
Gate oxide (SiO_2) thickness (t_{OX})	1 nm	1 nm
Gate work function	5.1 eV	5.1 eV
Gate length (L_G)	20 – 100 nm	20 – 100 nm
Distance between Gate and S/D contacts	25 nm	25 nm
Ground plane doping (N_A)	1 x 10^{20} cm^{-3}	1 x 10^{20} cm^{-3}

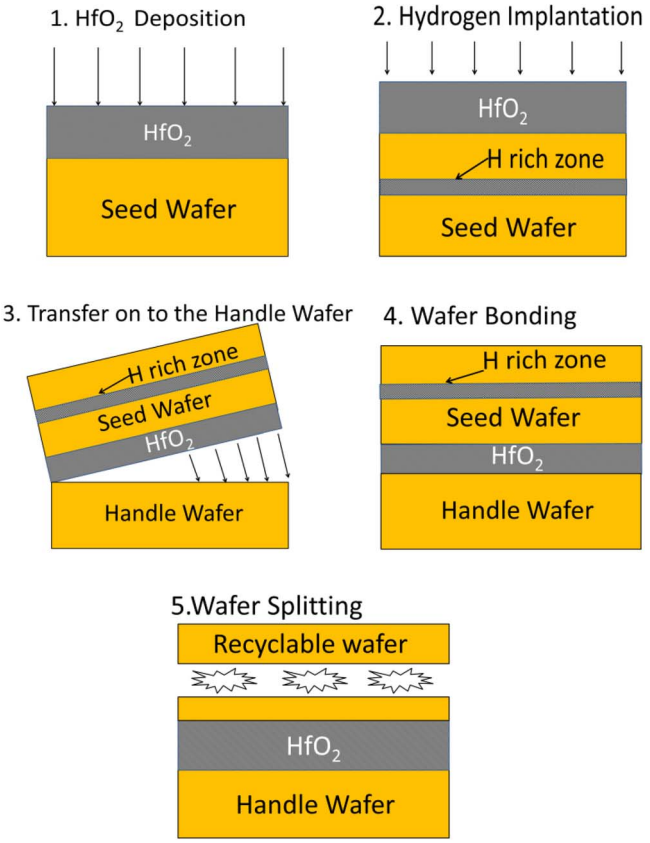

FIGURE 2. Suggested process flow to realize the high-k BOX SOI wafers based on the smart-cut process described in [8].

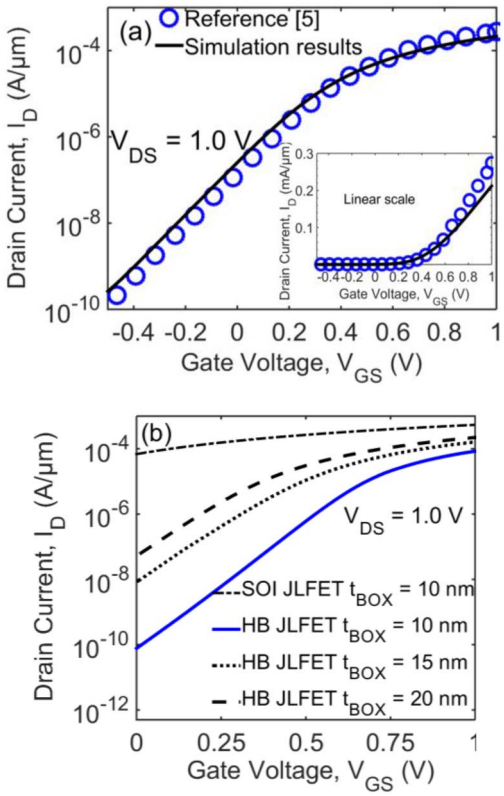

FIGURE 3. **(a) Simulation models calibrated by reproducing the results of [5] (average subthreshold slope of the simulated result = 165 mV/dec and that of [5] = 152 mV/dec) and (b) Transfer characteristics of the conventional SOI JLFET and the HB JLFET for different BOX thicknesses (t_{BOX}).**

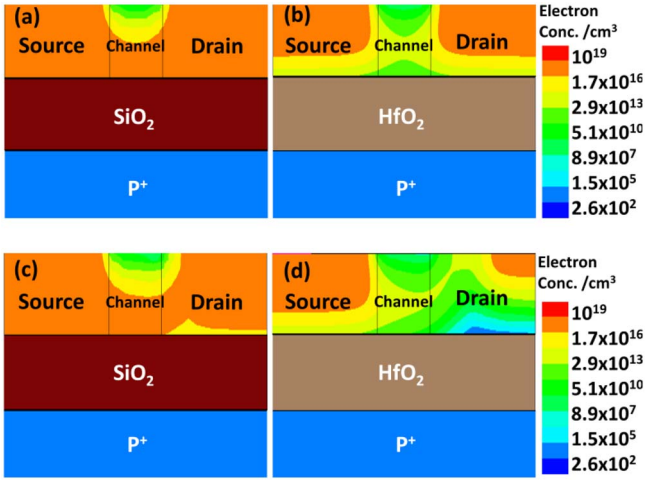

FIGURE 4. **Electron concentration contour plot of (a) the conventional SOI JLFET and (b) the HB JLFET in the thermal equilibrium state (V_{GS} = 0.0 V and V_{DS} = 0.0 V) and (c) the conventional SOI JLFET and (d) the HB JLFET in the OFF-state (V_{GS} = 0.0 V and V_{DS} = 1.0 V).**

the device simulations with $N_D = 1\times10^{19}$ cm^{-3} as given in Table 1. As can be observed from Fig. 3(a), the ON-state current and the subthreshold swing of the simulated results are somewhat degraded compared to the results reported in [5]. However, it may be noted that the main objective of this work is not to show the exact values of the currents, but to demonstrate the relative electrostatic effect of the high-k BOX on the electrical characteristics of the SOI JLFET.

The transfer characteristics of the conventional SOI JLFET and the proposed HB JLFET for different BOX thicknesses (t_{BOX}) are shown in Fig. 3(b). The OFF-state leakage current of the conventional SOI JLFET is very high as volume depletion is not achieved at $V_{GS} = 0$ V when the SOI thickness is 10 nm [5]. However, the OFF-state leakage current is reduced by six orders of magnitude for a HB JLFET (t_{BOX} = 10nm) compared to the conventional SOI JLFET. Further, as can be seen from [5], the HB JLFET has a lower OFF-state leakage current than the BPJLT. From the thermal equilibrium electron concentration contour plot shown in Fig. 4(a) and 4(b), we observe that the effective active layer thickness in a HB JLFET is lesser than the actual physical device layer thickness because of the depletion of the active device layer from the bottom. As a result, as shown in Fig. 4(c) and 4(d), the channel region in the HB JLFET is effectively volume depleted compared to the conventional SOI JLFET in the OFF-state. This significantly reduces the OFF-state leakage current in the HB JLFET compared to the conventional SOI JLFET.

Fig. 5(a) compares the OFF-state leakage current of the conventional SOI JLFET and the HB JLFET for different channel lengths. We observe that even when the channel length is reduced to 20 nm, the OFF-state leakage current of the HB JLFET is six orders lesser than the conventional SOI JLFET. This results in a drastically large ON-state to OFF-state current ratio (I_{ON}/I_{OFF} of $\sim10^6$) in a HB JLFET even for a channel length of 20 nm as observed in Fig. 5(b).

Fig. 6(a) shows the effect of ground plane doping on the transfer characteristics of the HB JLFET. As the ground plane doping reduces, the effective work function decreases resulting in a lesser depletion of the active device layer of the HB JLFET leading to an increased OFF-state leakage current. The impact of the traps at the Si-HfO_2 interface on the performance of the HB JLFET is shown in Fig. 6(b). For both acceptor and donor traps, a trap density of 1.5 x 10^{12} cm^{-2} located at the midgap [10] with a capture cross section of 2 x 10^{-13} cm^2 for the acceptor traps and 7 x 10^{-16} cm^2 for the donor traps [11] were used. We observe that the OFF-state leakage current decreases in the presence of the acceptor type traps while it increases when donor type traps are present. The acceptor traps become negatively charged upon ionization and hence, facilitate the depletion of the active device layer from the bottom [12]. However, the donor type traps become positively charged upon ionization leading to electron accumulation at the bottom of the active device layer and hence, screening the depletion of the active device layer from the heavily doped ground plane [12]. When both types of traps are present, the transfer characteristics are similar to those with only donor traps present.

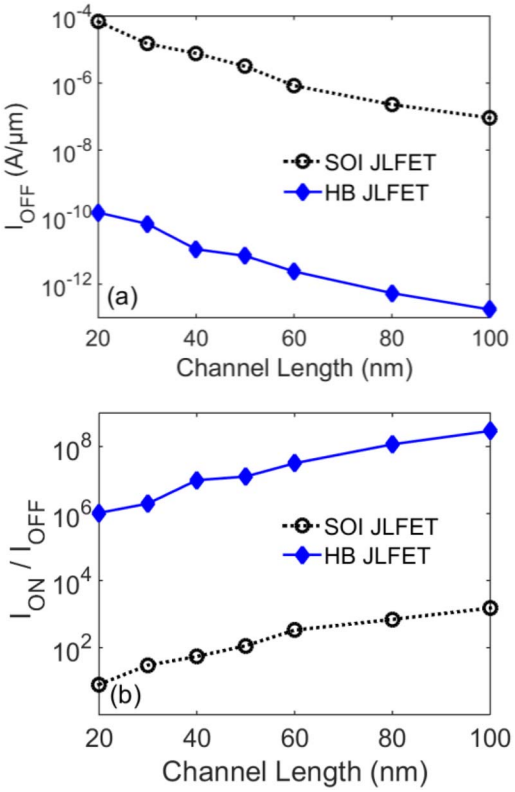

FIGURE 5. Variation of (a) the OFF-state leakage current and (b) the ON-state to OFF-state current ratio of the conventional SOI JLFET (t_{BOX} = 10 nm) and the HB JLFET (t_{BOX} = 10 nm) with the channel length.

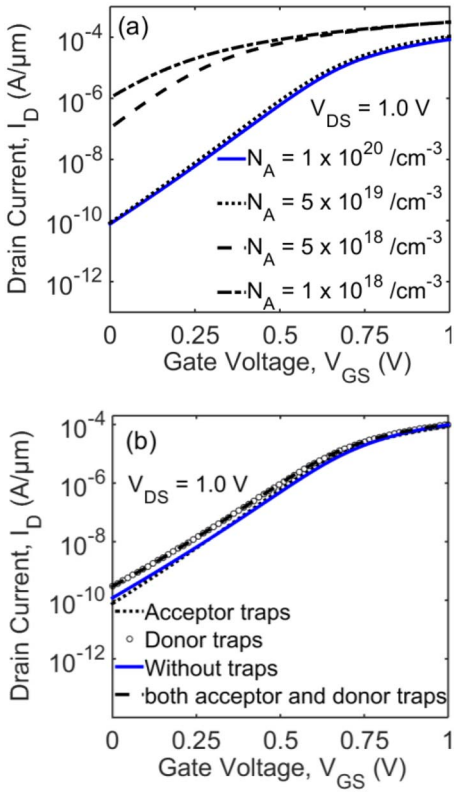

FIGURE 6. Transfer characteristics of the HB JLFET (t_{BOX} = 10 nm) (a) for different ground plane dopings and (b) in the presence of different types of traps.

Fig. 7 compares the transfer characteristics of the HB JLFET and the conventional SOI JLFET with different gate electrode work functions and in the presence of a substrate bias of -V_{dd}. It can be observed that the OFF-state current in the conventional SOI JLFET with a substrate bias of -1.0 V is still 10^4 times higher than that of the HB JLFET. This leads to a drastically low value of I_{ON}/I_{OFF} ratio ($\sim 10^2$) in the conventional SOI JLFET even in the presence of a substrate bias. Therefore, volume depletion can be achieved in the conventional SOI JLFETs only when either a large negative substrate bias $\ll$ -V_{dd} or a gate electrode with a work function $>$ 5.93 eV is employed. However, a gate electrode with a work function $>$ 5.93 eV is not practically feasible. Therefore, to attain a considerably low OFF-state current in the conventional SOI JLFETs, an additional power supply greater than V_{dd} or a charge pump circuit would be required for substrate biasing. Both these techniques would lead to an increased area overhead and an enhanced routing complexity for the circuit designers. Therefore, HB JLFET would be a promising alternative to the conventional SOI JLFETs.

Further, the conventional SOI JLFET with a substrate bias of -V_{dd} does not satisfy the ITRS specification [13] of the OFF-state current I_{OFF} for either low standby power (10^{-11} A/μm) or for high performance (10^{-7} A/μm). Therefore, a performance metric of I_{ON}/I_{OFF} and

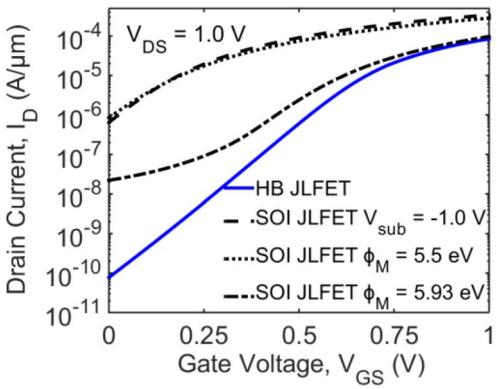

FIGURE 7. Transfer characteristics of the HB JLFET (t_{BOX} = 10 nm) and the conventional SOI JLFET (t_{BOX} = 10 nm) with different gate electrode work functions and in the presence of a substrate bias of -V_{dd}.

$I_{ON}/(I_{OFF} \times C_g)$, where C_g is the gate capacitance, has been chosen to compare the devices as shown in Fig. 8. The OFF-state current of the conventional SOI JLFET decreases with negative substrate bias because of the enhanced depletion from the bottom leading to an increase in the I_{ON}/I_{OFF} and $I_{ON}/(I_{OFF} \times C_g)$. Table 2 shows the I_{ON}/I_{OFF} and $I_{ON}/(I_{OFF} \times C_g)$ for the HB JLFET in the presence of different types of traps at the Si-HfO_2 interface. We observe that both I_{ON}/I_{OFF} and $I_{ON}/(I_{OFF} \times C_g)$ reduce in the presence of traps.

TABLE 2. Performance of the HB JLFET in the presence of traps.

Type of trap	I_{ON}/I_{OFF}	$I_{ON}/(I_{OFF} \times C_g)$ $(F/\mu m)^{-1}$
No traps	1.10×10^{6}	4.24×10^{21}
Only acceptor traps	7.98×10^{5}	2.65×10^{21}
Only donor traps	4.22×10^{5}	1.36×10^{21}
Both acceptor and donor traps	3.27×10^{5}	1.05×10^{21}

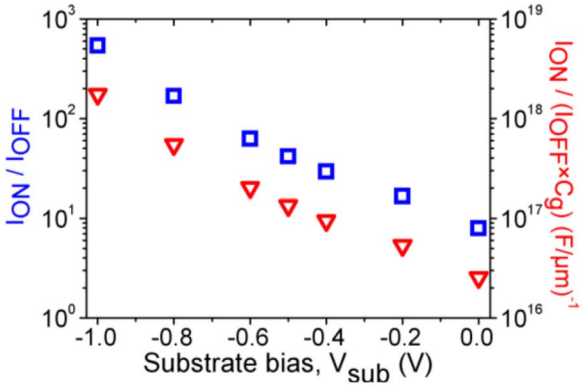

FIGURE 8. The variation of I_{ON}/I_{OFF} and $I_{ON}/(I_{OFF} \times C_g)$ for different substrate bias in the conventional SOI JLFET (t_{BOX} = 10 nm).

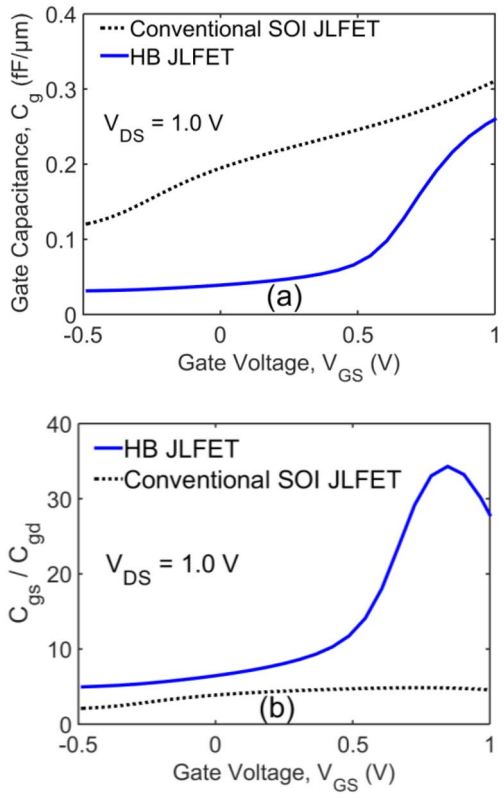

FIGURE 9. The variation of (a) the gate capacitance (C_g) and (b) the C_{gs} to C_{gd} ratio of the conventional SOI JLFET (t_{BOX} = 10 nm) and the HB JLFET (t_{BOX} = 10 nm) with the gate voltage.

Fig. 9(a) shows the variation of the gate capacitance C_g with respect to the gate voltage V_{GS}. The gate capacitance in a conventional SOI JLFET is higher than the HB JLFET due to a thinner depletion region width caused by insufficient volume depletion in the conventional SOI JLFET. However, in a HB JLFET, due to the depletion from both top and bottom, the depletion layer width is large and hence the depletion capacitance is low which comes in series with the oxide capacitance making the overall gate capacitance low. Similarly, as shown in Fig. 3(d), the drain region at the channel-drain interface is depleted in the HB JLFET which leads to a depletion capacitance in series with the gate to feedback capacitance C_{gd} and hence, reduces the Miller capacitance significantly. Therefore, the ratio of gate to source capacitance C_{gs} and the gate to drain feedback capacitance C_{gd} is significantly larger in the HB JLFET compared to the conventional SOI JLFET. A high C_{gs}/C_{gd} ratio means a better control of channel charge by the gate and a lower Miller capacitance [14]. Therefore, the use of high-k BOX in a JLFET improves the high-frequency performance.

IV. CONCLUSION

In this paper, we provide a simple and efficient means to significantly reduce the OFF-state leakage current in a JLFET by replacing the SiO_2 BOX with HfO_2 BOX. Using calibrated 2-D simulations, we have demonstrated that the JLFET with a high-k BOX depletes the active device layer from the bottom and hence, results in a reduced effective active device layer thickness compared to the physical thickness. Therefore, volume depletion is achieved even for a SOI film thickness of 10 nm in a HB JLFET. The proposed device provides a reduction in the OFF-state leakage current by six orders of magnitude compared to the conventional SOI JLFET and a significantly improved I_{ON}/I_{OFF} ratio of $\sim 10^6$ even when the channel length is 20 nm. The proposed HB JLFET could be a lucrative alternative to the conventional SOI JLFETs. Our results may provide the incentive for the experimental realization of this structure.

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SHUBHAM SAHAY received the B.Tech. (Hons.) degree in electronics engineering from the Indian Institute of Technology, BHU, Varanasi, India, in 2014. He is currently pursuing the Ph.D. degree in electrical engineering with the Indian Institute of Technology, New Delhi, India. He was a recipient of four gold medals for obtaining the highest marks and securing the first position in his B.Tech. degree.

His current research interests include semiconductor device design and modeling.

MAMIDALA JAGADESH KUMAR (SM'98) is a Professor of Electrical Engineering with the Indian Institute of Technology, New Delhi, India. He is currently the Vice-Chancellor of Jawaharlal Nehru University, New Delhi. He has widely published in the area of micro/nanoelectronics and is known for his excellence in teaching. He was an Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES from 2006 to 2015. He is an Editor of the IEEE JOURNAL OF THE ELECTRON DEVICES SOCIETY. He is a member (PT) of Telecom Regulatory Authority of India. More details about Dr. Kumar can be found at http://web.iitd.ac.in/∼mamidala.