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Impact of Channel Thickness Variation on Bandstructure and Source-to-Drain Tunneling in Ultra-Thin Body III-V MOSFETs

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ABSTRACT In nanoscale MOSFETs with sub-10 nm channels, the source-to-drain tunneling is expected to be a critical bottleneck, especially in III-V devices on account of their extremely low effective masses. Also, to maintain electrostatic integrity at extremely small gate lengths, the channels need to be made ultrathin. In such devices, the bandstructure of the channel material becomes thickness dependent due to quantum confinement effects, and deviates remarkably from that of the bulk material. In this paper, we use first principle density functional theory calculations to evaluate the variation of the effective mass and bandgap with channel thickness. Then, we perform semi-classical ballistic and full quantum non-equilibrium Green's function transport simulations to study the impact on source-to-drain tunneling in III-V nMOSFETs. We demonstrate that the severity of the expected degradation due to source-to-drain leakage is reduced significantly, when the beneficial impacts of change in bandstructure, and multi-valley transport are taken into account.

INDEX TERMS III-V MOSFET, source-to-drain tunneling, quantum confinement, effective mass, bandgap, NEGF.

I. INTRODUCTION

Quantum mechanical tunneling of carriers from the source to the drain is believed to be the major determinant of the ultimate transistor scaling limits [1], [2]. The tunneling probability through a barrier can be expressed using the well known WKB method as:

$$T(E) = exp\left(\frac{-2}{\hbar}\int \sqrt{2m_e^*\,(E_{barrier}(x) - E)}\,dx\right) \qquad (1)$$

where m_e^* is the transport effective mass of electron, $E_{barrier}(x)$ is the channel potential energy barrier between source and drain, and E is the electron energy with $E_{barrier}(x) > E$ in the tunnel region. III-V MOSFETs are the prime candidates for the 7 nm node and beyond [3]. However, it is evident from (1) that tunneling through the barrier is expected to be a lot more severe in III-V MOSFETs due to their smaller m_e^*. Some studies [4] have indeed reported drastic increase in the subthreshold current and the subthreshold slope (SS) due to source-to-drain tunneling (SDT) in III-V channel MOSFETs, imposing a longer limit to the gate length scaling compared to Si devices. But these studies have used bulk m_e^*, and hence are questionable. In this paper we show that it is crucial to consider the change in the bandstructure in the quantum confined thin channels for proper estimation of source to drain tunneling.

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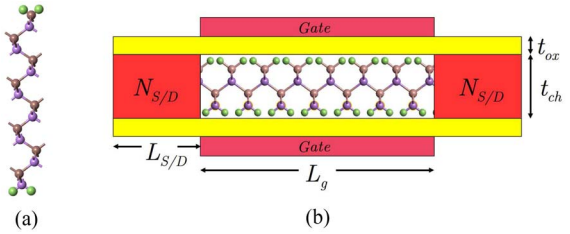


FIGURE 1. **(a) InAs cell structure (b) Schematic of devices used in the simulations. Gate length (L_g) = 6.6 nm, channel thickness (t_{ch}) = 2.43 nm, effective oxide thickness (EOT) = 0.47 nm, gate oxide: HfO_2 ($\epsilon_{ox} = 25$), source/drain length ($L_{S/D}$) = 7.5 nm, source/drain doping ($N_{S/D}$) = 2×10^{20} cm^{-3}, channel: undoped (intrinsic). The HfO_2/InAs and HfO_2/InSb barrier offset values are taken from [5]. Wafer orientation is (100) and transport is along [100] direction.**

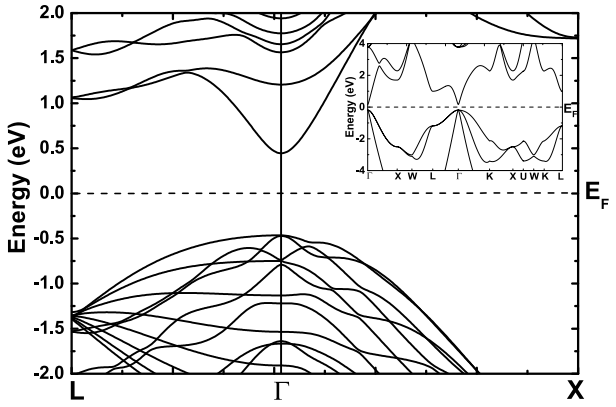


FIGURE 2. **Bandstructure of 2.43 nm thick InAs slab (16 atomic layers) calculated using DFT ($m_e^* = m_{DFT} = 0.0944\ m_0$, $E_g = 0.91$ eV). *Inset:* InAs Bulk Bandstructure ($m_e^* = m_{Bulk} = 0.023\ m_0$, $E_g = 0.35$ eV).**

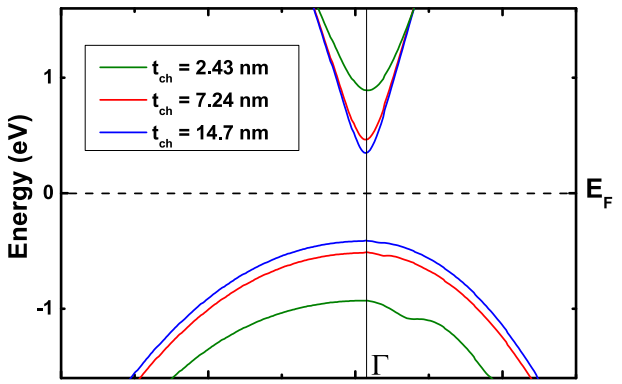


FIGURE 3. **Conduction and valence band edges for different InAs channel thicknesses (Blue: 14.7 nm, Red: 7.24 nm, Green: 2.43 nm). Thinner the device, higher are the electron effective mass and bandgap.**

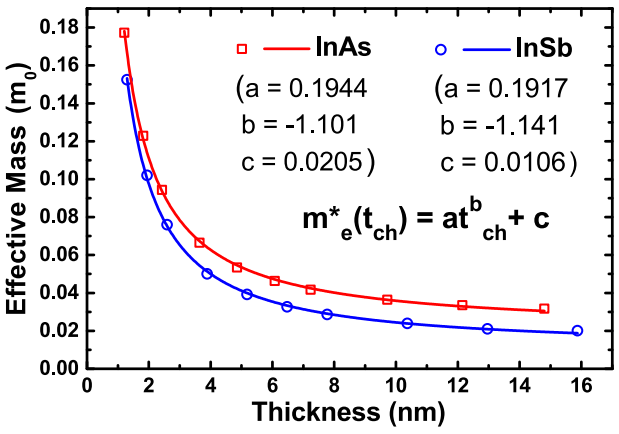
II. THICKNESS DEPENDENT BANDSTRUCTURE

As we approach the end of the ITRS roadmap, the channel thickness needs to be scaled to less than 6 nm while the gate length reduces to less than 10 nm [6]. In such extremely confined channels, using the parabolic effective-mass approach with bulk m_e^* is no longer valid [7] as m_e^* increases with confinement [8]. While the variation of m_e^* is reported to be quite small in case of Si [9], it can be quite appreciable in III-V materials, as shown by tight binding calculations [10], [11], and the empirical pseudo-potential method [12]. Similarly, the bandgap (E_g) has also been shown to increase as the channel is made thinner [13]. These effects cannot be neglected and have profound impact on the performance of transistors utilizing these high mobility compound semiconductors as channel materials [14].

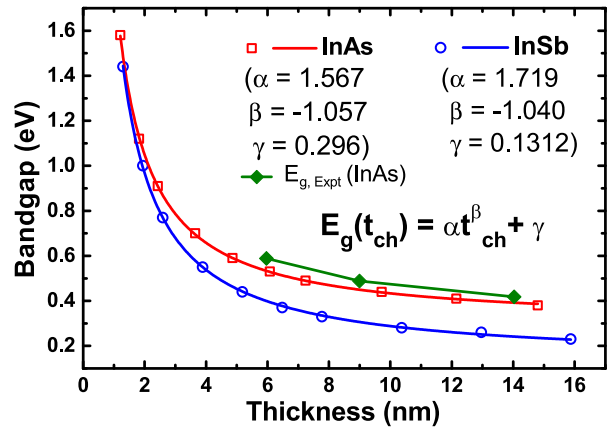
In this work, we calculate the band structure of (100) oriented InAs slabs with varying thicknesses using first principles DFT calculations based on the conventional Kohn Sham Hamiltonian. Meta Generalized Gradient Approximation [15], as implemented in ATK [16] is used for treating the exchange correlation. Fritz Haber Institute (FHI) pseudopotential having double zeta polarized basis sets are employed for In and As. Surface dangling bonds are passivated using an sp^3 hybridization scheme. Previously reported optimized lattice constants for InAs are considered for calculations [17]. The InAs cell structure is depicted in Fig. 1(a).

The bandstructure of 2.43 nm (16 atomic layers) thick InAs body is shown in Fig. 2. The inset shows the bandstructure of the bulk material. For a clear comparison of the thickness dependence of the bandstructure, the conduction and valence band edges for three channel thicknesses (t_{ch}) are shown in Fig. 3. It can be seen that the Γ valley bandgap increases while the band curvature decreases with decrease in t_{ch}. Similar results are obtained for InSb. Thickness dependent variation of m_e^* and E_g has been shown in Fig. 4. In our thickness dependent effective mass approximation approach, m_e^* are calculated at the conduction band minima by fitting the $E-k$ dispersion with a parabola for each channel thickness. Our results are in close agreement with experimental data, for example [13]. Further, we have fit the m_e^* and E_g values into thickness dependent empirical models (details in Fig. 4). These can be very useful for incorporation in TCAD programs and in compact modeling of III-V devices which need these material parameters, without resorting to atomistic calculations for arbitrary channel thicknesses. Fig. 5 shows the variation of energy offsets between the Γ and L/X valleys with t_{ch}.

The transverse and longitudinal electron effective masses (m_t and m_l respectively) in the L valley for different thicknesses are shown in Table 1. The calculated values for the effective masses for bulk InAs are close to those reported in [18]. The effective masses along the three axes in the device coordinate system (transport mass, m_x; transverse mass, m_y; and confinement mass, m_z) are calculated as per [10] and [19]. It is interesting to note that although the L valley transport and transverse effective masses are smaller than the bulk values (unlike the case for Γ valley), they still increase with t_{ch} scaling in the range of thicknesses considered.



(a)



(b)

FIGURE 4. **(a) m_e^* of electrons in the Γ valley, and (b) E_g as a function of the channel thickness for InAs and InSb. Symbols: DFT calculations, Solid curves: Empirical Relations, given by $m_e^*(t_{ch}) = at_{ch}^b + c$ (Root mean square error (RMSE) in the fit = 0.12% for InAs, and 0.11% for InSb). $E_g(t_{ch}) = \alpha t_{ch}^{\beta} + \gamma$ (RMSE = 0.4718% for InAs, and 0.5936% for InSb). The green symbols in figure (b) are the experimental bandgap values for InAs [13].**

III. SOURCE TO DRAIN TUNNELING IN III-V MOSFETS

We have simulated double gate MOSFETs as shown in Fig. 1(b), using NanoMOS [20], whose parameter values are chosen following the ITRS 2013 projections for III-V MOSFETs for the year 2025 [6]. For carrier transport along the channel, uncoupled mode space approach is used where transport in each subband is treated as an effective 1D problem. We discuss two cases: (i) the semi-classical top of the barrier model where the 1D Boltzmann's equation is solved in the ballistic limit without considering any tunneling, and (ii) quantum ballistic transport using the non-equilibrium Green's function (NEGF) formalism [21], which captures the SDT current. As a justification for our DFT effective mass approach with ballistic transport, we note that in [22] a similar approach with m_e^* extracted from TB bandstructure (instead of DFT) for InGaAs and strained Si FinFETs (and full quantum transport) has been demonstrated to result in $I_{DS} - V_{GS}$ characteristics that are almost identical

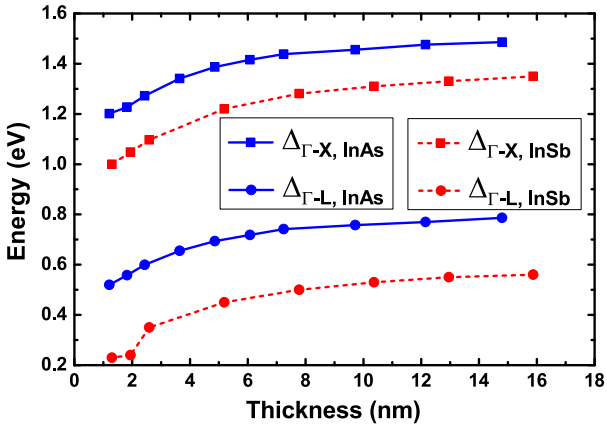


FIGURE 5. **Energy separation of the L and X valley minimas from the Γ valley minimum as a function of channel thickness for 1-D confined InAs and InSb ultra-thin bodies.**

TABLE 1. **L valley electron effective masses (obtained from DFT calculations).**

InAs			InSb		
t_{ch} (nm)	m_t	m_l	t_{ch} (nm)	m_t	m_l
1.21	0.154	0.91	1.296	0.128	0.93
1.82	0.144	0.74	1.944	0.118	0.68
2.43	0.137	0.73	2.592	0.118	0.63
Bulk	0.12	1.82	Bulk	0.096	1.57

to those obtained from a full TB model, with the respective on-currents differing only by around 5%. Similarly, it was shown in [10] that the use of a body-thickness dependent effective mass obtained from TB (and semi-classical ballistic (SCB)/top of the barrier model for transport) match the transport calculations using full TB analysis, except for some difference in injection velocity in strong inversion. Hence it is reasonable to apply the effective mass approach (with masses extracted from the DFT bandstructure) with NEGF transport, especially since in this work we focus on the sub-threshold regime. In this context, we would like to note that we have not included the variation of effective mass with energy, or non-parabolic effects in our calculations, as has been very recently reported in [23]. This is beyond the scope of the present work, and may be a subject of a future study.

To understand the impact of the change in effective mass on the SDT, the energy-resolved current density along the channel in an InAs MOSFET in the off-state in the quantum limit (i.e., only the lowest subband occupation [24]) has been plotted in Fig. 6. These simulations have been carried out considering quantum ballistic transport (NEGF). We have first adjusted the work functions to match off-currents (I_{OFF} of 100 nA/μm) for the two cases in semi-classical ballistic simulations and then the same values are used for the NEGF case. It can be seen that SDT under the barrier is higher when m_{Bulk} (lighter) is used (Fig. 6(a)) compared to the case when m_{DFT} (heavier) is used (Fig. 6(b)), in agreement with equation 1.

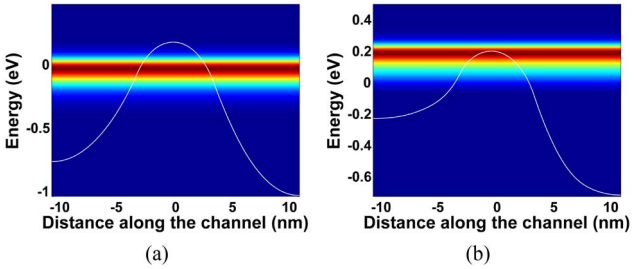


FIGURE 6. Energy-resolved current density in the off-state. (a) With m_{Bulk}: almost entire off current is due to SDT, and (b) With m_{DFT}: contribution of SDT is reduced while the thermionic current increases. (InAs MOSFET with $t_{ch} = 1.21$ nm, $L_g = 6.6$ nm).

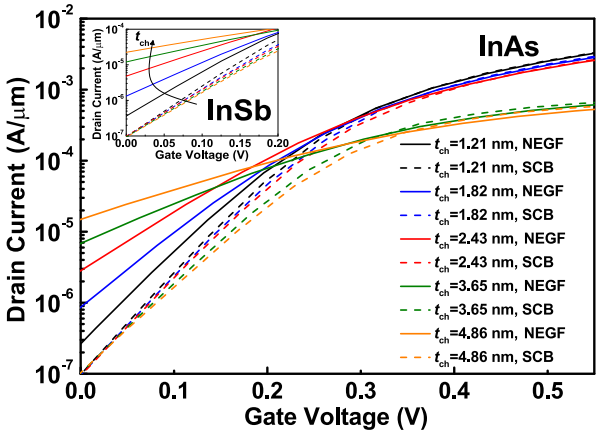


FIGURE 7. Transfer characteristics, $I_{DS} - V_{GS}$ plots for InAs and InSb MOSFETs ($V_{DS} = V_{DD} = 0.55$ V, $L_g = 6.6$ nm) $t_{ch,InAs} = 1.21$ nm, 1.82 nm, 2.43 nm, 3.65 nm, 4.86 nm. $t_{ch,InSb} = 1.29$ nm, 1.94 nm, 2.59 nm, 3.89 nm, 5.18 nm. Solid (dashed) curves correspond to the case when SDT is included (excluded). For semi-classical ballistic simulations, the devices are set to have the same I_{OFF} of 100nA/μm as per ITRS guidelines, using work function tuning. The same workfunctions are then used for the NEGF simulations. Both Γ and L valleys have been included. Impact of the Γ valley effective masses decreasing rapidly and asymptotically approaching the bulk values with increasing t_{ch} is evident in the sharp decline in the on-state currents as we go from 16 atomic layers (2.43 nm) to 24 atomic layers (3.65 nm) and beyond.

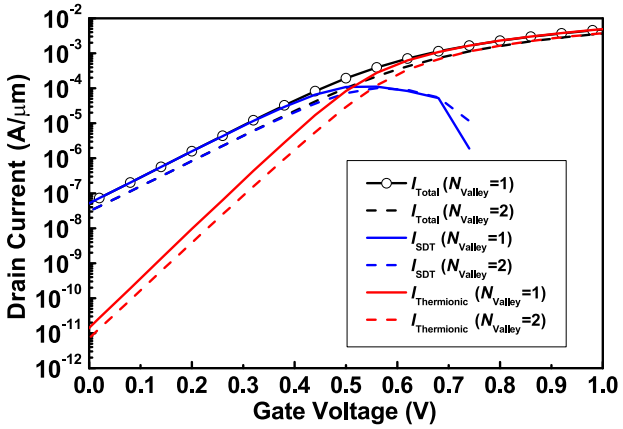


FIGURE 8. Impact of multi-valley transport on the total drain current (I_{Total}), the thermionic component ($I_{Thermionic}$) and the SDT component (I_{SDT}). (InSb MOSFET, $t_{ch} = 2.59$ nm, $L_g = 6.6$ nm, $V_{DS} = 0.55$ V). Simulation settings were identical for the two cases (no workfunction or V_{GS} shifts), except for difference in the number of valleys, N_{Valley}.

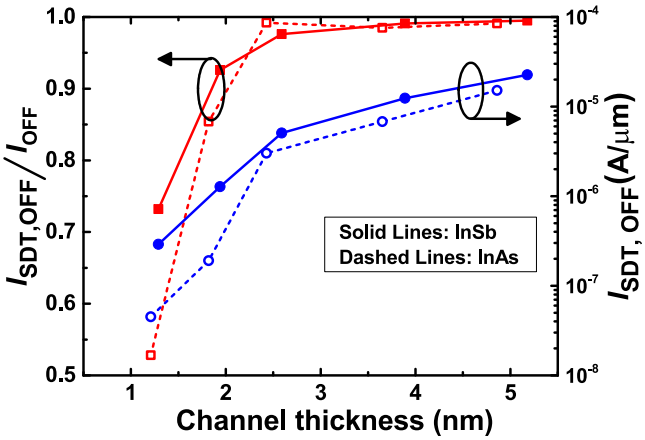


FIGURE 9. Off-state SDT current ($I_{OFF, SDT} = I_{OFF, NEGF} - I_{OFF, SCB}$) and ratio of SDT current to the total off-current. Extracted at $V_{GS} = 0$ V, $V_{DS} = 0.55$ V in InAs and InSb MOSFETs. $L_g = 6.6$ nm for different channel thicknesses. The gate workfunctions in the devices were set to have iso-I_{OFF} in the semi-classical ballistic case.

Along with the Γ valley, we have included the L valley in the rest of our simulations to account for any possible charge spill-over from Γ to L valley. $I_{DS} - V_{GS}$ characteristics of five InAs devices with different channel thicknesses with and without SDT, using m_{DFT} and $E_{g,DFT}$ for each thickness, are shown in Fig. 7. The inset shows the characteristics of InSb MOSFETs near off-state. The off-currents of InSb devices are higher than those of InAs devices due to the former having lighter effective masses and hence suffering from stronger SDT. It can be seen that the off-current is more than an order lower in semi-classical ballistic case compared to NEGF case, which justifies the importance of NEGF simulation, as was reported in [1] for a Si device using m_{Bulk}. It is also evident that the off-current (I_{OFF}) increases sharply with thicker channels and the subthreshold slope worsens.

Fig. 8 shows the total drain current (I_{Total}), the thermionic component ($I_{Thermionic}$) and the SDT component (I_{SDT}) for one valley and two valley cases. The extent of impact of the L valleys depends on a number of factors: the channel material, channel thickness, Γ-L separation ($\Delta_{\Gamma-L}$), values of the effective masses etc. Inclusion of both Γ and L valleys instead of only the Γ valley results in a reduction of the drain current: due to decrease in SDT in subthreshold, and due to an overall decrease of the injection velocity in strong inversion; both due to increased charge transport in the heavier L valley. The SDT current decreases with increasing gate bias and ultimately disappears at high bias, similar to the results reported in [25]. So there are two distinct regions - one dominated by SDT current and the other by thermionic current, separated by a crossover point in the $I_{DS} - V_{GS}$ characteristics.

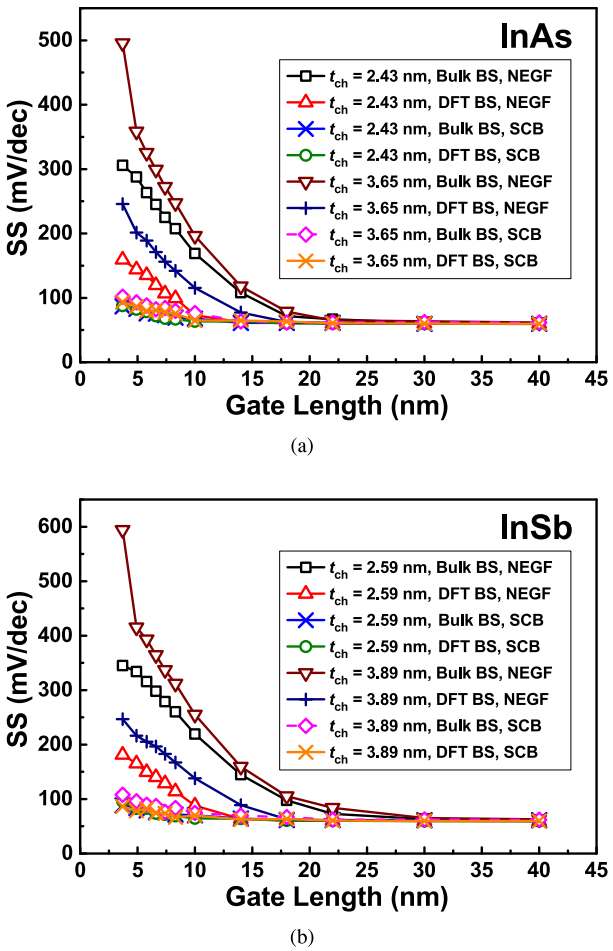


FIGURE 10. Comparison of SDT induced SS degradation in (a) InAs MOSFETs (t_{ch} = 2.43 nm, 3.65 nm) (b) InSb MOSFETs (t_{ch} = 2.59 nm, 3.89 nm). NEGF simulations capture the SS degradation due to SDT, which is seen to be reduced drastically when correct effective masses and bandgaps are used instead of the bulk values.

The variation in SDT current ($I_{OFF,\ SDT} = I_{OFF,\ NEGF} - I_{OFF,\ SCB}$) and the ratio of the SDT current to the total current at off-state with channel thickness for the two materials considering both Γ and L valleys, has been shown in Fig. 9. The gate workfunctions were set so as to have iso-I_{OFF} in semi-classical ballistic case. The SDT current is more in InSb devices, primarily because of the relatively lower effective mass in the Γ valley which dominates the charge transport. Since the effective masses increase and the energy offsets between Γ and L valleys ($\Delta_{\Gamma-L}$) decrease with decreasing channel thickness (implying an increased possibility of lighter Γ to heavier L valley transfer), SDT current is lesser in thinner devices. The fraction of SDT current in the total current increases and then saturates at thicker t_{ch}.

Variation of *SS* with gate length for devices for two channel thicknesses for InAs and InSb devices for semi-classical ballistic and NEGF transport simulations are shown in Fig. 10. In the devices with small t_{ch}/L_g ratios, the usual short channel effects due to loss of gate control are quite small since very good channel electrostatics is guaranteed. The subthreshold slope doesn't change much as we go from bulk bandstructure to DFT bandstructure in semi-classical ballistic simulation, approaching the thermal limit of 60 mV/dec as the gate length increases. Next, when the current is evaluated using the NEGF approach, SDT is taken into account. In this case, the use of bulk bandstructure for the UTB devices results in strong tunneling causing large off-currents and large degradation of the subthreshold slope and a longer critical gate length below which the device suffers from extremely poor switching behavior. However, the use of the increased m_e^* values obtained from the DFT bandstructure calculations results in reduced SDT, thereby improving the *SS*, and reducing the critical gate length. For example *SS* of 100 mV/dec is achievable at $L_g \approx 8$ nm for 2.43 nm thick InAs and $L_g \approx 9$ nm for 2.59 nm thick InSb MOSFETs. Thus, the expected deterioration in the switching characteristics is significantly less and device scalability improves when the effects of quantum confinement on the m_e^* and E_g are taken into account. Further, this improvement in subthreshold performance and gate length scaling in the SDT dominated regime can be boosted with t_{ch} scaling. Note that the *SS* values in Fig. 10 are higher for InSb than InAs MOSFETs due to the lighter effective masses, higher dielectric constant of InSb [26] and the slightly thicker channel used for InSb devices (but the same number of atomic layers as InAs) in the simulations.

IV. CONCLUSION

In this paper we have highlighted the impact of quantum confinement on the III-V material bandstructure and transport properties in extremely scaled MOSFETs. We have calculated the variation of effective mass of the electron in the Γ and *L* valleys which contribute to carrier transport, and E_g, with varying channel thickness for InAs and InSb based on density functional theory, and provided empirical relations for the same. In general we find that both the effective electron mass and the bandgap increase with decreasing channel thickness in III-V materials, and different valleys become energetically closer to each other. Using the thickness dependent m_e^* and E_g in quantum ballistic transport simulations (using non-equilibrium Green's function formulation) in extremely thin III-V devices, we demonstrate that the increased effective mass, increased bandgap, and multi-valley transport have a positive impact of mitigating the effect of source drain tunneling which is a major issue in ultra-short channel devices. We emphasize that for any realistic analysis of scaled III-V MOSFETs at the end of the ITRS roadmap, it is imperative to take these effects into account.

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