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Comparison of Pinning Voltage Estimation Methods in Pinned Photodiode CMOS Image Sensors

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ABSTRACT The pinning voltage is a key design parameter of pinned photodiode CMOS image sensors which significantly affects the device performances and which is often used by manufacturers to monitor production lines and for the optimization of technological processes. This paper presents a comparative study of pinning voltage estimation methods, which are based on both electrical measurements performed on isolated test structures (or on test structures arrays) and in-pixel measurements. It is shown, with the support of simulations and experimental measurements, that not all the estimation methods provide an absolute value of the pinning voltage. Moreover, this paper demonstrates that the commonly accepted theoretical definition of the pinning voltage does not correspond to the physical parameter which is measured with the existing methods.

INDEX TERMS CMOS image sensor, CIS, pinned photodiode, PPD, pinning voltage, characterization.

I. INTRODUCTION

Pinned Photodiode (PPD) CMOS Image Sensors (CIS) [1], are currently the main imaging technology for both scientific and commercial applications. The extremely fast ascent of these devices over more mature imaging technologies can be explained by both their low cost (with respect to Charge Coupled Devices) and outstanding noise performances compared to standard 3-transistors active pixel sensors (3T APS). A schematic drawing of a 4-transistors (4T) PPD-CIS pixel is shown in Fig. 1a. The pixel is composed of a PPD, which is the photosensitive element, a floating diffusion (FD) which is responsible for the charge-to-voltage conversion, and four other transistors (T1, T2 , T3 and TG in Fig. 1a), which correspond to the reset transistor, the source follower transistor, the column selection transistor and the transfer gate, respectively. The latter enables charge confinement within the PPD (TG off) during charge integration (Fig. 1b) and charge transfer from the PPD toward the FD (TG on) for readout of the signal (Fig. 1c). The peculiar "sandwiched" structure of the PPD (formed by a double p+np junction) brings two main advantages with respect to 3T APS:

- It strongly reduces the dark current of the device (by isolating the PPD depletion region from the generation centers located at the $SiSiO_2$ interface).
- It enables a "confinement" of the PPD potential between the substrate potential and the pinning voltage (V_{pin}), which therefore represents the maximum PPD potential. As a result, true charge transfer can be implemented, whereas only charge sharing is possible in 3T APS.

The V_{pin} plays a crucial role in the design of PPD CIS and often involves design trade-offs depending on the target application. In particular:

- A large V_{pin} value results in a large equilibrium full well capacity (EFWC) [3], which represents the maximum charge that can be stored by the PPD in dark conditions with the TG in accumulation mode (Fig. 1b).

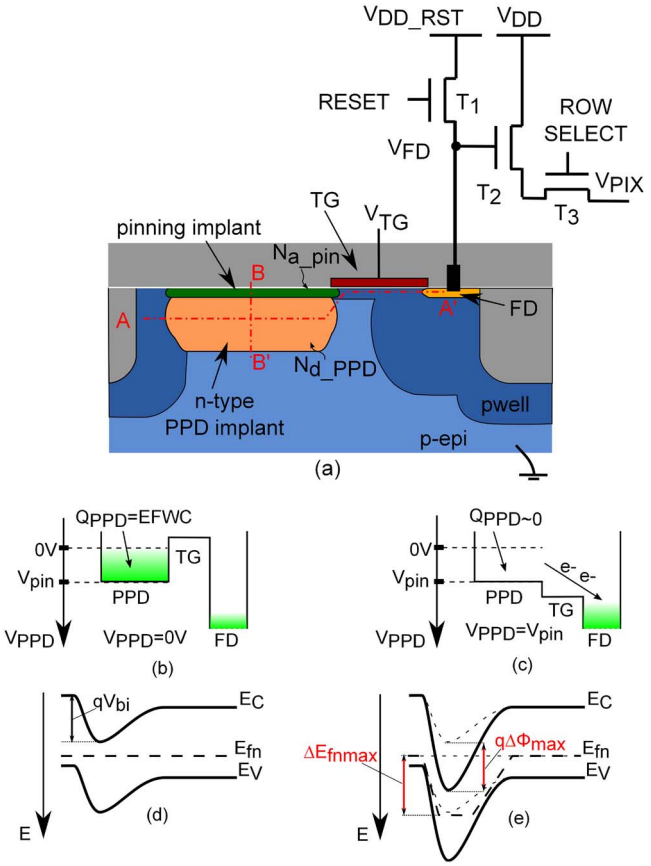

FIGURE 1. (a) Schematic representation of a PPD pixel. The schematic potential diagrams along the cut A-A′ at equilibrium and after charge transfer are shown in (b) and (c), respectively. The schematic energy band diagrams along the cut B-B′ at equilibrium and at full depletion conditions are shown in (d) and (e), respectively. The dashed curves in (e) represent the bands at equilibrium condition. FD stands for floating diffusion and TG for transfer gate. N_{a_pin} and N_{d_PPD} are the doping concentrations of the p-type pinning implant and of the n-type PPD implant, respectively. p-epi stands for p-type epitaxy. V_{bi} is the built-in voltage, $\Delta\Phi_{max}$ and $\Delta E_{fnmax}/q$ are the maximum variations of the electrostatic potential and of the electron quasi-Fermi levels, respectively, between equilibrium and full-depletion conditions [2]. q is the elementary charge.

- On the other hand, a small V_{pin} value often results in better charge transfer efficiency performances for given V_{DDRST} and TG biasing conditions.

This work addresses the definition and physical modelling of V_{pin} and discusses the working principle and the physical foundation of V_{pin} estimation methods used in the CIS community. In particular, it is shown that some methods provide arbitrary V_{pin} values, which depend on the experimental set-up. Moreover this study showed that the commonly accepted theoretical definition of the pinning voltage does not correspond to the physical parameter which is measured with the existing methods. This study is supported by both TCAD simulations and experimental data.

II. PINNING VOLTAGE: PHYSICS AND DEFINITION

The pinning voltage is commonly defined as the maximum deviation of the electron quasi-Fermi potential $\Delta E_{fnmax}/q$ between equilibrium (the PPD is as full as it can be in dark conditions) and full depletion conditions [4] (where it is assumed that the PPD is fully empty of minority carriers). The electron quasi-Fermi level E_{fnmax} is related to the concentration of minority carrier in the PPD n_{PPD} as [2]:

$$n_{PPD} = n_i e^{(E_{fn}-E_i)/kT} \tag{1}$$

with n_i the intrinsic carrier concentration, E_i the intrinsic Fermi level (at equilibrium), k the Boltzmann constant and T the temperature. In TCAD simulations, however, V_{pin} is often retrieved as the maximum variation of the electrostatic potential $\Delta\Phi_{max}$ [1], [5] (i.e., the deviation of the conduction band). As shown in the band diagrams in Fig. 1d and 1e, these two parameters ($\Delta E_{fnmax}/q$ and $\Delta\Phi_{max}$) represent two very different physical parameters which can differ, as discussed in this work, of several hundreds of mV.

A. TCAD SIMULATIONS

To gain a better insight on how the PPD potential (V_{PPD}) and the PPD charge (Q_{PPD}) change as a function of the biasing potential applied to the PPD, a possible approach is to simulate the structure in Fig. 2a, which corresponds to a PPD biased by means of two n+ implants located at both sides of the photodiode, i.e., to a Junction Field Effect Transistor (JFET) implemented with typical PPD implants (which will be referred to here as PPD-JFET structure). With respect to a full pixel (PPD+TG+FD), simulating a PPD-JFET structure has the advantage of allowing a symmetrical biasing of the PPD channel and guarantees that the potential applied to the PPD is not affected by the non-idealities of the TG. As addressed in this work, such JFET test structures represent a useful experimental tool to gain a better insight in the PPD physics and to optimize PPD technological processes. For this reason, V_{pin} is sometimes referred to as "*pinch-off voltage*" in analogy to the pinch-off voltage V_p of JFETs [6].

Figure 2b shows the maximum PPD electrostatic potential Φ, maximum electron quasi-Fermi level E_{fn} (divided by q for unit consistency) and maximum electron density Q_{PPD} (plotted in linear and logarithmic scales) as a function of the injection potential (V_{inj}) applied to a 3D PPD-JFET structure, such as the one in Fig. 2a. At small injection potentials, both Φ and E_{fn} increase as the reverse voltage V_{inj} applied to the p-n junction is increased [2]. As discussed in [7], the PPD capacitance can be considered roughly constant in this region, which explains the linear drop of Q_{PPD} with V_{inj}. If V_{inj} is further increased, the n-region of the PPD becomes eventually fully depleted and the electrostatic potential cannot increase any more. The saturation of the electrostatic potential corresponds to the biasing condition $V_{inj} = \Delta\Phi_{max}$. Note that the depletion condition does not imply that all minority carriers have been removed from the PPD, but only that the minority carrier concentration is negligible with respect to the impurity concentration [2]. In particular, residual electrons can be injected in the PPD due to thermionic emission of carriers [8] from the n+ regions

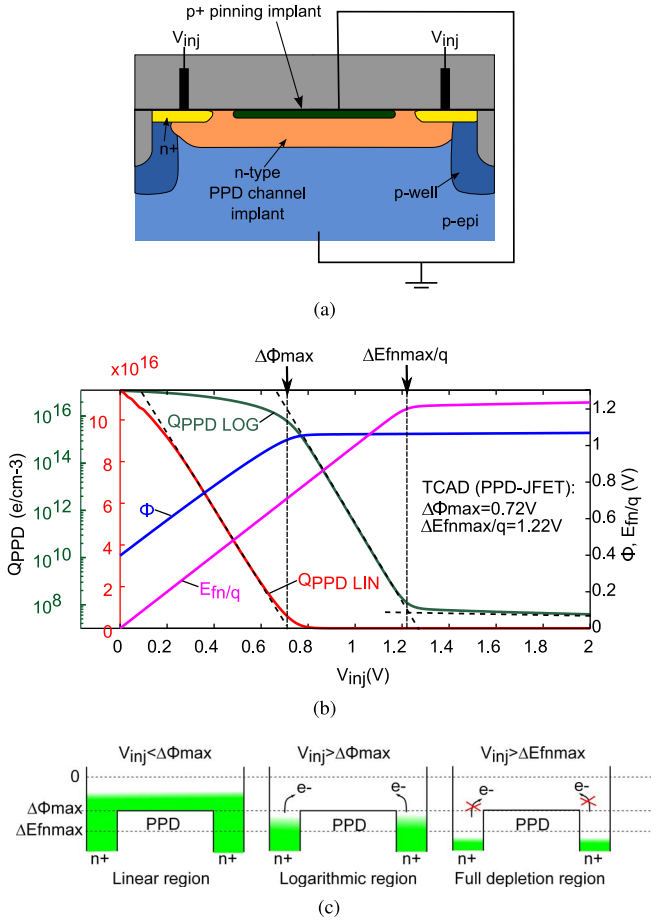

FIGURE 2. **(a) Cross section of the simulated PPD-JFET structure. The device is a 3D partially pinned PPD biased by means of two n+implants located at both side of the PPD channel, with $W_{JFET} = 2\mu m$ and $L_{JFET} = 10\mu m$. (b) PPD maximum electrostatic potential Φ, maximum E_{fn} and maximum electron density Q_{PPD} (plotted in linear and logarithmic scales) as a function of the injection potential applied to the PPD by means of two n+ implants. Three main working regions can be identified: a linear region ($V_{inj} < \Delta\Phi_{max}$), a logarithmic region ($E_{fnmax} > V_{inj} > \Delta\Phi_{max}$) and a full depletion region($V_{inj} > E_{fnmax}$). The corresponding potential diagrams are schematized in (c).**

toward the PPD channel (or from the TG channel, in the case of a full PPD pixel). For $V_{inj} > \Delta\Phi_{max}$, as long as the PPD is not empty, E_{fn}/q still increases linearly with V_{inj} (E_{fn} comes closer to the conduction band [2]). Since thermionic emission is an exponential function of the electrostatic barrier seen by electrons, in this region Q_{PPD} is an exponential function of V_{inj}. Eventually, thermionic emission becomes negligible and the PPD becomes empty of minority carriers. This point corresponds to $V_{inj} = \Delta E_{fnmax}/q$ on the simulated characteristic (Q_{PPD} and E_{fn} plateaus). A schematic representation of the simulated injection regimes is shown in Fig. 2c.

As a comparison, figure 3 shows the TCAD simulation of the maximum PPD electrostatic potential Φ, the maximum electron quasi-Fermi level E_{fn} and the maximum electron density Q_{PPD} (plotted in linear and logarithmic scales) as a function of the injection potential (V_{inj}) applied to the FD of a 3D PPD pixel structure (with the TG on and biased at 3.3V).

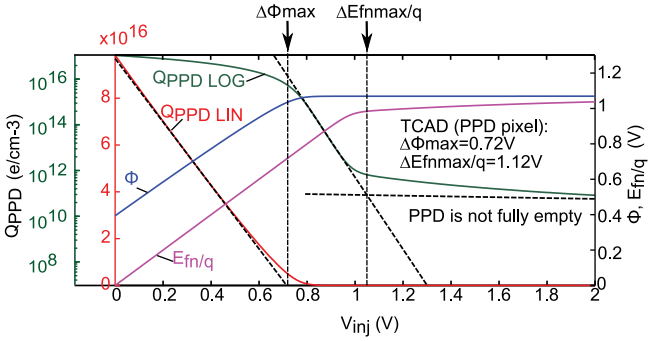

FIGURE 3. **PPD maximum electrostatic potential Φ, maximum E_{fn} and maximum electron density Q_{PPD} (plotted in linear and logarithmic scales) as a function of the injection potential applied to the FD of a PPD pixel with the TG on. The photodiode is a square $2.5\mu m \times 2.5\mu m$ PPD. The TG is $2.5\mu m$ large and $0.7\mu m$ long. Both the FD and the TG are biased at 3.3V.**

By comparing Fig. 3 to Fig. 2b, it can be observed that very similar $\Delta\Phi$max (here about 0.72V) can be estimated by simulating a PPD pixel and a PPD-JFET structure. However, it can also be observed that in the simulated PPD pixel all charges cannot be successfully extracted from the PPD. This can be explained by the presence of a residual potential barrier at the PPD TG interface due to a non perfect tuning of the doping implants profiles and overlaps [9], [10]. As a result, the $\Delta E_{fnmax}/q$ estimated in Fig. 3 does not correspond to a fully empty condition. Because of the dependence of the simulation results on the TG characteristics and on the applied biasing voltages, the simulation of the simpler symmetrically biased PPD-JFET structure is probably to be preferred for the optimization of the PPD doping profiles or when the detailed technological characteristics of the TG are unknown.

B. DEFINITION

Based on the TCAD simulations, it can be inferred that defining the pinning voltage as $\Delta E_{fnmax}/q$ is suitable when referring to the condition at which all charges have been removed from the PPD. In particular, $\Delta E_{fnmax}/q$ corresponds to the TG channel potential that must be applied to completely empty the PPD. However, due to the presence of design traps [9], such as a potential barrier or a potential pocket, which prevent the transfer of electrons from the PPD to the FD, this parameter is strongly affected by the design of the TG. Therefore $\Delta E_{fnmax}/q$ does not truly represents a "PPD parameter". Note also that if we assume that the PPD is "empty" when the PPD charge is about (or below) $1e^-$, the value of $\Delta E_{fnmax}/q$ (which is a function of the electron density in the PPD), will vary depending on the PPD size since the larger is the PPD, the lower is the charge density corresponding to the condition when $1e^-$ is left in the PPD.

On the other hand $\Delta\Phi_{max}$ mainly depends on the PPD design (geometry and doping profiles) and on the working temperature [3]. In particular, on the condition that the PPD width and length are large enough to neglect geometrical modulation effects [11], $\Delta\Phi_{max}$ does not depend on the

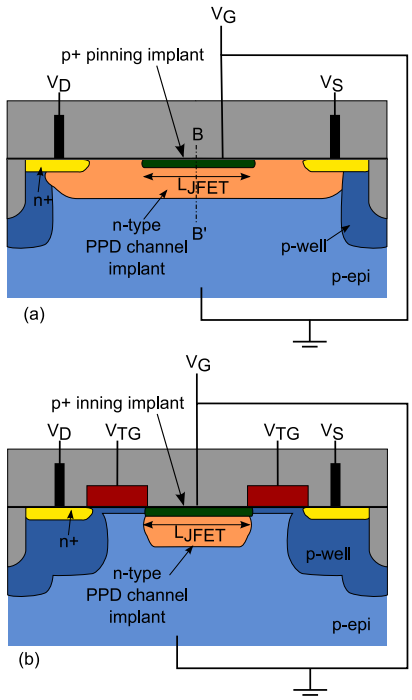

FIGURE 4. **Schematic drawing of a PPD-JFET structure (a) and of a TG-PPD-JFET structure (b), both implemented with typical PPD implants. V_D and V_S are the biasing voltages applied to the source and drain of the JFETs, respectively. V_{TG} is the biasing voltage applied to the TG of TG-PPD-JFET.**

PPD surface. Secondly, this parameter corresponds to the PPD potential floor, which can be a useful reference level to adjust the TG and FD doping profiles and biasing voltages to ensure an optimum charge transfer. Furthermore, as discussed in Section III, most of the existing pinning voltage estimation methods allow measurement of $\Delta\Phi_{max}$ and not of $\Delta E_{fnmax}/q$. Based on these considerations, in the following, V_{pin} has been defined as $\Delta\Phi_{max}$.

III. REVIEW OF THE MAIN PINNING VOLTAGE ESTIMATION METHODS

Pinning voltage measurements are often used in the industry to monitor production lines and for the optimization and development of technological processes. As none of the existing V_{pin} estimation methods has yet been officially identified as a "golden standard", each manufacturer measures the pinning voltage with custom developed techniques. In particular, in the CIS community, V_{pin} is estimated based on:

1) Electrical measurements performed on isolated test structures or on test structures arrays. These methods can be divided into:
   - JFET-based extraction methods [12]–[14], where V_{pin} is extracted as the pinch-off voltage V_p [6] of JFET test structures implemented with typical PPD implants (such as the ones in Fig.4a and Fig.4b).
   - Capacitance measurements [15].
2) In-pixel measurements [7], [16]–[18], where V_{pin} is measured directly on full PPD pixels arrays.

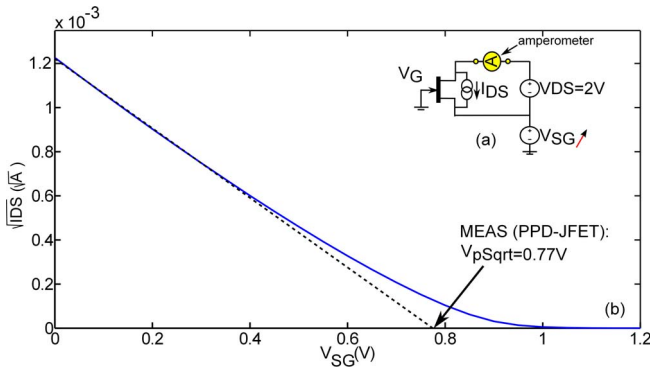

FIGURE 5. **(a) Equivalent circuit of the test set-up used in the Sqrt. method [12]. (b) Square root of the drain to source current (I_{DS}) as a function of the gate to source biasing voltage V_{SG} measured on a PPD-JFET structure (square root characteristic). A constant biasing voltage $V_{DS} = 2$ V is applied between drain and source. The pinch-off voltage V_P of the JFET is extracted as the x-intercept of the tangent to $\sqrt{I_{DS}}$ at small V_{SG} values. The tested device is a PPD-JFET (foundry A) with $\frac{W_{JFET}}{L_{JFET}} = \frac{2\,\mu m}{20\,\mu m}$.**

A. DEVICES UNDER TEST

All the tested devices have been designed in commercially available 0.18 μm PPD CIS technologies. For practical reasons, the tested PPD-JFET structures have been designed on two different foundries, which will be referred to as foundry A and foundry B. The experimental data presented is Section III.B.5 have been obtained on a third PPD technology and are a courtesy of Lahav Assaf, from TowerJazz. When known, the geometrical details and the dimensions of the tested JFET structures are specified in the different sections. In-pixel measurements have been performed on a 4T 64 × 128, 7 μm-pitch, pixels array (designed in foundry A) with a square 2.5 μm × 2.5 μm PPD, a long TG and a long FD (both 2.5 μm wide) on one side. The TG is 0.7 μm wide. The charge-to-voltage (CVF) conversion factor is about 20 $\mu V/e^-$.

B. TEST STRUCTURE METHODS

Different approaches, based on very different physical principles, are used today to estimate V_{pin} on isolated test structures. This section discusses the physical principle of some of the most commonly used methods.

B.1. THE SQUARE ROOT METHOD

The square root (Sqrt.) method [12] is a well established JFET pinch-off voltage (V_p) characterization technique. The corresponding experimental set-up is shown in Fig. 5a. The method is based on the resolution of JFET equations at saturation [6]:

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{SG}}{V_p}\right)^2 \tag{2}$$

where V_{SG} is the source-to-gate biasing voltage (with V_G the substrate biasing voltage and $V_{SG} > 0$), I_{DS} is the saturation drain-to-source current, and I_{DSS} is the I_{DS} saturation current measured for $V_{SG} = 0$. Note that for the purpose of clarity,

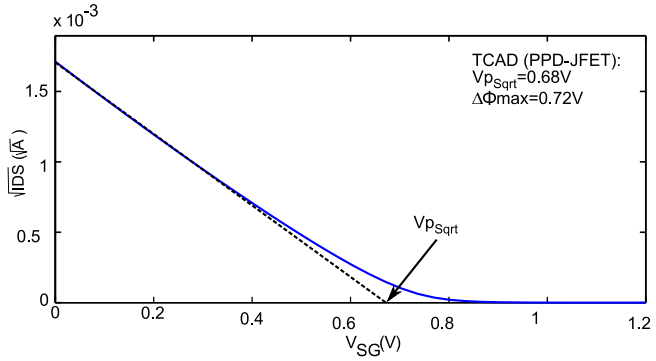

FIGURE 6. Square root of the drain to source current (I_{DS}) as a function of the gate to source biasing voltage V_{SG} simulated for the same JFET structure as in Fig. 2 ($W_{JFET} = 2\mu m$ and $L_{JFET} = 10\mu m$).

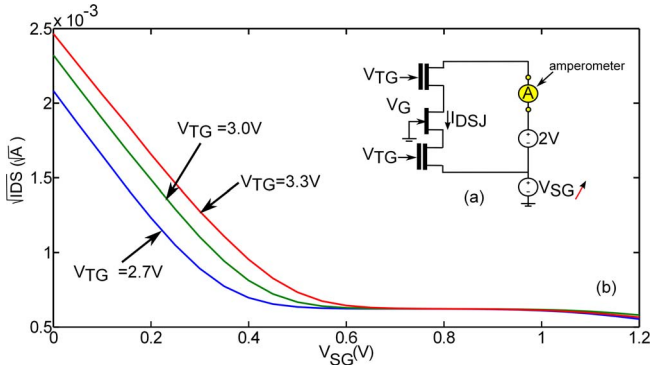

FIGURE 7. (a) Equivalent circuit of the experimental set-up when measuring the pinning voltage on a TG-PPD-JFET structure with the Sqrt. method. (b) Square root of the drain to source current I_{DS} as a function of the gate to source voltage (V_{SG}) measured on a TG-PPD-JFET (foundry A) for different TG biasing potentials (V_{TG}). The TG and the JFET dimensions are $\frac{W_{TG}}{L_{TG}} = \frac{10\,\mu m}{0.7\,\mu m}$ and $\frac{W_{JFET}}{L_{JFET}} = \frac{10\,\mu m}{20\,\mu m}$, respectively. As can be observed, I_{DS} always depends on V_{TG}, therefore no meaningful V_{pin} can be extracted on this type of devices.

V_p is defined here as a positive quantity (whereas in [6] it is defined as a negative quantity). Figure 5b shows the experimental extraction of V_p from the square root characteristic obtained on a PPD-JFET (Fig. 4a). V_p is estimated as the intersection of the tangent to the square root characteristic with the x-axis. The linear fitting is performed at small V_{SG} biasing voltages (of the order of a hundred mV), which correspond to high current values (here of the order of a few μA), therefore this measurement should not be affected by the current resolution of the set-up (here about 100 fA). Note however, that since a large voltage (2 V) is applied between source and drain, the Sqrt. method should be used only on long PPD-JFET structures to avoid the drain potential affecting the potential at the source (equivalent of short channel effects in MOS transistor [8]). This can be considered as a strong limitation of this technique, as designers aim at estimating V_{pin} in structures which are as close as possible to real pixels. However, since standard JFET structures usually include n+ implants at both sides of the PPD (to implement the source and the drain of the JFET), none of the JFET-based methods discussed in this work truly allows to observe the effect of the PPD length on V_{pin}. Therefore only V_{pin} variations with the PPD width [11] can be monitored with PPD-JFET devices. Figure 6 shows a square root characteristic simulated in TCAD. The PPD-JFET structure is the same as the one simulated Fig. 2. It is important to note that TCAD simulations have not been calibrated to match experimental data, therefore absolute V_{pin} values should not be compared. As it can be observed, the pinning voltage estimated with the Sqrt. method gives a good estimate of the $\Delta\Phi_{max}$ value of the simulated structure (here $\Delta\Phi_{max} \approx 0.72$V and $V_p \approx 0.68$V) and can thus be considered as a suitable technique for the estimation of the absolute value of V_{pin}.

To respect design rules and to approach as much as possible in-pixel conditions, PPD-JFET isolated structures can be designed with a TG on both source and drain sides[1] (Fig. 4b). These structures are referred to here as TG PPD-JFET structures. Figure 7 shows the square root characteristic measured on a TG-PPD-JFET. As can be observed, the measured current varies significantly with the TG biasing voltage. This behaviour is due to the fact that the JFET is in series with two TGs, which are often designed with an asymmetrical channel doping (to avoid charge spill back [19] toward the PPD) and present a strong channel resistance when electrons move from the FD toward the PPD (maximum currents of the order of a few μA have been measured on TG test transistors with $\frac{W_{TG}}{L_{TG}} = \frac{10\,\mu m}{0.7\,\mu m}$). This means that depending on the tuning of the technology and of the current gains (i.e., of the W/L ratios) of both the TG and the JFET, the measured output current can be either limited by the JFET or the TG. In the latter case, the estimated V_{pin} values are meaningless. Therefore these structures are not recommended for the estimation of the pinning voltage.

B.2. THE FLOATING SOURCE METHOD

The floating source (FS) method [14] consists in leaving the source of a PPD-JFET structure floating and in monitoring its source potential V_S as a function of the biasing voltage applied to the drain (V_D). During the measurement, a current I_{out} is forced at the source.[2] The equivalent circuit of the test set-up is shown in Fig. 8a. This method is based on the assumption of a "on-off" behaviour of the JFET. In particular it is assumed that, as long as $V_{SG} < V_p$, the JFET is "on" and V_S follows V_D (since the capacitance of the floating source is charged by a current $I_{DS} > 0$). V_S eventually stops following V_D. Since the JFET is considered to be "off" ($I_{DS} = 0$) at pinch-off (i.e., when $V_{SG} \geq V_p$), V_p is extracted as the V_S potential at saturation.

1. Or with only one TG on one side. In this case the PD is partially pinned.

2. Note that if I_{out} is too small, the effective output current will be the leakage current of the experimental set-up.

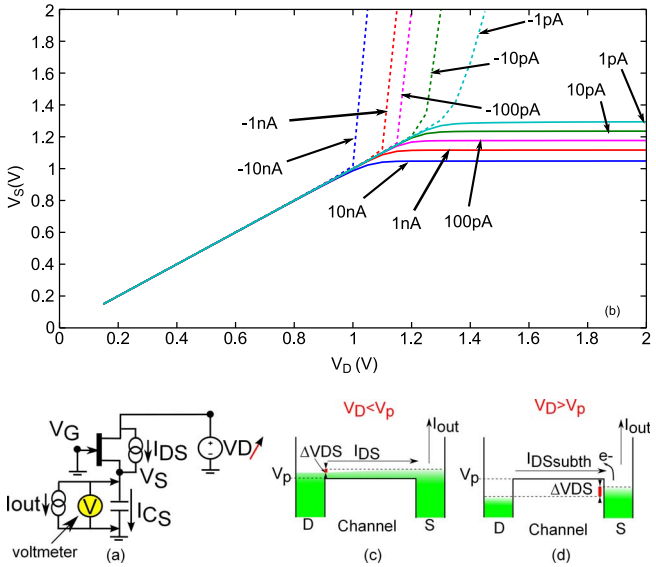

FIGURE 8. **(a) Equivalent circuit of the test set-up for the floating source (FS) extraction method discussed in [14]. I_{out} can be due to parasitic leakage currents or can be forced during the measurement. (b) Source potential (V_S) as a function of the drain potential (V_D) measured on a PPD-JFET structure for different I_{out} values with the FS method [14]. As can be observed, depending on I_{out}, an arbitrary V_P can be estimated with this method. As illustrated by the schematic diagrams in (c) and (d), if $V_D < V_P$, the current charging the source capacitance (I_C) becomes zero when $I_{JFET} = I_{out}$, whereas if $V_D > V_P$ the JFET is in sub-threshold conduction and the measured V_S depends on I_{out} and on the hold time t_H between two V_D steps. The tested device is a PPD-JFET with $\frac{W_{JFET}}{L_{JFET}} = \frac{10\ \mu m}{20\ \mu m}$ (foundry B).**

Figure 8b shows the V_S potential as a function of the V_D potential measured for different I_{out} values. As can be observed, arbitrary V_p values can be estimated with this method depending on I_{out}. This behaviour is due to the fact that, in practice, I_{DS} is never zero, as there is always a sub-threshold current flowing in the JFET due to the net thermionic emission of electrons from the source toward the channel [20]. As a result, V_S will follow the V_D potential even after pinch-off. In particular:

- For $V_D < V_p$ (Fig. 8c), the current charging the source capacitance (I_C) becomes zero when $I_{JFET} = I_{out}$.
- For $V_D > V_p$ (Fig. 8d), the JFET is in sub-threshold conduction and the measured V_S depends on I_{out} (and on the hold time before the sampling of the V_S value).

It should also be noted that since the saturation of the V_S curve depends on a current balance (and therefore on the amount of current flowing in the JFET), different V_p values are to be expected for two devices with the same width and different lengths (whereas they should have the same V_p if L_{JFET} was larger than a few μm).

B.3. CURRENT METHOD

In the extraction method used in [13], a small voltage difference is applied between V_D and V_S ($V_{DS} = 10$ mV), and I_{DS} is monitored while the V_D potential is increased with respect to V_G. V_p is estimated as the V_S potential at which the I_{DS} current reaches a certain percentage (for example 1%) of the

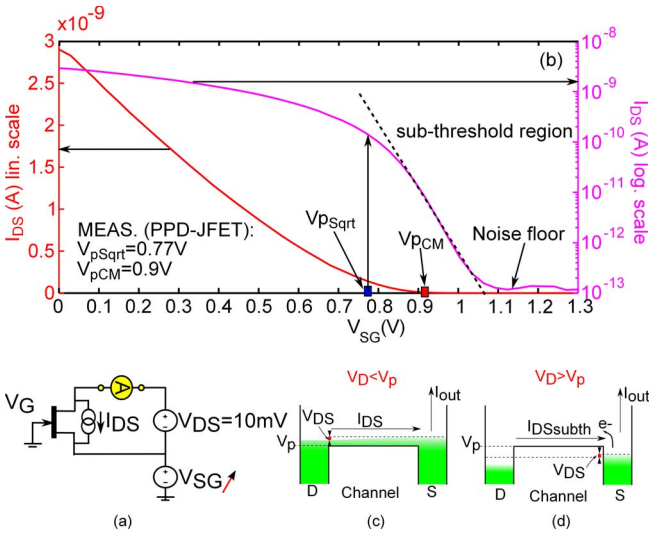

FIGURE 9. **(a) Equivalent circuit of the test set-up discussed in [13]. (b) Drain to source current I_{DS} characteristic measured as a function of the source to gate voltage V_{SG}, for $V_{DS} = 10$ mV. The tested PPD-JFET is the same as the one tested in Fig. 5. In [13] the pinch-off voltage (indicated here as V_{pCM}) is estimated as the V_{SG} potential at which the I_{DS} current is zero. V_{pSqrt} corresponds to the pinning voltage estimated with the Sqrt. method in Fig. 7. The schematic potential diagram for $V_D < V_P$ and $V_D > V_P$ are shown in (c) and (d), respectively.**

initial current value [21]. The equivalent circuit of the test set-up is shown in Fig. 9a. This method is referred to here as the Current (Cu.) method. Unlike the Sqrt. method, the Cu. method is not based on the resolution of JFET equations and like the FS method, it is based on the assumption of an "on-off" behaviour of the JFET. By looking at the I_{DS} characteristic in Fig. 9b in logarithmic scale, we can see that the zero current condition cannot be reached (as the minimum measurable current corresponds to the accuracy of the test set-up). Furthermore, since the characteristic is non-linear, the "zero" value cannot be estimated by a linear fit of the curve (while it is the case for the Sqrt. method). It can be observed that the Cu. method provides an overestimation of V_p with respect to the one estimated with the Sqrt. method (indicated as V_{psqrt} in the figure). In addition, it can also be observed that the biasing condition at which $V_{SG} = V_{psqrt}$ roughly corresponds to the transition of the I_{DS} characteristic into the sub-threshold region. This transition corresponds to the moment when the conduction between source and drain starts to be dominated by the thermionic emission of electrons from the source toward the JFET channel (i.e., when V_{PPD} reaches V_{pin}). Therefore, the experimental set-up proposed in [13] is suitable for the estimation of V_p, as long as the pinch-off voltage is estimated as the potential at which the I-V characteristic enters the logarithmic region and not when the current becomes "zero". This approach does not provide an accurate and unique V_p value (as there is no net transition between the two working regions), however it has the advantage, with respect to the Sqrt. method of being compatible with shorter JFET lengths (given the small applied V_{DS}) and to be based on a "symmetrical biasing" of the JFET.

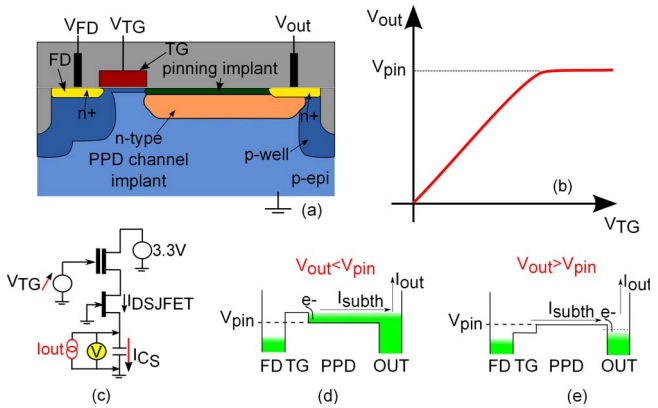

FIGURE 10. (a) Schematic drawing of the "rectangle" structure used for the estimation of V_{pin}. (b) Method working principle: V_{FD} is biased at 3.3 V and V_{pin} is retrieved as the V_{out} at saturation (as it is assumed that no current flows in the structure once $V_{out} > V_{pin}$). (c) Schematic circuit of the test set-up of the rectangle method. A current I_{out} is forced at the output. In practice, there is always a current flowing in the structure due to the thermionic emission of carriers across the potential barrier at the PPD-TG interface (d) or the barrier between the n+ output electrode and the PPD (e). As a result, arbitrary pinning voltage values can be obtained depending on the chosen I_{out}.

B.4. THE "RECTANGLE" METHOD

The "rectangle" method [21] is a pinning voltage estimation technique based on the "rectangle" structure shown in Fig. 10a. The equivalent circuit of the test set-up and a schematic explanation of the method working principle are also illustrated in Fig. 10. The FD is biased at 3.3 V, whereas the PPD is left floating, and the output potential V_{out} is monitored as a function of the TG biasing voltage. A constant current I_{out} is injected in the PD. The pinning voltage is extracted as the V_{out} potential at saturation. No experimental data are available for the rectangle method. However, like the FS method, this method is also based on the assumption that measured output voltage corresponds to the PPD potential and that once the PPD potential has reached V_{pin}, no more current can flow in the structure. The same considerations drawn for the FS method can be extended to the "rectangle" method. In particular, as shown in Fig. 10e, saturation is reached only when the sub-threshold current I_{subth} of the device formed by the series of the TG and of the PPD JFET becomes equal to I_{out}. Therefore V_{out} can become larger than V_{pin}. With respect to the floating diffusion method, results obtained on "rectangle" devices can be even harder to interpret, as measurements can be significantly affected by the design of the TG. Therefore this method is not suitable for the estimation of V_{pin}.

B.5. C-V METHOD

Another approach which is used in the industry to measure the pinning voltage is based on C-V (capacitance-voltage) measurements on large arrays of partially pinned photodiodes [15], [21] such as the one shown in Fig. 11a.[3]

3. A TG can also be included in the structure between the PPD and the biasing electrode.

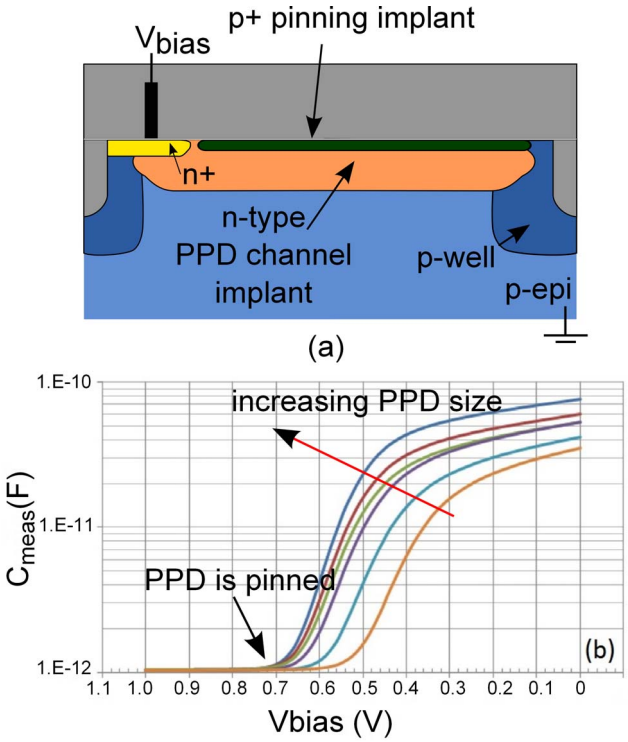

FIGURE 11. (a) Cross-section of a partially pinned PD structure used for the estimation of V_{pin} based on C-V measurements. The structure can also include a TG. (b) C-V measurements obtained on arrays of partially pinned photodiodes with increasing PPD areas. V_{pin} is extracted as the biasing potential at which C_{meas} reaches a plateau [15]. These data are a courtesy of A. Lahav, from TowerJazz.

The method consists in measuring the variation of the capacitance C_{meas} of a partially pinned diode as a function of the applied biasing voltage V_{bias}. The working principle is as following: as V_{bias} is increased, both the PPD charge and C_{PPD} decrease; when the PPD potential reaches its maximum value (V_{pin}), C_{PPD} becomes zero and C_{meas} reaches its minimum value. Therefore V_{pin} is extracted as the biasing voltage at which C_{meas} reaches a plateau. An example of experimental measurements obtained for different PPD sizes is shown in Fig. 11b. With respect to JFET methods, this approach has the disadvantage of requiring large test-structure arrays (in order to reach a high enough output capacitance). Furthermore, like in the CM, the pinning voltage is retrieved from the saturation of a non linear characteristic, leading to large value uncertainties depending on when one estimates that the curve has "reached the plateau". Finally, experimental measurements can be significantly affected by the numerous parasitic capacitances involved in such set-up.

C. IN-PIXEL METHODS

The in-pixel V_{pin} extraction method has been proposed by Tan *et al.* [16], then further discussed in [7], [17], and [18]. The method consists in monitoring the electrical injection of carriers in the PPD as a function of the injection potential V_{inj} applied to the FD (by modulating V_{DDRST} while

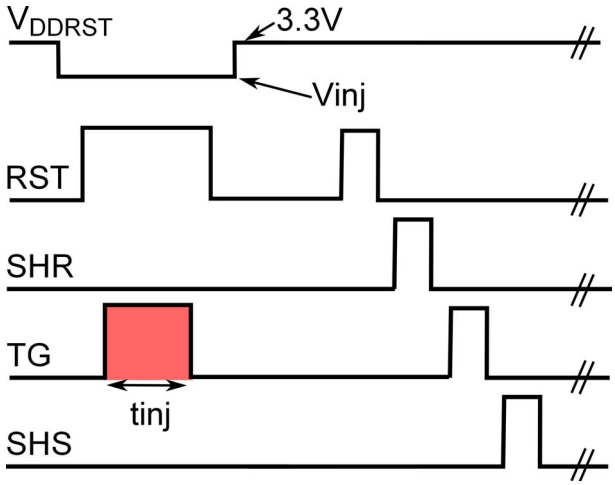

FIGURE 12. Timing diagram for the in-pixel estimation of the pinning voltage (reproduced from [7]). SHR and SHS are the signal for the sampling of the reference and of the signal, respectively. The injection time is 40μs.

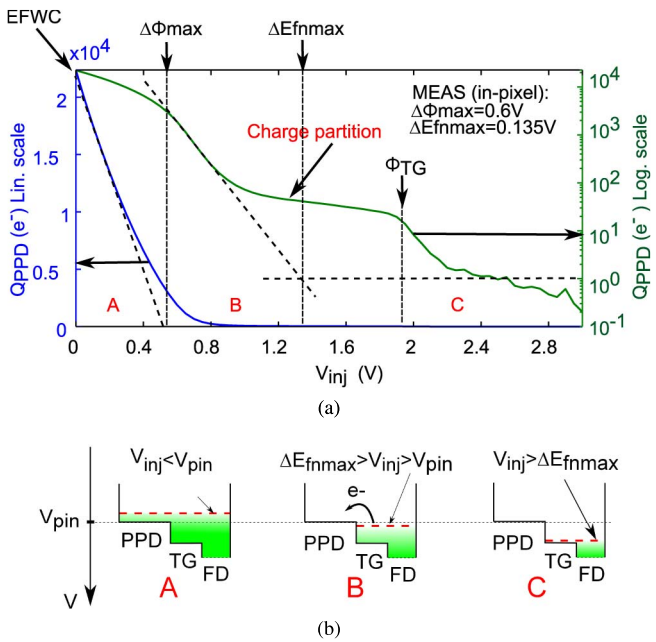

FIGURE 13. (a) Pinning voltage characteristic plotted in linear and logarithmic scales: injected charge Q_{inj} vs. injection potential V_{inj} measured in the dark at $T = 60$ °C. (b) Schematic potential diagram in regions A, B and C. The curve has been measured on a 64 × 128 4.5 μm-pitch PPD CIS pixel-array. The PPD size is 2.5 μm × 2.5 μm. The charge to voltage conversion factor is about 20 μV/e⁻.

the TG and RST transistors are on). The timing diagram is shown in Fig. 12. After the injection phase, the TG is turned off, the FD is reset (to sample the reference), then the TG is turned on again to transfer the injected charge back to the FD and the signal is sampled.

Figure 13a shows an example of an experimental pinning voltage characteristic (output charge Q_{out} as a function of V_{inj}). V_{pin} is estimated as the V_{inj} potential above which direct charge injection becomes zero. Whereas in [16], this potential is retrieved by means of a linear fit of the pinning voltage characteristic at small V_{inj} (linear method), the integral method proposed in [7] takes into account the integration of charges on the PPD capacitance. As was expected from the simulation in Fig. 2 and Fig. 3, the PPD is far from being empty when $V_{inj} = V_{pin}$. In particular, by looking at the pinning voltage characteristic in logarithmic scale, it can be observed that the PPD still contains a few percent of the initial charge.

Four main working regions can be identified on the characteristic:

- In region A ($V_{inj} < V_{pin}$) charges are directly injected in the PPD and Q_{out} is a linear function of V_{inj}. This is due to the fact that, as discussed in [7], in this region the capacitance is a very weak function of the PPD potential (and can therefore be approximated as constant). The PPD charge measured at $V_{inj} = 0$ corresponds to the Equilibrium Full Well capacity (EFWC) [3].
- In region B ($\Delta E_{fnmax}/q > V_{inj} > V_{pin}$) charges are injected in the PPD by thermionic emission. Since the thermionic emission is an exponential function of the potential barrier seen by electrons, the pinning voltage characteristic is a logarithmic function of V_{inj}.
- In region C ($V_{inj} > \Delta E_{fnmax}/q$) the thermionic emission is negligible ($Q_{out} \approx 1e^-$), thus the PPD can be considered empty. $\Delta E_{fnmax}/q$ can be estimated by finding the intercept between the charge plateau (here $\approx 1e^-$) and the fit of the logarithmic region.
- A forth working region, corresponding to the charge partition regime [7] can be identified on the characteristic. Whereas the other three regions mainly depend on the injection phase, charge partition is due to the partition of charge (that was located in the TG channel during charge injection) between the FD and the PPD when the TG is turned off to sample the reference.

Schematic potential drawings of regions A, B and C are shown in Fig. 13b. As indicated in Fig. 13a, different parameters can be estimated from the pinning voltage characteristic: V_{pin} (i.e., $\Delta\Phi_{max}$), $\Delta E_{fnmax}/q$ (which corresponds to the minimum potential that must be applied to a well adjacent to the PPD to completely empty the latter from minority carriers, i.e., to the minimum TG channel to ensure a good charge transfer efficiency), the Equilibrium Full Well Capacity (EFWC) [3] and the TG channel potential Φ_{TG} [7]). Note however, that V_{pin} values estimated with this method should be handled with care, since if the pixel presents a low CTE or if the experimental conditions and the timing diagram are not set carefully, wrong V_{pin} might be estimated [7].

IV. CONCLUSION

This work was dedicated to the definition of the pinning voltage and to a comparative study of different methods that are used in the CIS community to estimate the pinning voltage. It has been shown that the definitions that are used in the literature to indicate the pinning voltage ($\Delta\Phi_{max}$ and ΔE_{fnmax})

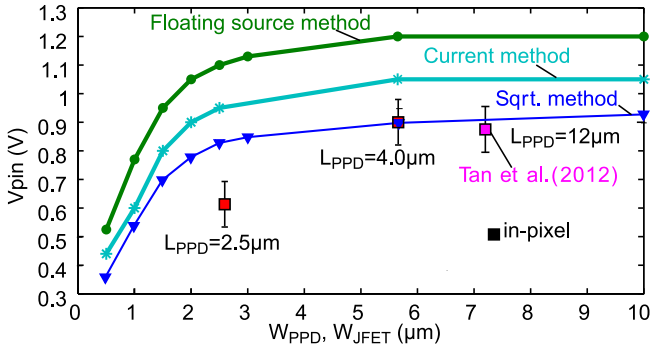

FIGURE 14. **V_{pin} as a function of the PPD-JFET channel width W_{JFET} (or PPD width W_{PPD}) extracted with the in-pixel method[16], with the floating source method (I_{out} = 1 pA), with the Cu. method and with the Sqrt. method. All the tested PPD-JFETs have a channel length L_{JFET} = 20 µm and have been designed in foundry A.**

correspond to two very different physical parameters, which can differ by several hundreds of mV:

- $\Delta\Phi_{max}$ corresponds to the maximum PPD electrostatic potential, and is the pinning voltage definition which should be used to estimate the PPD EFWC [3].
- ΔE_{fnmax} represents the minimum TG channel potential that must be induced to fully empty the PPD of minority carriers (neglecting charge partition phenomena and the effect of the potential barrier between the PPD and the TG).

In this study, V_{pin} was defined as $\Delta\Phi_{max}$.

Fig. 14 presents the V_{pin} values estimated with the floating source method, the current method and the square root method for different PPD-JFET lengths. The figure also shows the V_{pin} values estimated with the in-pixel methods on PPD CIS arrays with different photodiode sizes. As expected, in-pixel measurements are in good agreement with the Sqrt. method, as they both provide an absolute value of the pinning voltage (therefore of $\Delta\Phi_{max}$). The lower in-pixel V_{pin} value extracted at $W_{PPD} = 2.5$ µm can be explained by additional 3D effects [11], [13] due to the combination of a small W_{PPD} and a small L_{PPD}. It can also be observed that, even if the FS method and the Cu. method do not provide an absolute value of the pinning voltage (100 mV-300 mV higher here), they still allow to observe relative pinning voltage variations resulting from geometrical variations.

Test structure methods have the advantage of being based on simple I-V or C-V measurements, that can be performed by wafer probe. They also allow easy monitoring of the effect of process variations and testing of many different PPD widths. However, because of the presence of n+ implants on both sides of the PPD channel, JFET measurements do not allow to observe V_{pin} variations with L_{PPD}. On the other hand, the in-pixel approach gives less freedom in terms of the number of variations that can be tested but provides an estimate of V_{pin} in a real in-pixel environment, allowing observation of both the effect of the width and length of the PPD. In addition, other PPD CIS parameters, such as $\Delta E_{fnmax}/q$, the EFWC and the TG channel potential [7] can be estimated from the pinning voltage characteristic. For these reasons, the two approaches should be considered complementary.

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