Received 20 July 2015; revised 25 September 2015; accepted 13 November 2015. Date of publication 25 November 2015; date of current version 18 December 2015. The review of this paper was arranged by Editor M. Anwar.

Digital Object Identifier 10.1109/JEDS.2015.2503701

High-Current Submicrometer Tri-Gate GaN High-Electron Mobility Transistors With Binary and Quaternary Barriers

ERDIN TURE[1], PETER BRÜCKNER[1], BIRTE-JULIA GODEJOHANN[1], ROLF AIDAM[1], MOHAMED ALSHAREF[2], RALF GRANZNER[2], FRANK SCHWIERZ[2] (Senior Member, IEEE), RÜDIGER QUAY[1] (Senior Member, IEEE), AND OLIVER AMBACHER[1]

1 Fraunhofer Institute for Applied Solid-State Physics, Freiburg D-79108, Germany
2 Department of Fachgebiet Festkörperelektronik, Technische Universität Ilmenau, Ilmenau D-98684, Germany

CORRESPONDING AUTHOR: E. TURE (e-mail: erdin.ture@iaf-extern.fraunhofer.de)

ABSTRACT Through implementation of the 3-D tri-gate topology, GaN-based high-electron mobility transistors (HEMTs) have been fabricated and high-frequency performances as well as the short-channel effects are investigated. The designed tri-gate transistors are highly-scaled having 100 nm of gate length, which introduces the condition of a short channel. It is demonstrated that higher sub-threshold slopes, reduced drain-induced barrier lowering and better overall off-state performances have been achieved by the nano-channel tri-gate HEMTs with an AlGaN barrier. A lattice-matched InAlGaN barrier with the help of the fin-shaped nano-channels provide improved gate control, increasing current densities, and transconductance g_m. In a direct comparison, very high drain current densities (~3.8 A/mm) and g_m (~550 mS/mm) have further been obtained by employing a pure AlN barrier.

INDEX TERMS High-electron mobility transistor (HEMT), fin-shaped field-effect transistor (FinFET), Gallium nitride, short channel.

I. INTRODUCTION

The desirable properties of GaN-based high-electron-mobility transistors (HEMTs) have enabled development of high-performance circuits and devices in RF- and power applications. Recent studies [1], [2] have reported very high device speeds through extensive scaling as well as reduced short-channel effects (SCE) and parasitics. Nevertheless, the demonstrated device performances are still unable to match the predicted values regarding GaN material properties since some of the critical problems remain unresolved. One of the issues is the sub-optimal saturation current density of GaN devices as the reported results in the literature are below the theoretical figures [3]. Another issue which needs to be addressed is the undesired strong bias-dependence of the intrinsic device parameters, resulting in non-linear SCE and cut-off frequencies [4]. With the increase in the gate- or drain-bias voltages, transconductance (g_m) and current-gain cut-off frequency (f_T) decrease significantly after reaching respective peak values which becomes critical in large-signal operation.

In this letter, we adopt the lattice-matched InAlGaN and AlN-barrier layers [5]–[8] to improve the saturation drain current density and transconductance of Tri-gate [9]–[16] HEMTs, compared to the AlGaN. It has already been determined in an earlier study [5] that the use of quaternary layers bear great potential to enhance the performance of GaN HEMTs, having reached carrier mobilities over 1600 cm^2/Vs. Experimental results in this work demonstrate very linear RF- and superior DC-performance of the proposed FinFETs with record current densities of ~3.8 A/mm, which is more than double the value of conventional planar FETs.

II. DEVICE FABRICATION

The epitaxial growth of the hetero-structures is performed by using plasma-assisted molecular beam epitaxy (PA-MBE) on 4H-SiC substrates with 3-inch diameter. The epitaxial

2168-6734 © 2015 IEEE. Translations and content mining are permitted for academic research only.
Personal use is also permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

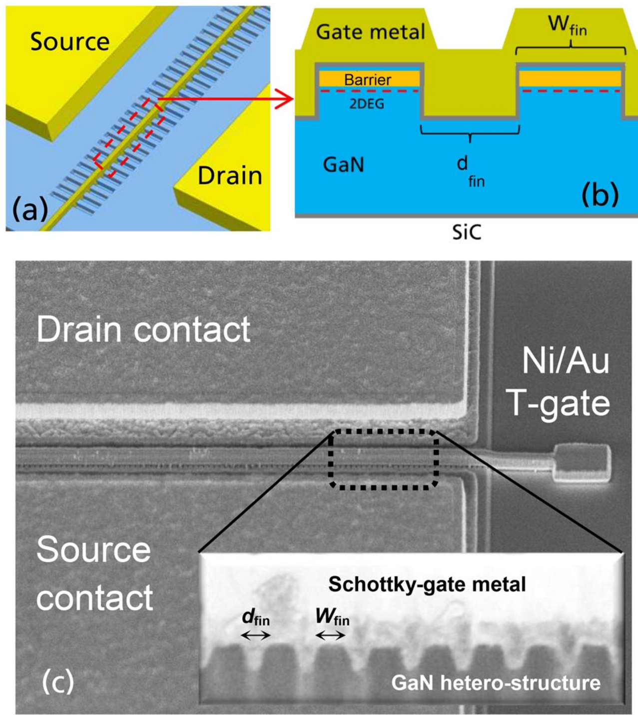

FIGURE 1. Perspective illustration (a), cross-sectional illustration (b), and quasi-top-view SEM image of the fabricated Tri-gate HEMT structure and the cross-sectional SEM image (c) of the fin-shaped nano-channels indicated along underneath the Schottky-gate electrode in the bottom inset.

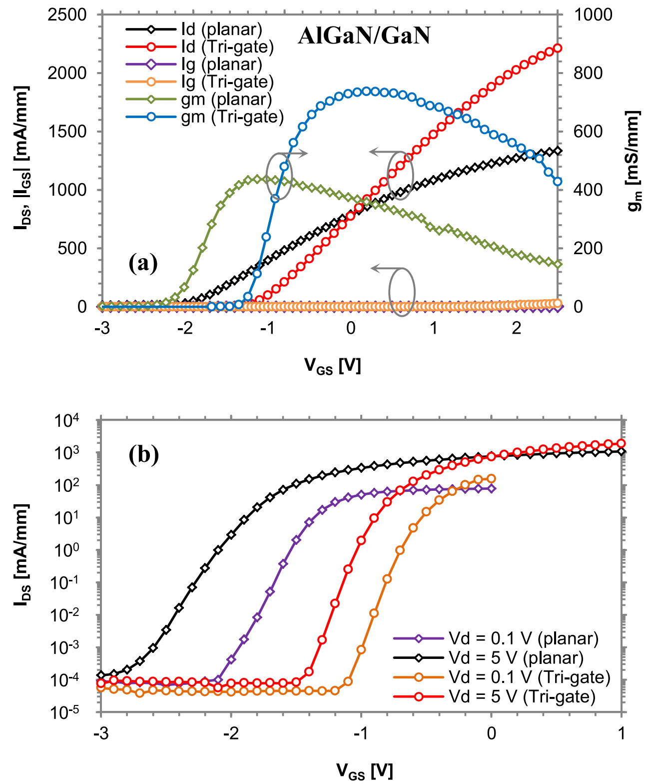

FIGURE 2. DC-transfer characteristics (a) at V_D = 5 V and sub-threshold current behavior (b) at drain bias voltages of V_D = 0.1 V and 5 V of the planar and Tri-gate AlGaN/GaN HEMTs.

structure of the conventional AlGaN/GaN wafer comprises a 120-nm AlN nucleation layer, 1.8-μm GaN buffer, 11-nm $Al_{0.32}Ga_{0.68}N$ barrier, and 2-nm GaN cap layer. Being one of the two lattice-matched epitaxy variations, the quaternary wafer consists of a 100 nm AlN nucleation layer, a 1.5 μm-thick GaN buffer, a 1.3 nm AlN spacer, a nearly lattice-matched 10 nm-thick $In_{0.1}Al_{0.55}Ga_{0.35}N$ barrier, and a 3 nm GaN cap layer. As for the latter variation, the binary wafer comprises a 4 nm-thick AlN single layer on top of the above-mentioned AlN nucleation and GaN buffer layers, as well as the same 3 nm GaN cap. Following the epitaxial growth, Ti/Al-based metal stacks are deposited and annealed to form ohmic contacts after an initial mesa isolation of the wafers. Electron beam lithography is used in order to define the 100 nm-long fin-shaped nano-channels, for which chlorine-based inductively-coupled plasma etching (Cl-ICP) is performed with a target etch depth of 50 nm. A 50 nm-thick Si_3N_4isolation layer is deposited by plasma-enhanced chemical vapor deposition (PECVD) whereas for the AlN/GaN FinFETs, an additional 20 nm Si_3N_4 layer is deposited covering the sidewalls of the fin-shaped channels (in this case the Schottky contact is only allowed at the top-surface of AlN/GaN fins). The Si_3N_4passivation layer at the gated area is then etched away where a second electron beam is employed to define the Ni/Pt/Au-based Schottky-gate electrode with L_g = 100 nm length, fully covering the fin-channels underneath. The devices are fully passivated by a final Si_3N_4 layer. The final structure of the proposed Tri-gate HEMTs with fin-channel patterns under the gate electrode and the cross-sectional scanning electron microscope (SEM) image of the gate profile can be depicted in Fig. 1. Both planar and Tri-gate devices exhibit the same metallurgical gate width of W_g = 100 μm, however, differ in total effective gate widths.

III. EXPERIMENTAL RESULTS AND DISCUSSION

Concerning the DC- and RF-measurements of the fabricated transistor devices, total gate width normalization is done with respect to the effective nano-channel width ($W_{eff} = n \times W_{fin}$, where n is the number of nano-channels and W_{fin} is the width of an individual fin-shaped nano-channel), which is the most widely accepted normalization method for Tri-gate HEMTs. The performance of conventional planar and Tri-gate FETs are compared on AlGaN/GaN wafers as well as two lattice-matched wafers with quaternary and binary hetero-structures, respectively.

A. AlGaN/GaN TRI-GATE HEMTs

The fabricated AlGaN/GaN FinFETs are comprised of n = 500 fin-shaped nano-channels with W_{fin} = 100 nm, accumulating a total effective gate width of W_{eff} = 50 μm, compared to $W_g = W_{eff}$ = 100 μm of the planar FETs on the same wafer. Hall measurements have determined 1300 cm^2/Vs of 2DEG mobility, 8×10^{12} cm^{-2} of carrier density and 450 Ω of sheet resistance. Fig. 2 reveals the measured

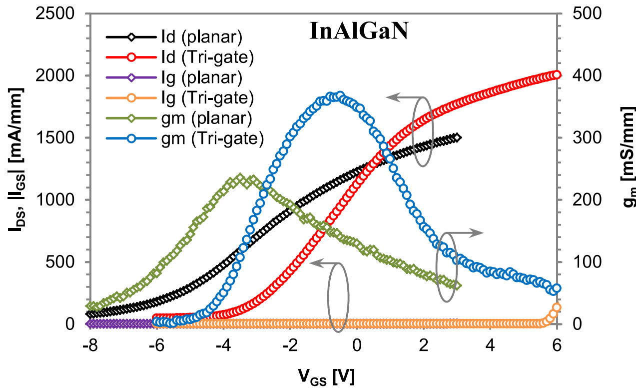

FIGURE 3. DC-transfer characteristics and transconductance of the planar and Tri-gate InAlGaN HEMTs at V_D = 20 V.

DC-transfer and sub-threshold characteristics of the planar and Tri-gate HEMTs. According to the results, Tri-gate devices reach 2.2 A/mm and 750 mS/mm of saturation current density (I_{Dsat}) and transconductance (g_m) respectively, compared to I_{Dsat} = 1.3 A/mm, and g_m = 450 mS/mm of the planar FETs. The fundamental reason behind the increase in the drain current density is assumed to be improved carrier transport mechanisms and therefore the saturated electron drift velocities with the help of uniform electric fields surrounding the 2DEG at the fins according to Tamura *et al.* [9]. Regarding the sub-threshold behavior depicted in Fig. 2-b, planar FETs result in diminished sub-threshold slopes of 150 mV/dec and 200 mV/dec at V_D = 0.1 V and 5 V respectively. It can be said that the planar devices are suffering from SCE due to the inadequate gate control only at the top of the channel. Tri-gates on the other hand provide better off-state performance with 75 mV/dec and 100 mV/dec of sub-threshold slopes at V_D = 0.1 V and 5 V respectively, as well as lower leakage currents even at high drain bias voltages. Furthermore, very low drain-induced barrier lowering (DIBL) of the FinFETs measured to be around 50 mV/V are also superior to 120 mV/V of the planars. Apart from the enhanced off- and on-state performance figures, FinFETs show a positive threshold voltage shift of ~1 V as predicted by the Tri-gate theory [9]–[13]. The investigation of the DC parameters points out that SCE are successfully suppressed by implementation of the nano-channel FinFETs.

B. InAlGaN TRI-GATE HEMTs

Similarly to the AlGaN/GaN devices, the InAlGaN FinFETs also exhibit a total effective gate width of W_{eff} = 50 μm with n = 500 and W_{fin} = 100 nm compared to W_g = W_{eff} = 100 μm of the planar FETs. 1350 cm^2/Vs of 2DEG mobility, 1.5×10^{13} cm^{-2} of carrier density and 310 Ω of sheet resistance have been achieved by Hall measurements. Fig. 3 reveals the measured DC-transfer characteristics of the planar and Tri-gate HEMTs. Accordingly, higher saturation current densities above 2 A/mm have been achieved by FinFETs, compared to the 1.5 A/mm of the planar FETs. The Tri-gate topology has once again shown improved and flatter g_m response with a peak value of 370 mS/mm, whereas the planar devices can only reach up to 230 mS/mm. It has to be noted that the epitaxial layer thicknesses of the lattice-matched structures have not been fully optimized yet and therefore the relatively low transconductance values are not comparable to the AlGaN/GaN wafer. On the other hand, high spontaneous polarization charges introduced by the InAlGaN barrier have resulted in a significant negative threshold-voltage-shift of the devices. Consequently, the obtained sub-optimal sub-threshold performance prevents a thorough SCE investigation, with leakage currents above 1 mA/mm being one of the prevailing issues in implementing lattice-matched hetero-structures and yet to be resolved with the help of further investigation.

In addition to the DC-performance analysis, small-signal S-parameter measurements of the devices up to 110 GHz have been conducted by using HP 8510XF vector network analyzer, followed by the extraction of intrinsic f_T parameters with the help of a 3-D transistor modeling method employing the state-space approach [17]. As mentioned earlier, the strongly bias-dependent nature of the dynamic g_m has a negative impact on the f_T accordingly, causing the non-linear behavior for the conventional planar-gate transistors. A recent study by Lee *et al.* [15] has already shown that by adopting the Tri-gate topology, a more linear f_T response can be achieved with respect to the varied gate bias voltage. It has been demonstrated in our previous study [18] that flatter Tri-gate f_T can be also maintained throughout higher gate and drain bias voltages thanks to the reduced SCE and on-state gate capacitance lowering (relatively sharp reductions in intrinsic C_{gs} with respect to increased gate- and drain bias voltage). As seen in the intrinsic f_T profiles extracted from the S-parameter measurements of the planar FETs in Fig. 4-a, the peak value of 90 GHz is reached at a bias point of V_G = -4 V, V_D = 15 V. Once the drain bias is altered to either V_D = 20 V or 10 V, the f_T immediately drops down to around 80 GHz and in combination with the increase in the gate voltage, it appears as low as 40 GHz. InAlGaN FinFETs however, have proven almost a bias-independent behavior remaining above 60 GHz and peaking up to 70 GHz (seen in Fig. 4-b) which is advantageous for high-gain power amplifier applications. It has to be noted here that the overall f_T values appear to be relatively low whereas the g_m appears higher. This is due to the adopted total gate width normalization with respect to the effective nano-channel widths, which neglects the parasitic effects. A more detailed analysis on the f_T and parasitics of the Tri-gate devices has already been investigated in a previous study [18].

C. AlN/GaN TRI-GATE HEMTs

Accounting for both planar and FinFETs, two variants of AlN/GaN HEMTs have been fabricated with different total gate widths of Wg = 100 μm and 300 μm. Despite the longer metallurgical width of the gate electrode, FinFETs of the latter variant have the same effective gate width of

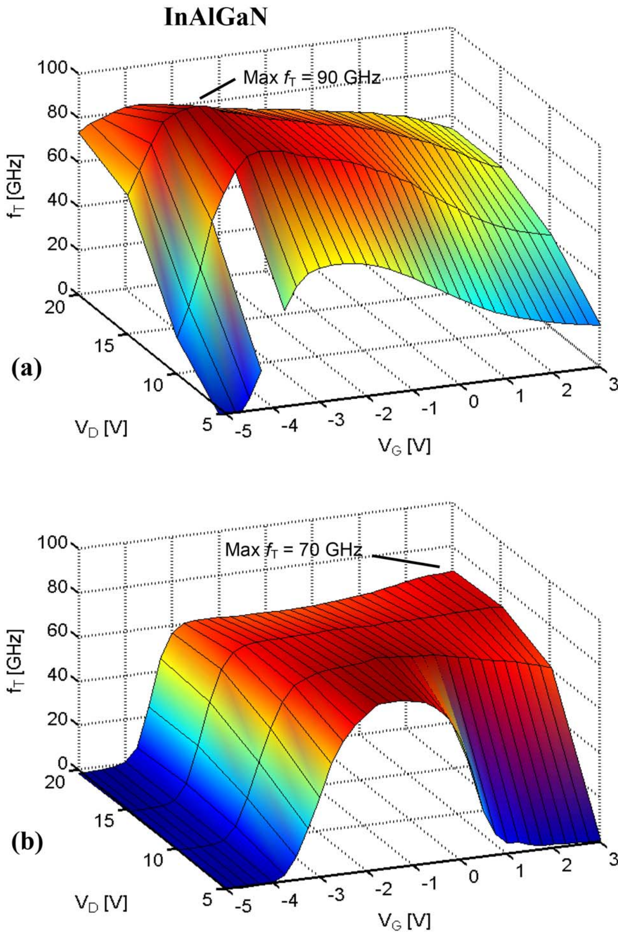

FIGURE 4. Intrinsic current-gain cut-off frequency (f_T) of the (a) planar and (b) Tri-gate InAlGaN HEMTs as a function of gate (V_G) and drain (V_D) bias.

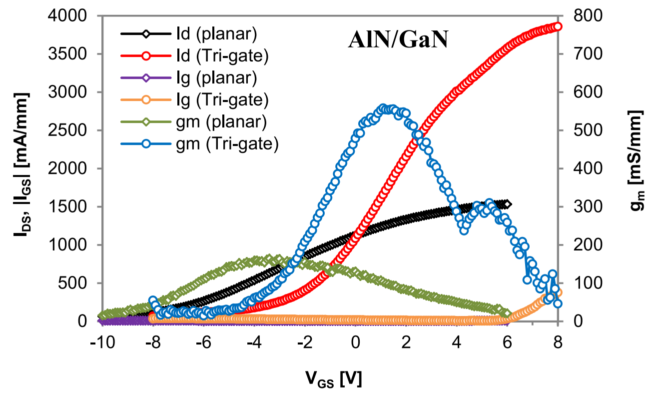

FIGURE 5. DC-transfer characteristics and transconductance of the planar and Tri-gate AlN/GaN HEMTs with W_{eff} = 100 μm at V_D = 30 V.

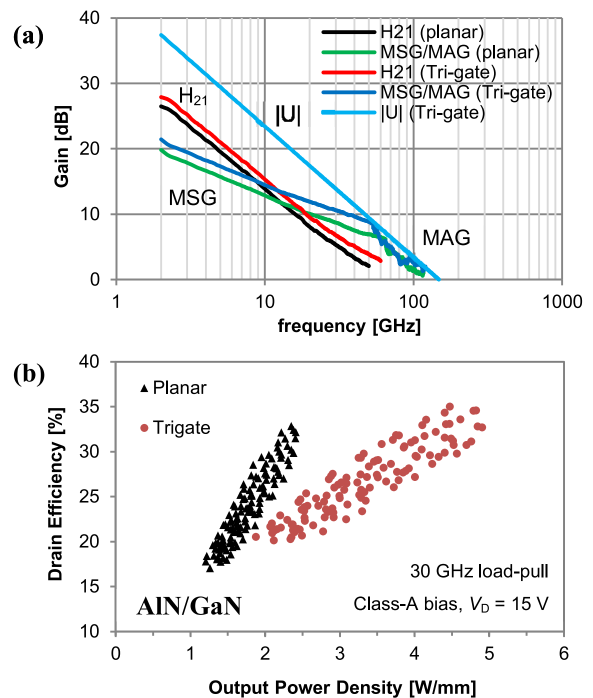

FIGURE 6. MSG/MAG, current gain (h_{21}), unilateral gain ($|U|$) (a), and large-signal performance (b) of the planar and Tri-gate AlN/GaN HEMTs with W_g = 100 μm at V_D = 15 V.

Weff = 100 μm since they consist of n = 1000 nano-channels with Wfin = 100 nm. Hall measurements have revealed 1100 cm^2/Vs of 2DEG mobility, 3.3×10^{13} cm^{-2} of carrier density and 170 Ω of sheet resistance. The measured DC-transfer characteristics of the planar and Tri-gate AlN/GaN HEMTs are indicated in Fig. 5. Occasional minor fluctuations and noisy spikes which are evident in the DC transfer curves of the FinFETs can be attributed to the surface traps caused by the slight etching damages of the sub-micron mesa patterns. In contrast to the medium-level saturation current densities of 1.5 A/mm achieved by the planar FETs, nano-channel FinFETs have delivered very high maximum current densities up to 3.8 A/mm. When compared to the state-of-art, this is one of the highest values recorded by GaN-based Tri-gate HEMTs following the reported devices by Arulkumaran *et al.* [16]. It also needs to be noted that the use of sidewall Si_3N_4 layer during the processing of AlN/GaN FinFETs has enabled eliminating higher gate-leakage currents at very high applied gate bias voltages as it introduces metal-insulator-semiconductor (MIS) interfaces only at the sidewalls of the fin structures.

Fig. 6-a sets display to the measured maximum stable- and available gain (MSG/MAG) responses of the planar and Tri-gate AlN/GaN HEMTs as a function of frequency. At a typical operating drain bias voltage of VD = 15 V, the maximum oscillation frequency (f_{max}) of FinFETs is extrapolated to be around 140 GHz whereas the f_T appears at 60 GHz as extracted from the measured current-gain (h_{21}). The large-signal performances have also been determined through load-pull measurements at 30 GHz of frequency and class-A biasing (I_{DQ} = 0.5 A/mm and 1 A/mm for planar and Tri-gates respectively) which have shown high output power densities up to 5 W/mm with 35% of efficiency as seen in Fig. 6-b.

A comparison of the DC-output (I_D-V_D) characteristics of the Tri-gate HEMTs on all three different structures (namely with AlGaN, InAlGaN, and AlN barriers) is depicted in

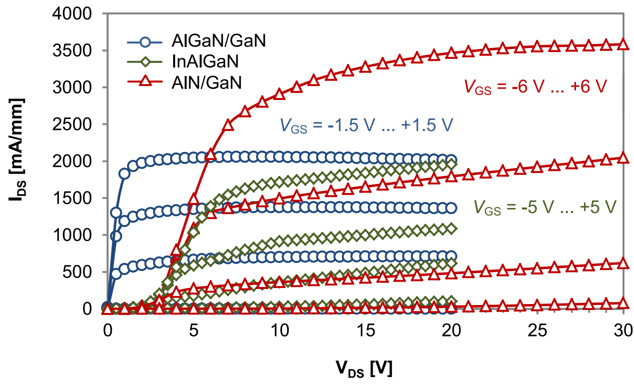

FIGURE 7. DC-output characteristics of Tri-gate HEMTs with AlGaN, InAlGaN, and AlN barriers.

TABLE 1. Device parameters on respective wafer structures.

Barrier / Parameter	ALGaN	InAlGaN	AlN
2DEG mobility	1300 cm^2/Vs	1350 cm^2/Vs	1100 cm^2/Vs
Planar max. I_D	1300 mA/mm	1500 mA/mm	1500 mA/mm
Tri-gate max. I_D	2200 mA/mm	2100 mA/mm	3800 mA/mm
Planar peak g_m	450 mS/mm	230 mS/mm	160 mS/mm
Tri-gate peak g_m	750 mS/mm	370 mS/mm	550 mS/mm
Planar V_{th}	-2.1 V	-6.2 V	-7.4 V
Tri-gate V_{th}	-1.1 V	-3.8 V	-3.6 V
Planar gate leakage	< 20 nA/mm	< 0.2 mA/mm	< 30 mA/mm
Tri-gate gate leakage	< 10 nA/mm	< 0.2 mA/mm	< 30 mA/mm
Planar drain leakage	< 100 nA/mm	< 30 mA/mm	< 50 mA/mm
Tri-gate drain leakage	< 50 nA/mm	< 20 mA/mm	< 50 mA/mm
Planar DIBL	120 mV/V	150 mV/V	300 mV/V
Tri-gate DIBL	50 mV/V	50 mV/V	75 mV/V
Planar SS	150 mV/dec	-	-
Tri-gate SS	75 mV/dec	-	-
Planar f_T/f_{max}	75/175 GHz	90/170 GHz	50/135 GHz
Tri-gate f_T/f_{max}	70/175 GHz	70/150 GHz	60/140 GHz

Fig. 7. It can be noticed that the InAlGaN and AlN/GaN devices exhibit shifted knee-voltages due to the unintentionally grown Schottky-like source and drain contacts on these respective wafers instead of ideal ohmic contacts. In order to keep the entire fabrication process consistent with the AlGaN/GaN devices, a standard procedure has been followed to deposit and anneal the Ti/Al-based metal stack, which resulted in such non-ideal contacts. However, a different process scheme by implementing regrown contacts with Si doping can be used to overcome this condition on wafers with InAlGaN and AlN barriers, which is subject to future work.

Table 1 summarizes the critical device parameters of interest, namely the mobility, saturation current density, peak g_m, threshold voltage (V_{th}), gate and drain leakage currents, DIBL, sub-threshold swing (SS), and f_T/f_{max} figures for each individual structure. Therefore, when compared to the other lattice-matched InAlGaN heterostructure, AlN/GaN Tri-gate devices provide higher peak g_m, current and output power densities whereas the InAlGaN FinFETs exhibit a bias-independent RF performance with very linear f_T.

IV. CONCLUSION

High-current GaN-based Tri-gate HEMTs are fabricated on wafers with binary and quaternary hetero-structures and the respective DC and RF performances are investigated. In comparison with the conventional planar FETs, AlGaN/GaN FinFETs have demonstrated reduced SCE and better off-state performance. Small-signal RF measurements of the Tri-gate devices employing a lattice-matched InAlGaN barrier have also shown bias-independent f_T behavior with very high linearity which is attractive for millimeter-wave applications. Record current densities as high as 3.8 A/mm exhibited by the AlN/GaN Tri-gate HEMTs have proven superior performance over the planar devices.

REFERENCES

[1] D. S. Lee *et al.*, "300-GHz InAlN/GaN HEMTs with InGaN back barrier," *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1525–1527, Nov. 2011.

[2] Y. Yue *et al.*, "InAlN/AlN/GaN HEMTs with regrown ohmic contacts and f_T of 370 GHz," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 988–990, Jul. 2012.

[3] K. Shinohara *et al.*, "Self-aligned-gate GaN-HEMTs with heavily-doped n^+-GaN ohmic contacts to 2DEG," in *Proc. IEEE Int. Electron Devices Meeting*, San Francisco, CA, USA, Dec. 2012, pp. 617–620.

[4] T. Palacios *et al.*, "Influence of the dynamic access resistance in the g_m and f_T linearity of AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 52, no. 10, pp. 2117–2123, Oct. 2005.

[5] R. Aidam *et al.*, "Growth model investigation for AlN/Al(Ga)InN interface growth by plasma-assisted molecular beam epitaxy for high electron mobility transistor applications," *Phys. Status Solidi A*, vol. 211, no. 12, pp. 2854–2860, Dec. 2014.

[6] Y. Liu *et al.*, "Demonstration of undoped quaternary AlInGaN/GaN heterostructure field-effect transistor on sapphire substrate," *Appl. Phys. Lett.*, vol. 86, no. 22, May 2005, Art. ID 223510.

[7] Y. Liu, T. Egawa, and H. Jiang, "Enhancement-mode quaternary AlInGaN/GaN HEMT with non-recessed-gate on sapphire substrate," *Electron. Lett.*, vol. 42, no. 15, pp. 884–886, Jul. 2006.

[8] R. Wang *et al.*, "220-GHz quaternary barrier InAlGaN/AlN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1215–1217, Sep. 2011.

[9] T. Tamura, J. Kotani, S. Kasai, and T. Hashizume, "Nearly temperature-independent saturation drain current in a multi-mesa-channel AlGaN/GaN high electron mobility transistor," *Appl. Phys. Exp.*, vol. 1, no. 2, Feb. 2008, Art. ID 023001.

[10] K. Ohi and T. Hashizume, "Drain current stability and controllability of threshold voltage and subthreshold current in a multi-mesa-channel AlGaN/GaN high electron mobility transistor," *Jpn. J. Appl. Phys.*, vol. 48, no. 8, pp. 1–5, 2009.

[11] M. A. Alsharef, R. Granzner, and F. Schwierz, "Theoretical investigation of trigate AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3335–3341, Oct. 2013.

[12] S. Takashima, Z. Li, and T. P. Chow, "Sidewall dominated characteristics of fin-gate AlGaN/GaN MOS-channel-HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3025–3031, Oct. 2013.

[13] K. S. Im *et al.*, "Characteristics of GaN and AlGaN/GaN FinFETs," *Solid-State Electron.*, vol. 97, pp. 66–75, Jul. 2014.

[14] S. Arulkumaran *et al.*, "$In_{0.17}Al_{0.83}N$/AlN/GaN triple T-shape Fin-HEMTs with g_m=646 mS/mm, I_{ON}=1.03 A/mm, I_{OFF}=1.13 µA/mm, SS=82 mV/dec and DIBL=28 mV/V at VD=0.5 V," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2014, pp. 25.6.1–25.6.4.

[15] D. S. Lee *et al.*, "Nanowire channel InAlN/GaN HEMTs with high linearity of g_m and f_T," *IEEE Electron Device Lett.*, vol. 34, no. 8, pp. 969–971, Aug. 2013.

[16] S. Arulkumaran *et al.*, "Electron velocity of 6×10^7 cm/s at 300 K in stress engineered InAlN/GaN nano-channel high-electron-mobility transistors," *Appl. Phys. Lett.*, vol. 106, no. 5, Feb. 2015, Art. ID 053502.
[17] F. V. Raay *et al.*, "New low-frequency dispersion model for AlGaN/GaN HEMTs using integral transform and state description," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 1, pp. 154–167, Jan. 2013.
[18] E. Ture *et al.*, "Performance and parasitic analysis of sub-micron scaled tri-gate AlGaN/GaN HEMT design," in *Proc. Eur. Microw. Integr. Circuit Conf. (EuMIC)*, Paris, France, Sep. 2015, pp. 97–100.

ERDIN TURE received the M.Sc. degree in microsystems engineering from the University of Freiburg, Freiburg, Germany, in 2013, where he is currently pursuing the Ph.D. degree.

He is a Student Researcher with the Fraunhofer Institute for Applied Solid-State Physics, Freiburg. His research interests include design of broadband power amplifiers and development of GaN HEMTs.

PETER BRÜCKNER received the Diploma degree in electrical engineering and the Ph.D. degree from the University of Ulm, Ulm, Germany, in 2004 and 2008, respectively.

He is currently with the Fraunhofer Institute for Applied Solid State Physics, Freiburg, Germany, where he is involved in the development of GaN HEMT technologies.

BIRTE-JULIA GODEJOHANN received the M.Sc. degree in crystalline materials from the University of Freiburg, Freiburg, Germany, in 2013, where she is currently pursuing the Ph.D. degree in cooperation with the Fraunhofer Institute for Applied Solid State Physics.

Her research interests include epitaxy development of GaN-based HEMT structures using both MOCVD and MBE.

ROLF AIDAM received the Diploma and Ph.D. degrees in physics from the University of Karlsruhe, Karlsruhe, Germany, in 1996 and 1998, respectively.

Since 2002, he has been a Research Physicist with the Fraunhofer Institute for Applied Solid State Physics, Freiburg, Germany. His research interests include InP- and GaAs-based electronics and optoelectronics as well as GaN-based electronics.

MOHAMED ALSHAREF received the master's degree in electrical engineering from Technische Universität Ilmenau, Germany, in 2012. He is with the RF & Nano Device Research Group, TU Ilmenau.

His current research work centers on modeling and simulation of nitride heterostructures.

RALF GRANZNER received the Diploma and Ph.D. degrees from Technische Universität Ilmenau, Germany, in 2000 and 2013, respectively.

He is with the RF & Nano Device Research Group, TU Ilmenau. His current research interests include on modeling and simulation of devices based on nitride heterostructures, silicon nanowires, and 2-D materials.

FRANK SCHWIERZ (M'96–SM'01) received the Ph.D. degree from TU Ilmenau, Germany, in 1986.

He serves as a Privatdozent and the Head of the RF & Nano Device Research Group, TU Ilmenau. His research interests include design and material concepts for transistors.

RÜDIGER QUAY (M'01–SM'10) received the Diploma degree in physics from Rheinisch-Westfälische Technische Hochschule, Aachen, Germany, in 1997, a second Diploma degree in economics in 2003, and the Ph.D. (Hons.) degree in technical sciences and the Venia Legendi (Habilitation) degree in microelectronics from Technische Universität Wien, Vienna, Austria, in 2001 and 2009, respectively.

In 2001, he joined the Fraunhofer Institute of Applied Solid-State Physics, Freiburg, Germany. He is currently the Deputy Head of the Business Field Gallium Nitride RF-Power Electronics with Fraunhofer. Since 2011, he has been a Lecturer with the IMTEK, Albert-Ludwig University, Freiburg. He has authored and co-authored over 200 refereed publications and two monographs. He holds two patents.

Dr. Quay has been an Associate Editor of the *International Journal of Microwave and Wireless Technologies*, since 2011. Since 2013, he has been an Associated Editor of the IEEE ELECTRON DEVICE LETTERS. He is a Co-Chairman of MTT-6, Microwave and Millimeter Wave Integrated Circuits, and since 2012, he has been a member of the IEEE Electron Device Society Compound Semiconductor Subcommittee.

OLIVER AMBACHER received the Dipl.-Phys. and Dr. degrees (Hons.) from Ludwig-Maximilians and Technical University Munich, Munich, Germany, in 1989 and 1993, respectively.

In 1993, he joined the Walter Schottky Institute, Technical University Munch, to investigate the epitaxial growth of group-III nitrides-based heterostructures. Since 1995, the research interests of his group have included fabrication of GaN-based devices as well as on the understanding of polarization-induced effects in group-III nitride heterostructures and quantum wells. From 1998 to 1999, he was an Alexander von Humboldt Fellow with Cornell University, Ithaca, NY, for one year, where he was involved in the optimization of polarization induced AlGaN/GaN HEMTs for high-frequency and high-power applications. He became a Professor of Nanotechnology and the Head of the Institute for Solid State Electronics, Technical University of Ilmenau, Ilmenau, Germany, in 2002. In 2004, he was elected as the Head of the New Center of Micro- and Nanotechnologies. Since 2007, he has been the Director of the Fraunhofer Institute for Applied Solid State Physics, Freiburg, Germany, and a Professor for Compound Semiconductor Microsystems with the University of Freiburg, Freiburg.