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Abnormal Output Characteristics of p-Type Low Temperature Polycrystalline Silicon Thin Film Transistor Fabricated on Polyimide Substrate

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ABSTRACT We report on an abnormal output characteristics in p-type low temperature polycrystalline silicon thin-film transistors fabricated on polyimide (PI); negative differential conductance behavior is often observed in saturation region of drain current from large width devices. To understand such abnormal output characteristics, device dimension dependence was studied in a systematic way. As a result, we found that enhanced self-heating is mainly responsible originating from the poor thermal conductivity of PI substrate. A related degradation model is also proposed.

INDEX TERMS Thin-film transistor (TFT), LTPS, self-heating effect, hot carrier effect, polyimide (PI), flexible.

I. INTRODUCTION

Flexible displays have drawn much attention due to their various merits including light weight, unbreakable form, and its portability in application [1], [2]. Active matrix organic light emitting diode (AMOLED) arrays are also suitable on flexible substrate along with thin-film transistor (TFT) backplanes, which not only request high mobility but also good saturation behavior for sufficient current driving in drain current-drain voltage (I_D-V_D) output characteristics. For the flexible AMOLED application, low-temperature processed amorphous indium-gallium-zinc-oxide (a-IGZO) TFT has been considered as a candidate to meet with such output characteristics [2] while p-type low temperature polycrystalline silicon (LTPS) TFT is more readily-suggested candidate with even superior current drivability to a-IGZO TFT. A favored flexible substrate is polyimide (PI), which can possibly endure device fabrication temperature of conventional LTPS process [3]. However, PI induces heat barrier issue due to its inherent poor thermal conductivity, which is far poorer than that of glass substrate [1], [4], although even glass substrate for conventional LTPS TFT seems not to show good thermal conductivity [5]. So, self-heating-induced degradation must be an issue in LTPS TFT on PI substrate. Nevertheless, studies to characterize the self-heating in LTPS TFT on PI substrate are rare in fact [4].

In this letter, we report on abnormal output characteristics of p-type LTPS TFT fabricated on PI substrate, also proposing a model to explain the causes of the degradation; serious self-heating enhanced by PI substrate was mainly responsible for such behavior.

II. EXPERIMENT

Conventional coplanar p-type LTPS TFTs were fabricated on PI with carrier glass substrate. A 17 μm-thick PI layer was slit-coated on 370 × 470 mm^2 glass substrate with buffer dielectric layer, and then annealed at 450 °C for 4 hr in a convection oven for degassing and hardening. A 50 nm-thick a-Si layer was deposited on the PI by SiH_4-based plasma-enhanced chemical vapor deposition (PECVD) and crystallized by excimer-laser annealing. After deposition of 100 nm-thick PECVD SiO_2 of gate insulator (GI), 300 nm-thick Mo gate was patterned by

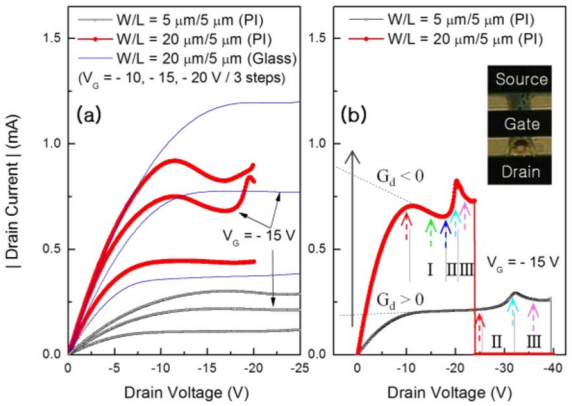

FIGURE 1. **(a) Comparison of I_D-V_D output curves of TFTs fabricated on PI and glass, (b) another comparison of output curves of two TFTs on PI with different W/L ratio, here three device failure regions were defined with 20/5 ratio sample as I (NDC), II (kink), and III (eventual breakdown). Inset shows an optical microscopic image (bottom illumination, W/L = 5 μm/5 μm) after breakdown by V_D sweep.**

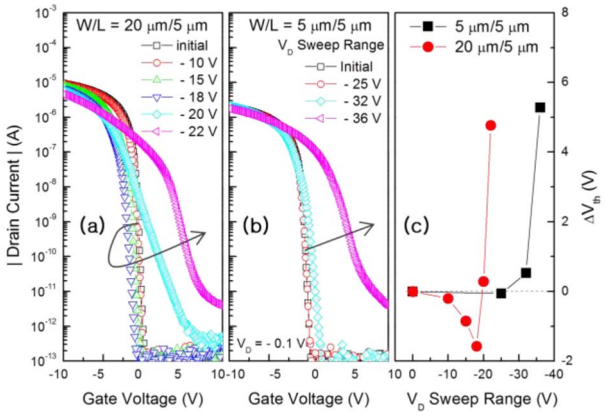

FIGURE 2. **Variation of transfer curves after V_D sweep, for (a) wide (W = 20 μm) and (b) narrow (W = 5 μm) TFT. (c) Plots of ΔV_{th} vs. V_D sweep range to show the V_{th} behavior of wide and narrow TFTs.**

wet etch. For self-aligned highly doped source/drain (S/D) region, B was implanted (70 keV, 2.5e^{15} cm^{-2}) through GI with gate metal as implantation mask and subsequent annealing at 380 °C followed for dopant activation. Stacked Mo/Al/Mo was patterned as S/D metal, prior to final passivation processes composed of SiN_x by PECVD at 230 °C and 1 hr-long post-annealing in air ambient (at 230 °C). After TFT fabrication was finished, the PI substrate was delaminated by laser anneal using 355 nm wavelength (through glass substrate), and a free-standing flexible backplane was eventually formed, which was attached to a glass carrier for electrical measurements. The drain current-gate voltage (I_D-V_G) transfer and I_D-V_D output characteristics were measured with Agilent 4155C semiconductor parameter analyzer.

III. RESULTS AND DISCUSSION

Fig. 1(a) shows I_D-V_D curves of three p-type LTPS TFTs with 5 μm gate length (L): two on PI substrate and one on glass. It is interesting to note that abnormal output characteristics with negative differential conductance (NDC, $G_d \equiv \Delta I_D/\Delta V_D$) are apparently observed from TFTs on PI with wide width (W) under high V_G and high V_D sweep region. (The device on PI substrate shows slightly higher I_D (before NDC region) than that of other device on glass but this is regarded as an intrinsic difference that comes from their V_{th} difference.) In order to investigate the abnormal behavior on PI-substrate devices in more detail, V_D was swept up to an extended range (0 ~ (-) 40 V) under a representative V_G = (-) 15 V as shown in Fig. 1(b), where the abnormal V_D regions are clearly observed and device breakdown eventually follows. In fact, a drastic I_D drop by device breakdown should be observed for all devices, because thermal runaway by extreme self-heating in the active layer anyway takes place at a certain high V_D as shown in the inset image. However, there exist a noticeable difference between the two TFT devices with a wide (20 μm) and narrow (5 μm) W, since the device with wide W obviously shows the NDC region I prior to region II and III while the other TFT with narrow W does not display the region I at all. We thus suspect that such abnormal output curves with NDC come from wide W which leads to high channel temperature on PI substrate.

To find out and explain the root causes of NDC, we attempted a systematic analysis by I_D-V_G transfer characteristic measurements and device area variation. Fig. 2(a) shows negative shift of transfer curves in 20 μm-wide devices, which have been swept for output curve to NDC region I before transfer curve measurements. Positive shift also follows after the output curve sweep range increases up to region II and III. In contrast, the 5 μm-narrow TFT in Fig. 2(b) shows no negative but only positive shift due to its absence of NDC region. The plots of Fig. 2(c) summarize the trend of threshold voltage shift (ΔV_{th}) in both devices as a function of initial output sweep range; here, V_{th} was defined as the V_G at $|I_D|$ of 1 nA (under $|V_D|$ = 0.1 V). The negative ΔV_{th} in the wide channel TFT indicates that it might be caused by hole trapping at the GI/poly-Si interface and at GI itself near the interface as well, and also suggests that the trapping would be facilitated in thermionic ways by channel-heating under the V_D sweep (to NDC region) and constant V_G of (-) 15 V. The heat dissipation (power dissipation) from the channel becomes more difficult as W increases more, leading to higher channel temperature. It is because the PI substrate beneath the wide channel cannot properly dissipate the heat [4]. Elevated temperature may enhance thermionic hole emission from channel to the trap levels in the GI [5], which causes negative threshold voltage shift. Devices with narrow W seldom show such negative shift due to their dimensional advantage: relatively lower temperature during device operation.

To assure such channel dimension dependence of the NDC, we measured I_D-V_D curves of TFTs with various device dimensions on PI. First, Fig. 3(a) displays

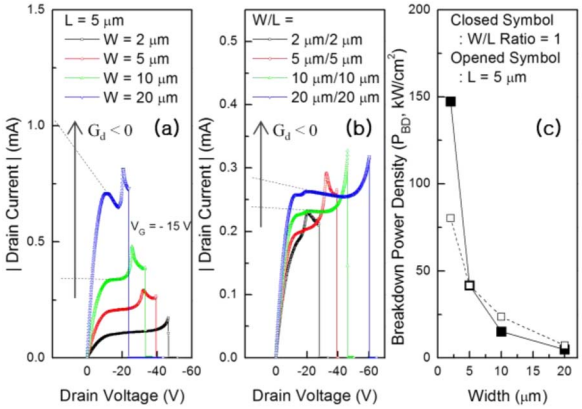

FIGURE 3. **Comparison of I_D-V_D curves among TFTs (a) with different W (L is fixed as 5 μm), and (b) with different device area but with same W/L ratio (= 1). (c) Breakdown power density (P_{BD}) normalized by TFT area at a fixed V_G (= - 15 V) as a function of W, obtained from (a) and (b).**

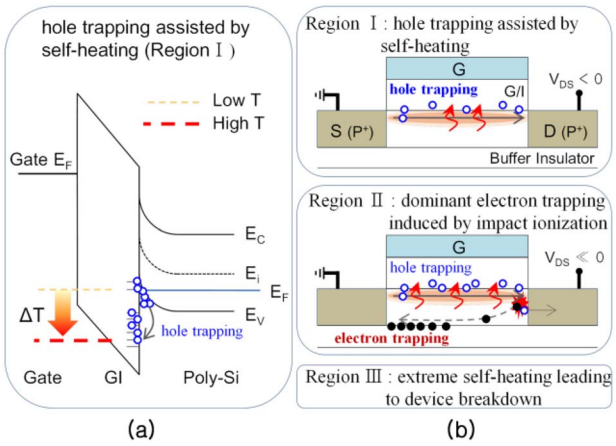

FIGURE 4. **Device failure (degradation) processes: (a) band model illustrating thermionic emission of thermally-excited holes to elevated energy states mainly at the GI/poly-Si front interface (including the GI near the interface) (NDC), (b) schematic device model explaining the NDC output characteristics (up: region I) and impact-ionization-induced kink (middle: region II). Region III is about the device breakdown by thermal runway as shown in the inset of Fig. 1(b).**

I_D-V_D curves of 5 μm-long TFTs with various widths (W = 2 ∼ 20 μm), where W-dependence of NDC is displayed; devices with wide W (≥ 10 μm) only show NDC. Next, Fig. 3(b) plots I_D-V_D curves of TFTs with different device area but the fixed W/L ratio (= 1). From the results, it is again evidenced that NDC phenomena are mainly from large area devices. Temperature would be elevated by enhanced self-heating under corresponding power density [$P_D \equiv I_D \times V_D$/area (WL)] [6]. Breakdown P_D (P_{BD}) is thus plotted in Fig. 3(c), according to which P_{BD} appears dependent on TFT dimension and easy breakdown comes to the devices with wide W (> 5 μm). Similar P_D –TFT area relation was reported in the previous literature [7].

Fig. 4(a) shows a band diagram model to illustrate the temperature-induced hole trapping mainly at the GI/poly-Si front interface (including the GI near the interface), which takes place in a large device under the high $|V_G|$ for region I (or NDC); temperature increase (ΔT) by self-heating induces thermionic emission of thermally-excited holes to elevated energy states at the front interface, and this would not be easy in devices with small dimension due to low thermal energy. Such hole trapping at the front interface would cause negative ΔV_{th} and increase hole injection barrier near the source (S) region as well.

The upper part of Fig. 4(b) again illustrates such a hole-trapping model with a schematic device cross section. In the mid part of Fig. 4(b), we also propose a model for the region II, which is known as kink, originating from hot carrier effect because impact ionization would occur near the drain (D) under a very high V_D [8]. According to the schematic device cross section, the generated electrons by impact ionization would move to the S along the back channel while they are often trapped at the back interface due to its floating body structure [9]. Such impact-ionization-induced behavior eventually results in positive-feedback effect; the trapped electrons near the S and back-interface (mid part of Fig. 4(b)) would lower the source/channel barrier, decrease V_{th} (positive shift), increase I_D, and generate more electrons by impact ionization in return. So, these phenomena are opposite to the NDC mechanism. Although enhanced self-heating always exists in both region I and II, higher V_D applied for region II now causes the impact-ionization overwhelming the NDC phenomena of region I. The kink phenomena take place in all TFT devices for their final step after output saturation. Eventually, reaching to region III, the device with increased I_D and V_D would experience extreme self-heating and thermal runaway that causes device breakdown as shown in the inset of Fig. 1(b). Likewise, we now believe that our proposed model accordingly explain the experimental results and data shown in Fig. 1∼3.

IV. CONCLUSION

We studied abnormal output characteristics which are encountered in p-type LTPS TFT fabricated on PI substrate, of which the poor thermal conductance leads to NDC phenomena at high V_Ds before kink and device breakdown come. Such NDC was often observed from large area devices due to their poor heat dissipation efficiency, which causes device temperature increase and thermionic hole trapping mainly at the front interface between GI and poly-Si. After output V_D sweep to NDC region, V_{th} thus increases toward negative voltage due to the hole trapping. Under a higher V_D the kink is then caused by hot carrier effect as reported, shifting the V_{th} back to positive voltages. We here propose device failure models to explain NDC and kink, concluding that enhanced self-heating on PI substrate is responsible for the abnormal output characteristics although eventual device breakdown is combined with hot carrier effect.

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