Analytical Modeling of Flicker Noise in Halo Implanted MOSFETs

HARSHIT AGARWAL[1] **(Student Member, IEEE), SOURABH KHANDELWAL**[2] **(Member, IEEE),**
SAGNIK DEY[3] **(Senior Member, IEEE), CHENMING HU**[2] **(Fellow, IEEE), AND**
YOGESH SINGH CHAUHAN[1] **(Senior Member, IEEE)**

1 Nanolab, Department of Electrical Engineering, Indian Institute of Technology Kanpur, Kanpur 208016, India
2 Department of Electrical Engineering and Computer Science, University of California, Berkeley, Berkeley, CA 94720, USA
3 SPICE Modeling Laboratory, Embedded Processing Technology Development, Texas Instruments, Dallas, TX 75243, USA

CORRESPONDING AUTHOR: Y. S. CHAUHAN (e-mail: chauhan@iitk.ac.in)

ABSTRACT An improved analytical model for flicker noise ($1/f$ noise) in MOSFETs is presented. Current models do not capture the effect of high-trap density in the halo regions of the devices, which leads to significantly different bias dependence of flicker noise across device geometry. The proposed model is the first compact model implementation capturing such effect and show distinct improvements over other existing noise models. The model is compatible with BSIM6, the latest industry standard model for bulk MOSFET, and is validated with measurements from 45-nm low-power CMOS technology node.

INDEX TERMS BSIM6, halo doping, flicker noise, compact model.

I. INTRODUCTION

For low power technologies driven by challenging targets for off-state leakage current without compromising performance, strong halo implants are necessary for suppressing parasitic 2-D electrostatics for the minimum length device. However, such strong halo implants have been found to be detrimental to analog performance [1], [2] including 1/f noise [3], [4] in particular for long channel devices [5]. The degradation of 1/f noise has been attributed to extra trap states generated due to implantation process [3], and/or threshold voltage variation along the channel [4]. Due to this reason noise behavior in strong pocket devices are significantly different than in uniformly doped devices. Existing compact models that can successfully capture noise behavior in uniformly doped devices are no longer valid.

Fig. 1 shows the measured median (of 21 different sites in wafer) drain current flicker noise power spectral density (PSD) normalized to channel width for long and short channel devices for 45nm low power CMOS technology node [6]. Note that contrary to uniform channel doped noise, the strong pocket devices show no impact of channel length scaling for 1/f noise in the subthreshold or near-threshold-voltage region. This is a key factor that needs to be understood as analog designs are targeting low power regions of operation. As the drain current is increased by increasing the gate-voltage, the long channel device further show anomalous bias dependence through a sudden decrease in slope. The short channel device does not show this characteristic. Such behavior cannot be captured by existing noise models based on uniformly doped channel devices [7] (see Fig. 1). Although a noise model specific to halo devices was earlier proposed by Wu *et al.* [4] based on a non-uniform threshold voltage distribution using the unified noise model, it adds the noise contributions from the different regions with equal proportions. Such formulation might lead, in certain cases, to excess contribution of noise from pocket part in strong inversion, or excess contribution from channel part for lower bias. Also that model does not consider the impact of higher trap densities (in halo regions) on noise typical to pocket implant process, and is valid only in strong inversion. In this work, we will discuss the physical mechanisms behind the bias dependence for halo implanted devices and present an analytical model, valid from weak inversion (WI) to strong inversion (SI), that can capture the behavior across
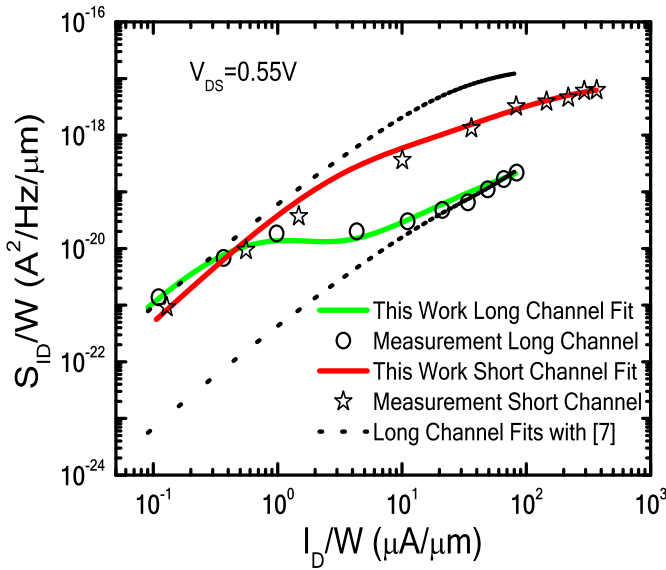
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FIGURE 1. Drain current flicker noise power spectral density versus drain current at V_{DS} = 0.55 V, both normalized to channel width. Measurements are from the same technology as in [6] and show complex dependency on gate voltage, especially for long channel device. Weak inversion noise is dominated by contributions from halo regions and therefore there is no impact of length scaling on 1/f noise.

FIGURE 2. Representation of MOSFET for noise modeling. Channel length L can be divided into two parts—the halo region of length L_h with doping N_h and the channel region of length L-L_h with doping N_{ch}.

FIGURE 3. Small signal analysis of two transistor noise circuit. Principle of superposition is used to obtain total noise from individual noise contributions. (a) Noisy halo transistor and noiseless channel transistor. (b) Noisy channel transistor and noiseless halo transistor.

length considering the impact of both non-uniform threshold voltage and increased trap density. The model is compatible with BSIM6 MOS model, which is the latest industry standard compact model of bulk MOSFET [8]–[10].

II. ANALYTICAL FLICKER NOISE MODEL
A. MODEL FORMULATION
Starting with the earlier Langevin method for flicker noise modeling, there exist other approaches like equivalent circuit method, impedance field method, Klaassen Prins (KP) approach, etc. [11]–[13]. The presented formulation is based on small signal approach, which is similar to the impedance field method. The halo doped transistor can be represented as in Fig. 2, where the total length L is segmented into two parts: a region of higher doping of length L_h with equivalent resistance R_h, noise PSD $S_{ID,h}$ and another low doped region of length L-L_h with resistance R_{ch} and noise PSD $S_{ID,ch}$. In a very crude form (neglecting transistor transconductance), overall drain current noise PSD (S_{ID}) can be expressed as [14],

$$S_{ID} = S_{ID,h} \left[\frac{R_h}{R_h + R_{ch}} \right]^2 + S_{ID,ch} \left[\frac{R_{ch}}{R_h + R_{ch}} \right]^2 \quad (1)$$

We have demonstrated earlier that (1) can be implemented by simple two transistor subcircuit model where resistances of channel and halo regions are calculated by SPICE [14]. However, such an implementation cannot be used for a practical industry standard compact model formulation since it degrades the simulation speed as well as complicates model parameter extraction procedure. Here we will present a complete analytical model that can successfully reproduce the
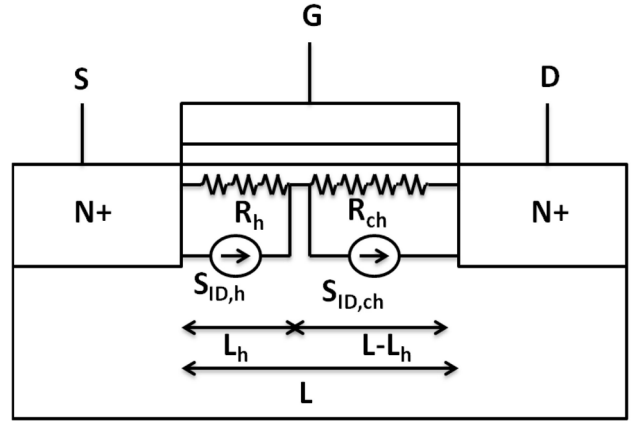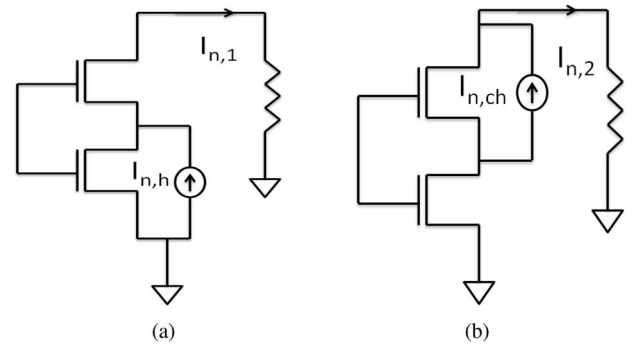
series transistor noise behavior without above limitations. Firstly, the I-V parameters of the family of devices under test are extracted. For the noise modeling, it is now assumed that the transistor is composed of two transistors, channel transistor of length L-L_h and halo transistor of length L_h connected in series and carries same current (I_{DS}) as in single transistor configuration. The individual contribution of the halo and channel transistors to overall noise is obtained using small signal analysis and principle of superposition.

From Fig. 3(a), the drain current noise PSD due to halo transistor is obtained by assuming channel transistor to be noiseless. Using small signal analysis,

$$I_{n1} \simeq I_{n,h} \frac{g_{m,ch} + g_{d,ch}}{g_{m,ch} + g_{d,ch} + g_{d,h}} \quad (2)$$

$$S_{ID,1} = S_{ID,h} \left[\frac{g_{m,ch} + g_{d,ch}}{g_{m,ch} + g_{d,ch} + g_{d,h}} \right]^2 \quad (3)$$

where $g_{m,ch}$, $g_{d,ch}$ are the transconductance and output conductance of channel transistor and $g_{d,h}$ is the transconductance of the halo transistor. Similarly from Fig. 3(b),

the noise PSD due to the channel transistor is expressed as

$$I_{n2} \simeq I_{n,ch} \frac{g_{d,h}}{g_{m,ch} + g_{d,ch} + g_{d,h}} \tag{4}$$

$$S_{ID,2} = S_{ID,ch} \left[\frac{g_{d,h}}{g_{m,ch} + g_{d,ch} + g_{d,h}} \right]^2 \tag{5}$$

Total drain current noise PSD becomes,

$$S_{ID} = S_{ID,1} + S_{ID,2} \tag{6}$$

$$= S_{ID,h} \left[\frac{g_{m,ch} + g_{d,ch}}{g_{m,ch} + g_{d,ch} + g_{d,h}} \right]^2$$

$$+ S_{ID,ch} \left[\frac{g_{d,h}}{g_{m,ch} + g_{d,ch} + g_{d,h}} \right]^2 \tag{7}$$

$$= S_{ID,h}.CF_h + S_{ID,ch}.CF_{ch} \tag{8}$$

We refer to the multiplying factors to $S_{ID,h}$ and $S_{ID,ch}$ in (7) as contribution factors (CF). From [15],

$$g_{d,ch} = 2n_q \mu C_{ox} \frac{W}{L - L_h} V_t q_{d,ch} \tag{9}$$

$$g_{d,h} = 2n_q \mu C_{ox} \frac{W}{L_h} V_t q_{d,h} \tag{10}$$

$$g_{m,ch} = 2\mu C_{ox} \frac{W}{L - L_h} V_t (q_{s,ch} - q_{d,ch}) \tag{11}$$

where n_q, μ, C_{ox}, and V_t are the slope factor, effective mobility, oxide capacitance per unit area and thermal voltage respectively. $q_{s,ch}$, $q_{d,ch}$, $q_{s,h}$ and $q_{d,h}$ are the normalized inversion charge densities at the source and drain ends of channel and halo transistor respectively. q_{sh} and $q_{d,ch}$ are obtained from analytical solution of BSIM6 [16] charge equation given by (12), where pinch-off potential (ψ_p, normalized to thermal voltage V_t) is given by (13) and is calculated independently for the two transistors using source potential $v_{ch} = v_s$ and $v_{ch} = v_d$ (effective drain potential) respectively. v_g, v_{fb}, ϕ_f and γ in these equations are the normalized gate voltage, flat band voltage, bulk potential and body factor, respectively and ψ_{p0} is the approximation of pinch-off potential when it is close to zero. To calculate $q_{d,h}$ and $q_{s,ch}$, the fact that the same current flows in one transistor and two transistor noise equivalent configuration is used,

$$i_h = \frac{I_{DS}}{-2n_q \mu C_{ox} \frac{W}{L_h} V_t^2} = \left(q_{s,h}^2 + q_{s,h} \right) - \left(q_{d,h}^2 + q_{d,h} \right) \tag{14}$$

$$i_{ch} = \frac{I_{DS}}{-2n_q \mu C_{ox} \frac{W}{L-L_h} V_t^2} = \left(q_{s,ch}^2 + q_{s,ch} \right) - \left(q_{d,ch}^2 + q_{d,ch} \right) \tag{15}$$

where i_h and i_{ch} are the normalized drain current of halo and channel transistor respectively. Since I_{DS} is known from DC modeling, the above equations are solved for,

$$q_{d,h} = -\frac{1}{2} + \frac{1}{2}\sqrt{1 + 4\left(q_{s,h}^2 + q_{s,h} - i_h\right)} \tag{16}$$

$$q_{s,ch} = -\frac{1}{2} + \frac{1}{2}\sqrt{1 + 4\left(q_{d,ch}^2 + q_{d,ch} + i_{ch}\right)} \tag{17}$$

B. NOISE SOURCE
The source of flicker noise in MOSFETs is attributed to mobility fluctuation and/or carrier number fluctuation [17]–[19]. There exist popular models which unifies the two approaches [7], [20], [21]. Here we have used the unified model presented in [20] (which has been widely used in industry standard bulk MOSFET models [22]–[24]) for halo and channel transistors separately, where S_{ID} is expressed as

$$S_{ID,h} = \frac{kTI_{DS}^2}{\gamma f W L_h^2} \int_0^{L_h} \frac{N_{t,h}^*(E_{F_n})}{N_h^2} dx \tag{18}$$

$$S_{ID,ch} = \frac{kTI_{DS}^2}{\gamma f W (L - L_h)^2} \int_{L_h}^L \frac{N_{t,ch}^*(E_{F_n})}{N_{ch}^2} dx \tag{19}$$

where apparent trap density $N_{t,ch(h)}^*(E_{F_n}) = A_{ch(h)} + B_{ch(h)}N_{ch(h)} + C_{ch(h)}N_{ch(h)}^2$, A, B, C are the noise parameters, γ is the tunneling parameter, k is the Boltzmann constant and T is the temperature. It is important to note that $S_{ID,h}$ and $S_{ID,ch}$ are in explicit form since (18) and (19) can be expressed as a function of $q_{s,h}$, $q_{d,h}$ and $q_{s,ch}$ and $q_{d,ch}$ respectively [25]. Also note that S_{ID} in the halo region might be locally higher than in the channel region due to increased trap density which is captured by the noise parameters of the halo transistor. Hence formulation of S_{ID} is based on the local trap density, inversion charge densities specific to the region that generates the noise as well as the length of the region. Using (18) and substituting (16), (17), $q_{s,h}$, $q_{d,ch}$ in (7) gives the overall PSD.

III. RESULTS AND DISCUSSION
The model is validated with the measurements at 45nm CMOS technology. Validation is carried for both long and short channel device at $V_{DS} = 0.55$V. Fig. 1 shows the model data overlay for long and short channel transistors. Unlike for the short channel case, long channel device shows significant bias dependency, and the model is able to accurately reproduce the experimental characteristics both for the long and short channel devices. For the better understanding,

$$\ln(q_i) + \ln\left[\frac{2n_q}{\gamma} \left(q_i \frac{2n_q}{\gamma} + 2\sqrt{\psi_p - 2q_i} \right) \right] + 2q_i = \psi_p - 2\phi_f - v_{ch} \tag{12}$$

$$\psi_p = \begin{cases} -\ln\left[1 - \psi_{p0} + \left(\frac{v_g - v_{fb} - \psi_{p0}}{\gamma} \right)^2 \right] & \text{if } v_g - v_{fb} < 0 \\ 1 - e^{-\psi_{p0}} + \left[\sqrt{v_g - v_{fb} - 1 + e^{-\psi_{p0}} + \left(\frac{\gamma}{2} \right)^2} - \frac{\gamma}{2} \right]^2 & \text{otherwise} \end{cases} \tag{13}$$
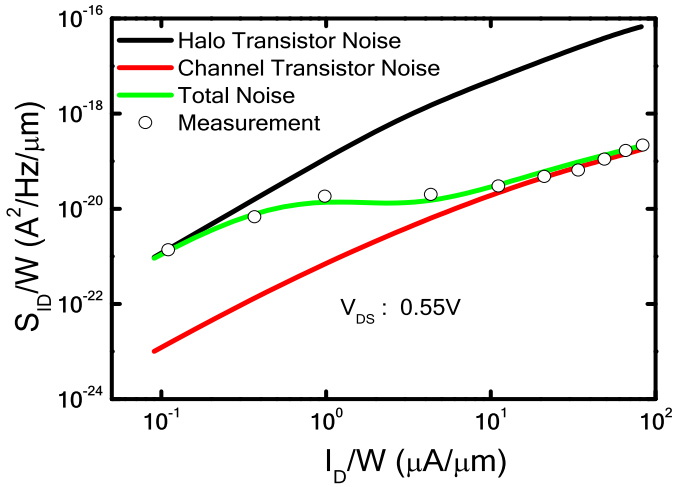
FIGURE 4. Model validation with long channel device: S_{ID} versus I_{DS} at $V_{DS} = 0.55$ V. S_{ID} asymptotically follows halo transistor noise in weak inversion and channel transistor noise in strong inversion.
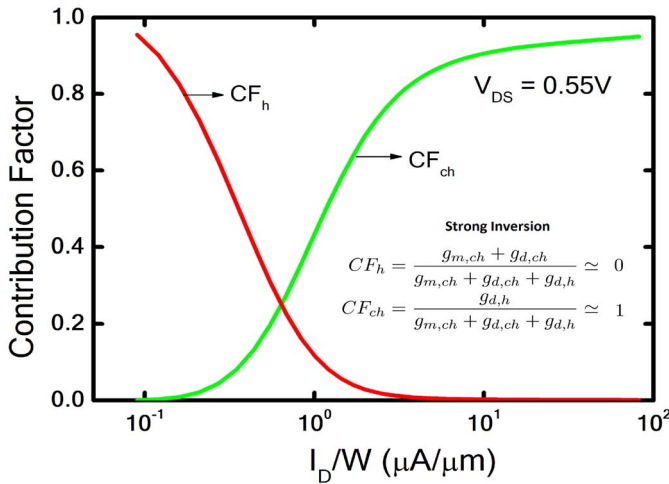

FIGURE 5. Contribution factor of halo and channel transistors versus drain current. In weak inversion, $CF_h \gg CF_{ch}$, and thus S_{ID} is dominated by the noise from the halo region [see (8)]. On the other hand, CF_h falls rapidly in the strong inversion leading to the negligible contribution from halo region in S_{ID}. The role of CF in this model is similar to that of impedance field [11], which is responsible for noise propagation from a point in the channel to the drain terminal. Note that [4] adds halo and channel contribution with equal weights, therefore will overestimate noise in strong inversion.

long channel noise PSD along with the halo and channel transistor PSD is shown in Fig. 4. Although the devices have halo doping at source and drain ends, we found that two transistor sub-circuit implementation is sufficient to capture the bias and channel length dependencies for noise modeling and simpler for parameter extraction than a three transistor implementation. Due to higher doping in halo MOSFET, it has higher threshold voltage than the channel counterpart which leads to significantly lower inversion charge density especially at low gate voltages. For a given current, S_{ID} is inversely proportional to the square of inversion charge density, and therefore halo transistor will have much higher S_{ID} compared to the channel transistor. Furthermore, in WI
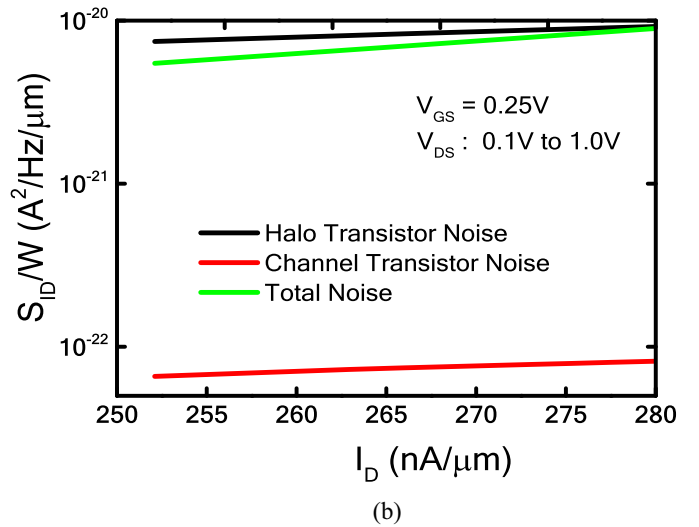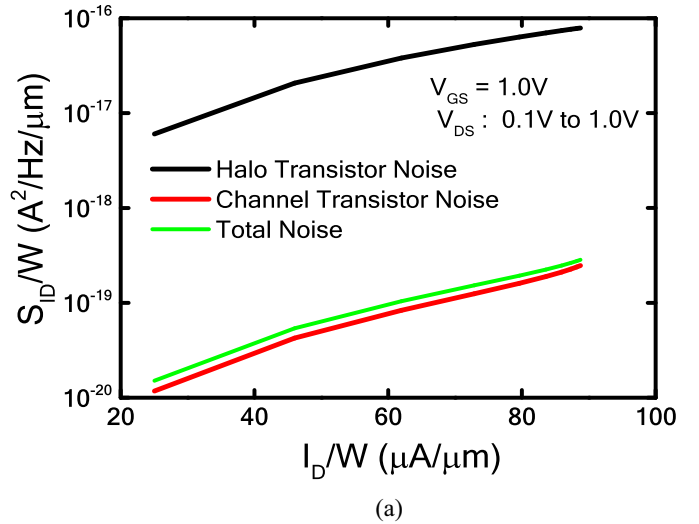

(a)

(b)

FIGURE 6. Simulated drain current noise spectral density versus drain current for constant gate voltage and varying V_{DS} from 0.1 to 1.0 V for the long channel device. (a) $V_{GS} = 1.0$ V. (b) $V_{GS} = 0.25$ V. (a) High gate voltage strongly inverts both halo and channel regions. However, resistance of the channel region is larger as its length is large compared to the halo region, as a result total noise is dominated by the channel region noise. (b) Halo region offers much higher resistance than the channel part due to its high threshold voltage and hence the total noise is determined by the noise of the halo transistor.

$g_{d,h} \ll g_{m,ch}$ (as $q_{s,ch} \gg g_{d,h}$ since halo transistor has higher threshold voltage) leading to

$$CF_h = \frac{g_{m,ch} + g_{d,ch}}{g_{m,ch} + g_{d,ch} + g_{d,h}} \simeq 1 \qquad (20)$$

$$CF_{ch} = \frac{g_{d,h}}{g_{m,ch} + g_{d,ch} + g_{d,h}} \simeq 0 \qquad (21)$$

Since the contributed noise is the product of CF and S_{ID}, overall noise is dominated by halo transistor noise in WI. From (8) it follows that,

$$S_{ID} \simeq S_{ID,h} \qquad (22)$$

While the CF for the halo transistor falls rapidly, the CF for the channel transistor rises sharply as the region of operation moves from WI to SI as shown in Fig. 5, and as a result,

the channel transistor noise becomes the dominant component of the noise in SI. The model presented in [4] adds the individual contributions with equal weights, and therefore cannot model the complex noise characteristics. Fig. 1 also shows the S_{ID} vs drain current for short channel device. It is interesting to observe that short channel device does not shows the bias dependency like the long channel device. This can be explained by the fact that the length of halo transistor is comparable with the length of channel transistor for short channel device, making the transition smoother from halo dominated region to channel dominated region. For the sake of completeness, the model behavior with different drain voltage is also studied. Fig. 6 shows the drain current noise PSD vs drain current for two gate voltages, $V_{GS} = 1V$ in Fig. 6(a) and $V_{GS} = 0.25V$ in Fig. 6(b), and varying drain voltage. For the entire drain bias range (0.1V to 1.0V), total noise is mainly due to the channel transistor noise in Fig. 6(a). This could be understood as follows: high gate voltage strongly inverts both channel and halo regions, however channel region offers higher resistance due to its larger length (as compared to halo region length) leading to $CF_{ch} >> CF_h$ and hence $S_{ID,ch} >> S_{ID,h}$ from (8). Similarly for the low gate voltages, total noise is dominated by the noise of the halo region as seen in Fig. 6(b), since resistance of the halo region is much higher than the resistance of the channel region due to its high threshold voltage.

IV. CONCLUSION

An analytical model of flicker noise for halo implanted MOSFET is presented. The impact of halo regions associated with the device on flicker noise is modeled using a separate MOSFET connected in series with the channel transistor. The model is a significant improvement over existing models in capturing bias and channel length dependencies of noise in devices employing strong halo technology. The model is amenable to be integrated with BSIM6 and provides an excellent solution to model the 1/f noise for the low power CMOS technology with high quality analog capability.

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HARSHIT AGARWAL received the M.Tech. degree from the National Institute of Technology, Hamirpur, India, in 2012. He is currently pursuing the Ph.D. degree with the Nanolab, Department of Electrical Engineering, Indian Institute of Technology Kanpur, Kanpur, India. His research interest includes semiconductor device physics, modeling, and characterization.

SOURABH KHANDELWAL (M'14) received the Ph.D. degree from the Norwegian University of Science and Technology in 2013 and the M.Tech. degree from the Indian Institute of Technology Bombay in 2007. He was a Research Engineer with IBM Semiconductor Research from 2007 to 2010. He is currently a BSIM Program Manager/Post-Doctoral Researcher with the BSIM Group, Department of Electrical Engineering and Computer Science, University of California, Berkeley. His Ph.D. work on GaN compact model named ASM-HEMT model is under consideration for industry standardization at the Compact Model Coalition. He has authored several journal and conference publications in the area of device modeling and characterization.

CHENMING HU (F'03) is the TSMC Distinguished Professor Emeritus with the University of California Berkeley (UC Berkeley), Berkeley, CA, USA. He was the Chief Technology Officer with Taiwan Semiconductor Manufacturing Company. He is a Board Director of SanDisk Inc. and the non-profit Friends of Children with Special Needs. He is well known for his work on the 3-D transistor, FinFET, which can be scaled to single digit nanometers. He has developed widely used integrated circuit (IC) reliability models and led the research of BSIM-the first industry-standard SPICE model used by most IC companies to design CMOS products since 1996. He was a recipient of the IEEE Andrew Grove Award, the Solid State Circuits Award, the Nishizawa Medal, the Kaufman Award of the EDA Industry, the University Research Award of the U.S. Semiconductor Industry Association, the UC Berkeley's Highest Honor for teaching, and the Berkeley Distinguished Teaching Award.

SAGNIK DEY received the Ph.D. degree in electrical engineering from the University of Texas at Austin, Austin, TX, USA, in 2006. He is currently a member-group of technical staff in the Embedded Processor Technology Development at Texas Instruments, Dallas, USA, where he is involved in the development of compact models for CMOS technology nodes. His current research interests include modeling, analysis and characterization of statistical variability, mismatch and noise in advanced technology nodes for analog/RF applications.

YOGESH SINGH CHAUHAN (SM'12) received the Ph.D. degree from the École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, in 2007. He was with IBM Semiconductor Research from 2007 to 2010, the Tokyo Institute of Technology in 2010, and the University of California Berkeley from 2010 to 2012. Since 2012, he has been an Assistant Professor with the Indian Institute of Technology Kanpur, India. His research interests are characterization, modeling, and simulation of advanced semiconductor devices. He was a recipient of prestigious Ramanujan Fellowship from the Government of India in 2012 and the IBM Faculty Award in 2013. He is an Editor of the Institution of Electronics and Telecommunication Engineers Technical Review.