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Junctionless Biristor: A Bistable Resistor Without Chemically Doped P-N Junctions

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ABSTRACT In this paper, using 2-D simulations, we report a novel junction-less biristor in which the emitter and collector regions are created by applying the charge plasma concept on a P-doped silicon film. Since no chemical doping is required, the junction-less biristor can be realized with a low thermal budget. We demonstrate that the junction-less biristor exhibits not only a significant low latch-up voltage (2.0 V) but also has a large latch window (0.66 V) when compared to that of a conventional silicon biristor with similar parameters. The reasons for this improved performance are discussed.

INDEX TERMS Biristor, junction-less, bistable resistor, current gain, SALTran effect.

I. INTRODUCTION

The biristor is an open base n-p-n or p-n-p bipolar junction transistor which exhibits bi-stable current voltage characteristics. Due to high speed and high endurability, it is a greatly suitable candidate for volatile memory applications [1]–[5]. However, the fabrication of a conventional biristor involves creation of two abrupt p-n metallurgical junctions, which needs either ion implantation together with costly ultrafast annealing or a thermal diffusion process [1]–[4], both of which require high thermal budgets.

To use a biristor for memory applications, it is necessary to have a low operating voltage. However, the reported values of latch-up voltages of the conventional silicon biristor are as high as 5 V [1]–[5]. Therefore, it is important to explore different device architectures and concepts (i) for realizing the biristor using a low thermal budget process and (ii) for reducing its operating voltage for low voltage applications. A low thermal budget process makes it possible to realize biristors on non-silicon substrates such as system-on-glass reducing the cost [6]. Recently, it has been shown that the latch voltages of the biristor can be reduced [7] using the SALTran concept [8], [9]. However, the SALTran biristor too requires chemical doping using either ion implantation or thermal diffusion.

In this paper, therefore, we propose a junction-less biristor which does not require chemical doping and also exhibits reduced latch voltages compared to a conventional biristor. In the junction-less biristor, using the charge plasma concept [10]–[22], the "N^+" emitter and "N^+" collector regions are induced on a lightly doped p-type silicon film using metal electrodes of appropriate work function. Using 2-D simulations, we demonstrate that the junction-less biristor exhibits a latch-up voltage of 2.00 V and a latch-down voltage of 1.34 V. We also discuss the reasons for this improved performance.

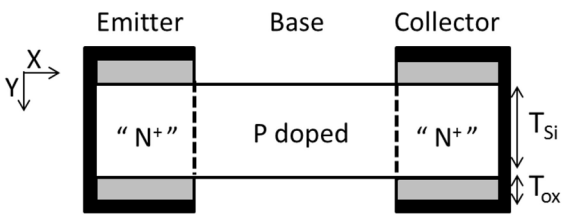

FIGURE 1. Schematic cross section of the junction-less biristor structure.

II. DEVICE STRUCTURE AND SIMULATION PARAMETERS

The cross-sectional view of the junction-less biristor is shown in Fig. 1. The device parameters of the junction-less biristor used for the investigation are as follows: silicon film doping (N_A) = $3 \times 10^{17}/cm^3$, silicon film thickness (T_{si}) = 10 nm, silicon dioxide layer thickness (T_{ox}) = 1 nm, P base width = 150 nm and emitter and collector electrode length = 50 nm. The "N^+" emitter and collector regions are created by inducing electrons in the P doped silicon

film by using hafnium (work function = 3.9 eV) as the metal electrode [10]–[22]. The junction-less biristor can be fabricated on similar lines as that of a FinFET. Although oxide layers are present on either side of the film under the metal electrodes, the device may not suffer from hot carrier injection. This is due to the fact that the metal electrode and the induced "N^+" region are both at the same potential either on the emitter side (0 V) or on the collector side (V_{CE}).

The models used in Atlas device simulation tool [23] include the concentration dependent Shockley–Read–Hall model, trap-assisted tunneling model, Masetti low field mobility model, parallel electric-field-dependent mobility model, energy balance model, Fermi-Dirac carrier statistics and Toyabe non-local impact ionization model. We used the CURVETRACE algorithm to simulate the breakdown phenomenon. In simulations involving snapback and breakdown, this algorithm can automatically switch between voltage and current boundary conditions [23].

As done earlier in [7], the current voltage characteristics of the junction-less biristor are obtained using the Toyabe (non-local) impact ionization model. The electron and hole impact ionization rates α_n and α_p, respectively, are given by:

$$\alpha_n = ANexp\left(-\frac{BN}{E_{eff,n}}\right)$$
$$\alpha_p = APexp\left(-\frac{BP}{E_{eff,p}}\right)$$

where AN = 3.8×10^6/cm, AP = 2.25×10^7/cm, [24] and BN = 1.23×10^6 V/cm, BP = 1.69×10^6 V/cm are the default values from Atlas simulator [23].

III. RESULTS AND DISCUSSION

For the junction-less biristor shown in Fig. 1, the band diagrams are shown in Fig. 2 for (a) thermal equilibrium conditions ($V_{CE} = 0V$), (b) just below the latch-up voltage ($V_{CE} = 1.99V$) and (c) just above the latch-down voltage ($V_{CE} = 1.35V$). In thermal equilibrium ($V_{CE} = 0V$), as shown in Fig. 3(a), the net electron concentration (taken midway through the silicon film) in the emitter and collector is approximately $2.5 \times 10^{18}/cm^3$. The hole concentration in the middle of the base region, $3 \times 10^{17}/cm^3$ and is equal to the P doping of the silicon film. In Fig. 2(b), the band diagram at V_{CE} just below the latch-up voltage (1.99 V) shows a clear reduction in the built-in potential at the emitter-base indicating that this junction is now forward biased. Hence, there is a rise in the minority carrier concentration in the emitter and base regions as shown Fig. 3(b). The emitter-base internal forward bias is still higher at V_{CE} just above the latch-down voltage (1.35 V) as shown in Fig. 2(c) and hence there is a further rise in the minority carrier concentration in both the emitter and base regions as shown in Fig. 3(c). On the other hand, at the collector-base junction as seen in Fig. 2(b) and (c), the applied voltage V_{CE} added with the barrier potential appears as the reverse bias

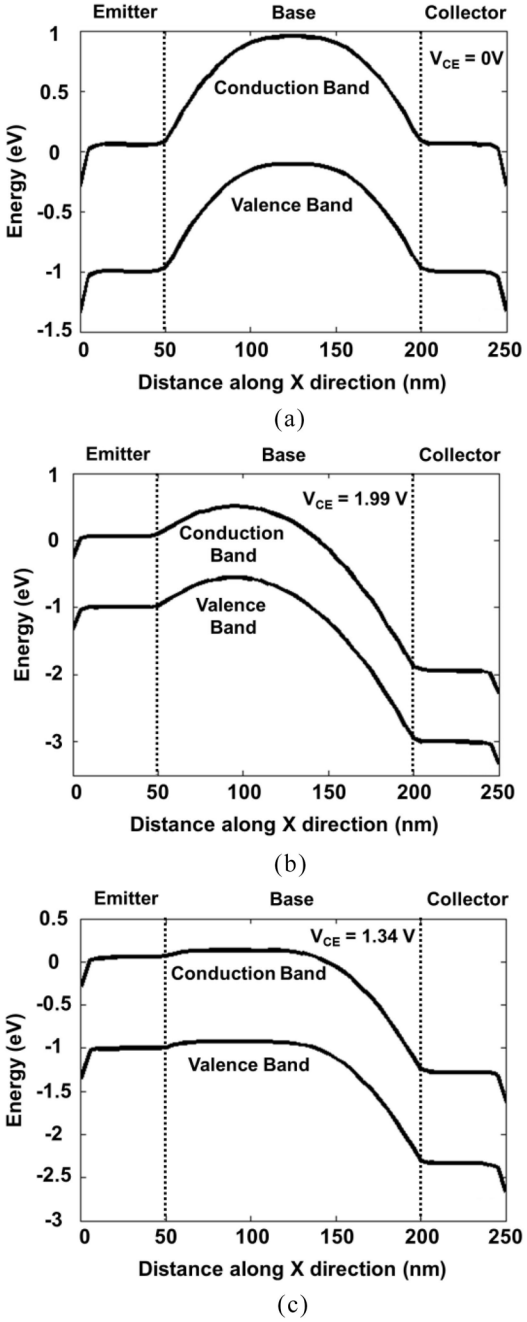

FIGURE 2. Band diagrams across the device taken midway through the film (a) under thermal equilibrium (V_{CE} = 0 V), (b) just below latch-up voltage (V_{CE} = 1.99 V), and (c) just above latch-down voltage (V_{CE} = 1.35 V).

voltage across the collector-base junction and is sufficient to cause significant impact ionization leading to breakdown and hence the electron-hole concentration in the collector region has increased. In Fig. 3(c), where V_{CE} is just above the voltage that is sufficient to suppress the breakdown, the very large number of electrons in the base region is due to the breakdown. Hence, the behaviour of the junction-less biristor is similar to that of the conventional biristor qualitatively.

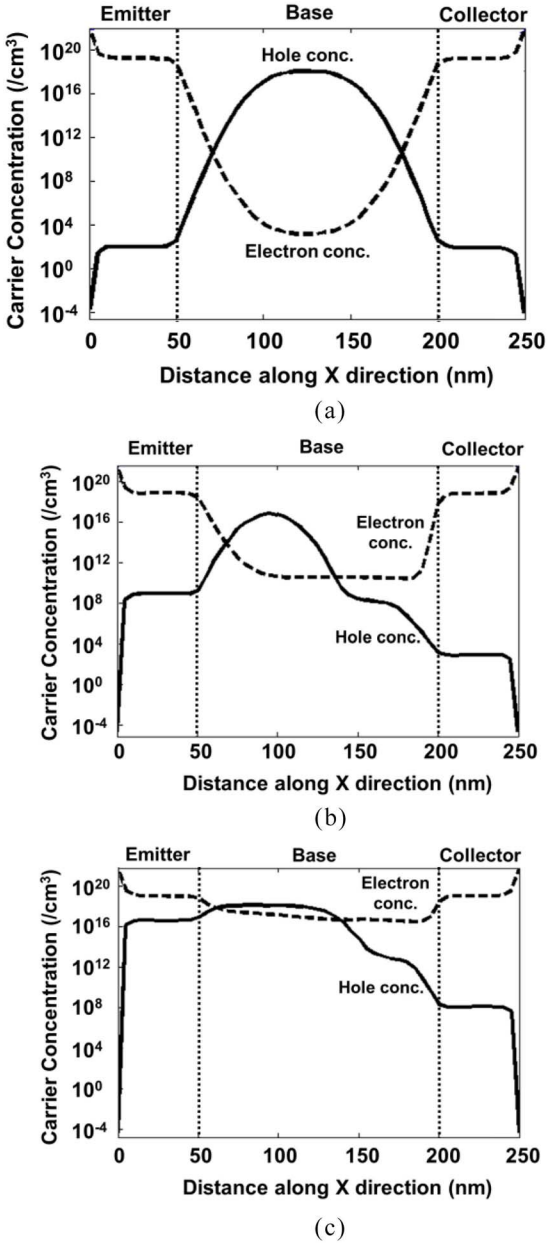

FIGURE 3. **Electron and hole carrier concentration profiles across the device taken midway through the film (a) under thermal equilibrium ($V_{CE} = 0$ V), (b) just below latch-up voltage ($V_{CE} = 1.99$ V), and (c) just above latch-down voltage ($V_{CE} = 1.35$ V).**

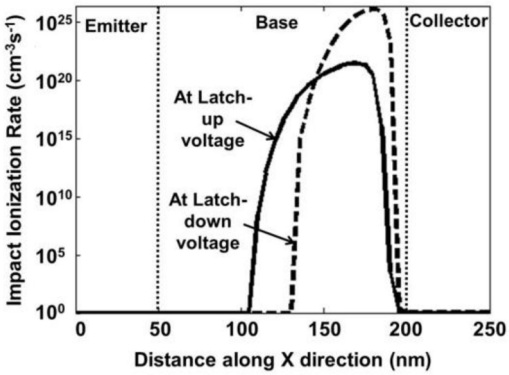

FIGURE 4. **Impact ionization rate midway through the film at latch-up (before breakdown) and latch-down (before the suppression of breakdown) voltages, $V_{LU} = 2.00$ V and $V_{LD} = 1.34$ V, respectively.**

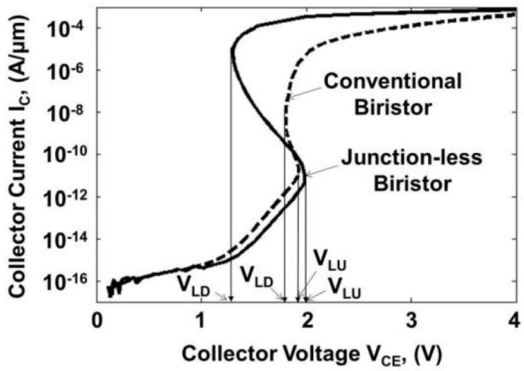

FIGURE 5. **$I_C - V_{CE}$ characteristics of the proposed junction-less biristor ($V_{LU} = 2.00$ V and $V_{LD} = 1.34$ V) compared with that of the conventional biristor.**

The impact ionization plot in Fig. 4 shows that the peak value of impact ionization (of the order of 10^{21} $cm^{-3}s^{-1}$) is higher than that of a conventional biristor by at least two orders of magnitude [7]. Such a high value of impact ionization rate in the junction-less biristor is due to the enhancement of current gain caused by the SALTran effect [8], [9]. It has been reported earlier [12]–[15] that transistors implemented using the charge plasma concept demonstrated a significantly higher current gain compared to their conventional counterparts due to the SALTran effect. We, therefore, first discuss the SALTran effect briefly before studying the I_C-V_{CE} characteristics of the junction-less biristor.

The SALTran effect can be observed when a metal with a work function lower than that of the n-type emitter is used at the emitter contact. The transfer of electrons from the metal into the semiconductor results in a surface accumulation of electrons in the semiconductor near the metal-semiconductor interface. The concentration gradient of this accumulated electrons is such that the resultant induced electric field at the metal-emitter contact opposes the flow of holes entering from the base region into the emitter region, which results in the reduction of base current and hence an enhancement in the current gain [12]–[15]. The SALTran effect has been successfully employed in [7] to reduce the operating voltage of the silicon biristor. Utilising the same effect, we demonstrate that the proposed junction-less biristor is capable of working at a lower operating voltage than the conventional biristor [1]–[5]. The I_C-V_{CE} characteristics of the junction-less biristor and the compatible conventional biristor with the emitter and collector regions doped with $N_D = 1 \times 10^{20}/cm^3$ are shown in Fig. 5. We observe that the junction-less biristor exhibits a latch window as high as 0.66 V and a latch-up voltage V_{LU} of 2.00 V and

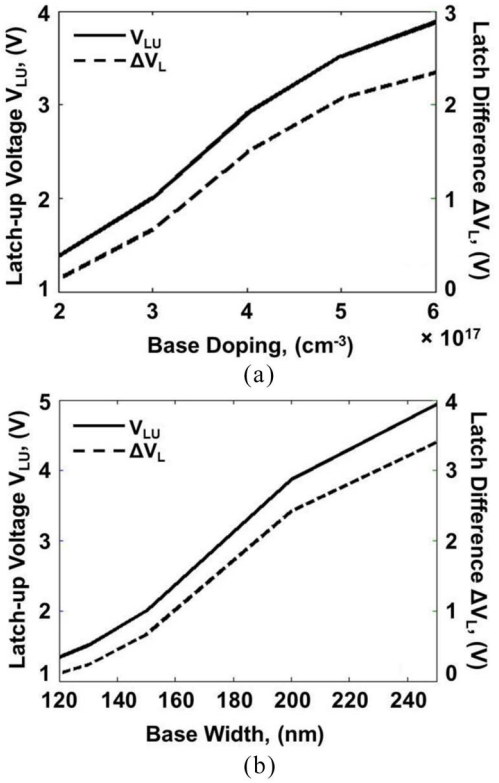

FIGURE 6. **Variation of latch-up voltage (V_{LU}) and latch difference (ΔV_L) with (a) base doping for base width = 150 nm and (b) base width for base doping = $3 \times 10^{17}/cm^3$.**

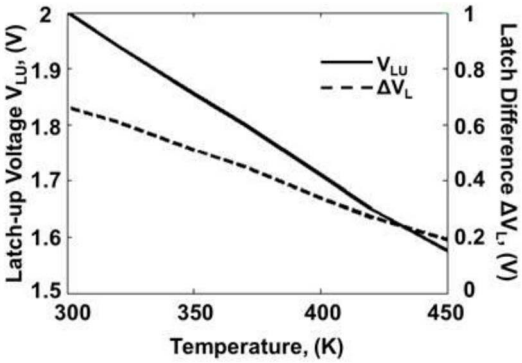

FIGURE 7. **Variation of latch-up voltage (V_{LU}) and latch difference (ΔV_L) with temperature.**

a latch-down voltage V_{LD} of 1.34 V, both lower than that of any reported silicon biristor. However, the latch window of the conventional biristor is too low (0.08 V) making it unusable.

The choice of the base doping and the base width will determine the latch voltages and the latch difference of the biristor [1], [2], [5], [7]. The variation of these parameters for the junction-less biristor is shown in Fig. 6 which indicates that further reduction in the latch-up voltage is possible, by reducing either the P-base doping or the base width but with a degraded latch window. However, while optimizing the base width and base doping, care needs to be taken to avoid base punchthrough. Otherwise, the latch characteristics will disappear as demonstrated in [1]. Fig. 7 shows that the latch difference (ΔV_L) of the junction-less biristor decreases with temperature just as in the case of the conventional biristor [2]. This is due to an increase in the current gain at higher temperatures. However, the junction-less biristor can be used with a reasonable latch window up to 400 K.

IV. CONCLUSION

In this work, using 2-D simulations, we have demonstrated the possibility of realizing a biristor without the need for creating chemically doped metallurgical junctions. By using metal electrodes of suitable work function on the two sides of a P-doped silicon film, the junction-less biristor can be realized with very low thermal budgets. The proposed junction-less biristor not only exhibits a latch-up voltage of 2 V but also has a reasonably high latch window of 0.66 V which is significantly higher than that of a compatible conventional silicon biristor. Our results may provide the incentive for further experimental study and analysis of the junction-less biristor.

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