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TFET-Based Circuit Design Using the Transconductance Generation Efficiency g_m/I_d Method

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ABSTRACT Tunnel field effect transistors (TFETs) have emerged as one of the most promising post-CMOS transistor technologies. In this paper, we: 1) review the perspectives of such devices for low-power high-frequency analog integrated circuit applications (e.g., GHz operation with sub-0.1 mW power consumption); 2) discuss and employ a compact TFET device model in the context of the g_m/I_d integrated analog circuit design methodology; and 3) compare several proposed TFET technologies for such applications. The advantages of TFETs arise since these devices can operate in the sub-threshold region with larger transconductance-to-current ratio than traditional FETs, which is due to the current turn-on mechanism being interband tunneling rather than thermionic emission. Starting from technology computer-aided design and/or analytical models for Si-FinFETs, graphene nano-ribbon (GNR) TFETs and InAs/GaSb TFETs at the 15-nm gate-length node, as well as InAs double-gate TFETs at the 20-nm gate-length node, we conclude that GNR TFETs might promise larger bandwidths at low-voltage drives due to their high current densities in the sub-threshold region. Based on this analysis and on theoretically predicted properties, GNR TFETs are identified as one of the most attractive field effect transistor technologies proposed-to-date for ultra-low power analog applications.

INDEX TERMS Si-FinFETs, tunnel field effect transistors (TFET), ultra-low power design, g_m/I_d method, one-stage common-source amplifier, two-stage operational transconductance amplifier (OTA) with Miller effect compensation.

I. INTRODUCTION

Since its early proposals, the perspectives of Tunnel Field Effect Transistors (TFETs) for low-power digital circuits, have been widely studied [1]. However, the benefits of employing these devices in analog applications, besides the possibility of operating at low V_{DD} voltages, i.e., $V_{DD} < 0.1$V, due to their sub 60 mV/decade subthreshold slope, have remained largely unexplored until recently [2]. Low power circuit design often requires transistors to operate in the region where they are more efficient as generators of transconductance hence bandwidth, i.e., in the subthreshold region [3]. In this region, a key parameter for analog IC designers is the transconductance-to-drain-current ratio (from herein g_m/I_d) [4], which might be interpreted as a measure of transconductance generation efficiency. In traditional FETs the g_m/I_d ratio is theoretically limited to values below 38.5 V^{-1}. This value corresponds to $1/nU_t$, where n is the subthreshold slope factor, and U_t is the thermal voltage. The subthreshold swing SS and the g_m/I_d ratio are related by [5]:

$$\frac{g_m}{I_d} = \frac{\text{Ln}(10)}{SS}. \tag{1}$$

At room temperature a 60 mV/decade subthreshold swing corresponds to a g_m/I_d ratio of 38.5 V^{-1}. Due to the possibility of achieving subthreshold swings below 60 mV/decade [5], TFETs can outperform traditional FETs

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in transconductance generation efficiency, promising g_m/I_d values well above 100 V^{-1} (i.e., higher transconductance per bias current than traditional FETs). In this work: *(i)* we review the application of the g_m/I_d integrated circuit design methodology [4] to circuits containing TFETs in order to predict the performance of these transistors for low power and high-frequency analog applications. In this context is worth mentioning that the g_m/I_d method has previously been successfully extended to transistor technologies other than traditional FETs, such as Piezoelectric Oxide Semiconductor FETs [6]. Also, *(ii)* we discuss and employ -in the context of the g_m/I_d method- a recently proposed compact TFET device model, which is valid in all the device biasing space [7], [8]. From this model, employing a limit analysis, *(iii)* we derive a new single-piece analytical expression capable of representing g_m/I_d as a function of the bias voltage, which can benefit future compact model device representations. As case studies, we consider two circuit topologies: *i)* a one-stage common-source amplifier, and *ii)* a two-stage operational transconductance amplifier (OTA) with Miller effect compensation [4]. At the 20-nm channel length node: (a) InAs DG TFET; and at the 15-nm gate length node: (b) GNR nano-ribbon TFET, (c) InAs/GaSb nano-wire TFET, and (d) Si-FinFET are analyzed and compared. We discuss the circuit performance, and, in which way the g_m/I_d methodology encompasses a number of interrelated circuit features.

Analog IC designers often employ a wide range of well-established methodologies and equations as a guide for highly-efficient optimal circuit design. These methodologies should comprise a broad set of tools like: analytical equations and simplified device models, to guide the designers towards the study of the circuit dynamics and an understanding of its tradeoffs, therefore allowing designers to formulate design criteria to obtain optimum system on-a-chip implementations. Furthermore, design methodologies and design approaches must provide designer-reconfigurability in order to reduce re-engineering efforts when incorporating minor changes to the integrated circuits. Until now, comparisons between different TFET technologies have been addressed in the literature, pointing out their advantages and peculiarities. However, the above mentioned desired design features, have not yet been taken into account. For instance Trivedi *et al.* [5] analyzed potentials and challenges of implementing ultra-low power analog circuits based on TFETs in the context of an Operational Transconductance Amplifier (OTA) design for implantable biomedical applications. The design and circuit performance were analyzed by using Technology CAD (TCAD). Although the benefits of the subthreshold properties of TFETs were identified and discussed, the design was not implemented by using compact device models and low-power oriented circuit design methodologies as we employ and discuss in this work. Liu *et al.* [9] discussed the design of an III-V Heterojunction HTFET (HTFET)-based neural amplifier employing a telescopic operational transconductance amplifier (OTA). The design was performed by means of a calibrated Verilog-A device model incorporating electrical noise.

In terms of TFET device models, Zhang and Chan [10] introduced a SPICE model based on a closed-form current representation by means of analytical electrostatic potential solutions. The same group also presented a compact device model in Verilog-A for public use [11]. From a low-power analog circuit-designer perspective, Sensale-Rodriguez *et al.* [12] introduced the transconductance-to-drain-current ratio (g_m/I_d) methodology in the context of TFETs.

This work improves our previous work [12]; first of all, because we show that the g_m/I_d method may be used in conjunction with compact device models valid in all the device biasing space, providing thus well-known tools for circuit designers. Secondly, the performance of a wider set of technologies is compared. In addition, we derive for the first time a compact equation that allows to estimate the minimum sub-threshold swing (or maximum g_m/I_d) based on a semi-empirical compact physics based model.

This article is organized as follows: Section II discusses the g_m/I_d method. Based on a semi-empirical compact physics based model [7], [8], Section III discusses how g_m/I_d can be continuously estimated as a function of the bias voltage in all the device bias design-space. From a limit-analysis analytical expressions for the minimum sub-threshold swing (or maximum g_m/I_d) are estimated. Section IV discusses the design of two circuit topologies: i) a one-stage common-source amplifier, and ii) a two-stage OTA with Miller effect compensation for four TFET device technologies. The g_m/I_d method is used to i) achieve the circuit design specifications and ii) to assure the selection of the best TFET technology. The article concludes with a brief summary and discussion.

II. g_m/I_d INTEGRATED CIRCUIT DESIGN METHOD APPLIED TO TFETs

As pointed out in [13]–[15], established design methodologies and tools as well as compact equations representing the device response in all the biasing design space are often required by analog IC designers as a guide for performing optimal circuit design. Here we discuss the g_m/I_d method and a compact device-model as some of such tools enabling TFET-based analog circuit design.

The g_m/I_d method can provide a criterion that assures the selection of the best TFET technologies as well as the most appropriate biasing schemes to achieve a set of desired functional features. Moreover, several design difficulties might be circumvented by employing the g_m/I_d integrated circuit design methodology. Following, we discuss the peculiarities of TFETs and why this design methodology can be employed for these devices. For this purpose, we recall here a well-known n+(source)/i(channel)/p+(drain) p-TFET structure from the literature. A schematic of the device cross section is depicted in Fig. 1(a). The pair of energy band diagrams shown in Fig. 1(b) illustrates its

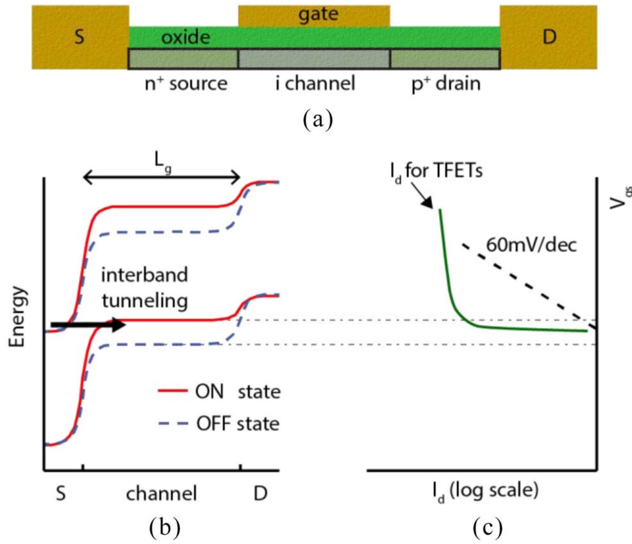

FIGURE 1. TFET operation. (a) Cross sectional representation of a *p*-type TFET. (b) Band diagram in ON and OFF state. (c) *I-V* characteristic of the device.

operation principle: with zero volts applied between gate and source (dashed lines) the transistor is off, the channel is fully-depleted so that tunneling from source to channel is prohibited. When a negative voltage is applied to the gate (continuous lines) electrons can tunnel from source to channel, which leads to a net drain current. In contrast with traditional FETs, where the turn-on mechanism is thermionic emission and, therefore, the subthreshold swing is limited to > 60 mV/decade, the current turn-on mechanism of TFETs is inter-band tunneling allowing thus subthreshold swing values below 60 mV/decade.

To introduce the g_m/I_d method, the approach we adopt in this work is to use the physics-based compact analytical model developed by Lu *et al.* [7], [8]. In accordance with this model, the TFET tunnel drain current is of the form:

$$I_d = a\, f(\cdot)\; V_{TW}\; \xi\; \exp\left(-\frac{b}{\xi}\right), \tag{2}$$

where a and b are coefficients that depend on the material properties, and f (.) is a function capable of smoothly connecting the subthreshold and above-threshold operation regions. Moreover, V_{TW} is the tunneling window voltage and ξ is the average electrical field. All of these parameters, with the exception of the coefficients a and b, are dependent on V_{GS} and V_{DS}. This model is very useful because: *i)* it is given by a continuous equation capable of representing the TFET operation in the subthreshold as well as above-threshold regions; and *ii)* it uses few adjustable parameters, which are strongly linked to the device-physics, device geometry, and materials structure of the TFET as well as with the device fabrication process (i.e., the model is physics based, but it requires device characterization and parameter fitting).

By using this physics-based compact model it is possible to employ the g_m/I_d methodology to design analog circuits that are based on TFET devices; which is a result of I_d being linearly proportional to the TFET width W. In (2) the coefficient a is given by:

$$a = \frac{W t_{ch} q^3}{8\pi^2\hbar^2}\sqrt{\frac{2m_{eff,R}}{E_G}}, \tag{3}$$

where W is the TFET width, t_{ch} is the channel thickness, E_G is the semiconductor band gap, and $m_{eff,R}$ is the electron reduced effective mass. One should notice that it is possible to write (2) in a general form as follows:

$$I_d = W\psi\,(V_{GS}, V_{DS}) \tag{4}$$

where ψ(.) expresses the general dependence of current on the bias point voltage (V_{GS} and V_{DS}). On the other hand:

$$g_m = \left[\frac{\partial I_d}{\partial V_{GS}}\right]_{V_{GS},V_{DS}}. \tag{5}$$

Then, g_m/I_d is calculated as follows:

$$\frac{g_m}{I_d} = \frac{1}{\psi(.)}\left[\frac{\partial\psi(.)}{\partial V_{GS}}\right]_{V_{GS},V_{DS}} = \left[\frac{\partial \mathrm{Ln}\psi(.)}{\partial V_{GS}}\right]_{V_{GS},V_{DS}}, \tag{6}$$

since:

$$\frac{g_m}{I_d} = \frac{1}{I_d/W}\left[\frac{\partial I_d/W}{\partial V_{GS}}\right]_{V_{GS},V_{DS}} = \left[\frac{\partial \mathrm{Ln}(I_d/W)}{\partial V_{GS}}\right]_{V_{GS},V_{DS}}. \tag{7}$$

From the above discussion, one can observe that the g_m/I_d versus I_d/W curve can be considered a technology-characteristic as well as a function of V_{GS} and V_{DS} (bias point). For this reason, it is possible to extract this curve from either TFET simulations or from device measurements, and therefore employ the g_m/I_d method as it is traditionally done for circuit design based on CMOS transistors [4].

III. TRANSCONDUCTANCE GENERATION EFFICIENCY

In the literature it is often discussed that TFETs can outperform traditional FETs in transconductance generation efficiency, promising g_m/I_d values well above 100 V^{-1}. Such affirmation is based either on numerical simulations performed by employing TCAD or on theoretical estimations. Nevertheless, from a circuit-design perspective, it is necessary to: *i)* have a compact equation, valid in all the transistor operation regions describing how g_m/I_d depends on bias, and *ii)* estimate the maximum g_m/I_d values attainable in each TFET device technology. To perform this, we will continue employing the model developed in [7] and [8], which is a compact semi-empirical model, because to the best of our knowledge it is the only model proposed so far that is capable of expressing g_m/I_d in a compact single-piece equation.

This section is then devoted to analytically estimate g_m/I_d and its maximum value $(g_m/I_d)_{MAX}$, which is calculated from the following limit:

$$\left(\frac{g_m}{I_d}\right)_{MAX} = \mathrm{Lim}_{V_{GS}\to V_{OFF}}\left(\frac{g_m}{I_d}\right), \tag{8}$$

where V_{OFF} is the minimum valid gate-source voltage for which the model given by (2) is valid [7], [8]. The tunnel drain current for $V_{GS} > V_{OFF}$ is given by (2) from where the following expression can be obtained for g_m/I_d:

$$\frac{g_m}{I_d} = \left[\frac{\partial \mathrm{Ln}\left(af(.)V_{TW}\xi \exp\left(-\frac{b}{\xi}\right)\right)}{\partial V_{GS}} \right]_{V_{GS},V_{DS}}. \quad (9)$$

The derivatives will be evaluated at a given bias point (V_{GS}, V_{DS}). From herein, this will not be mentioned anymore in the following discussion in order to avoid overwhelmed notation. Equation (9) results in:

$$\frac{g_m}{I_d} = \frac{1}{f}\frac{\partial f}{\partial V_{GS}} + \frac{1}{V_{TW}}\frac{\partial V_{TW}}{\partial V_{GS}} + \frac{1}{\xi}\frac{\partial \xi}{\partial V_{GS}} + \frac{b}{\xi^2}\frac{\partial \xi}{\partial V_{GS}}, \quad (10)$$

where each function and parameter are technology-specific as mentioned in Section II. In the following subsections, we will calculate all terms in (10) by determining each derivative.

A. FIRST TERM: FUNCTION F (.) AND ITS DERIVATIVE

By using the expression for f (.) given in [7]:

$$f(.) = \frac{1-\exp\left(-\frac{V_{DS}}{\Gamma}\right)}{1+\exp\left(\frac{\lambda \tanh(V_{GS}-V_{OFF})-V_{DS}}{\Gamma}\right)}, \quad (11)$$

we determine that:

$$\mathrm{Lim}_{V_{GS}\to V_{OFF}}\, f(.) = \tanh\left(-\frac{V_{DS}}{2\Gamma}\right), \quad (12)$$

where Γ is an adjustable parameter [7], [8]. Therefore, the derivative of f (.) can be expressed as follows:

$$\frac{\partial f(.)}{\partial V_{GS}} = \frac{\left(1-\exp\left(-\frac{V_{DS}}{\Gamma}\right)\right)\exp\left(\frac{\lambda \tanh(V_{GS}-V_{OFF})-V_{DS}}{\Gamma}\right)\left(1-\tanh^2(V_{GS}-V_{OFF})\right)}{\left[1+\exp\left(\frac{\lambda \tanh(V_{GS}-V_{OFF})-V_{DS}}{\Gamma}\right)\right]^2}\frac{\lambda}{\Gamma} \quad (13)$$

where λ is another adjustable parameter [7], [8]. After performing the limit when $V_{GS} \to V_{OFF}$, it results that:

$$\mathrm{Lim}_{V_{GS}\to V_{OFF}}\frac{\partial f(.)}{\partial V_{GS}} = \frac{\left(1-\exp\left(-\frac{V_{DS}}{\Gamma}\right)\right)\exp\left(-\frac{V_{DS}}{\Gamma}\right)}{\left[1+\exp\left(-\frac{V_{DS}}{\Gamma}\right)\right]^2}\frac{\lambda}{\Gamma}. \quad (14)$$

B. THRESHOLD TUNNELING WINDOW VOLTAGE V_{TW} AND ITS DERIVATIVE

The tunneling window V_{TW}, is defined as follows [7], [8]:

$$V_{TW} = U\ \mathrm{Ln}\left[1+\exp\left(\frac{V_{GS}-V_{TH}}{U}\right)\right], \quad (15)$$

where U is the Urbach factor and V_{TH} is the threshold voltage. From (15) it results:

$$\mathrm{Lim}_{V_{GS}\to V_{OFF}} V_{TW} = \gamma_0 U_0 \mathrm{Ln}\left[1+\exp\left(\frac{V_{OFF}-V_{TH}}{\gamma_0 U_0}\right)\right], \quad (16)$$

where γ_0 is the parameter that controls the closing velocity of the tunneling window with gate bias and $U_0 = nKT/q$ with n being the subthreshold ideality factor [7], [8]. On (15) derivation gives:

$$\frac{\partial V_{TW}}{\partial V_{GS}} = \frac{\partial U}{\partial V_{GS}}\mathrm{Ln}\left[1+\exp\left(\frac{V_{GS}-V_{TH}}{U}\right)\right] + U\frac{\partial\left(\mathrm{Ln}\left[1+\exp\left(\frac{V_{GS}-V_{TH}}{U}\right)\right]\right)}{\partial V_{GS}}. \quad (17)$$

Moreover, it can be noticed that:

$$\frac{\partial U}{\partial V_{GS}} = \frac{1-\gamma_0}{V_{TH}-V_{OFF}}U_0, \quad (18)$$

and:

$$\frac{\partial\left(\mathrm{Ln}\left[1+\exp\left(\frac{V_{GS}-V_{TH}}{U}\right)\right]\right)}{\partial V_{GS}} = \frac{\exp\left(\frac{V_{GS}-V_{TH}}{U}\right)}{1+\exp\left(\frac{V_{GS}-V_{TH}}{U}\right)}\frac{U-(V_{GS}-V_{TH})\frac{1-\gamma_0}{V_{TH}-V_{OFF}}U_0}{U^2}. \quad (19)$$

Therefore,

$$\mathrm{Lim}_{V_{GS}\to V_{OFF}}\left(\frac{\partial V_{TW}}{\partial V_{GS}}\right) = \frac{(1-\gamma_0)U_0\mathrm{Ln}\left[1+\exp\left(\frac{V_{OFF}-V_{TH}}{\gamma_0 U_0}\right)\right]}{V_{TH}-V_{OFF}} + \frac{\exp\left(\frac{V_{OFF}-V_{TH}}{\gamma_0 U_0}\right)}{\left[1+\exp\left(\frac{V_{OFF}-V_{TH}}{\gamma_0 U_0}\right)\right]\gamma_0^2}. \quad (20)$$

C. AVERAGE ELECTRIC FIELD ξ AND ITS DERIVATIVE

The average electric field model given in [7] and [8] holds:

$$\mathrm{Lim}_{V_{GS}\to V_{OFF}}\xi = \xi_0(1+\gamma_1 V_{DS}+\gamma_2 V_{OFF}), \quad (21)$$

where the parameters γ_1 and γ_2 are adjustable parameters and ξ_0 is the built-in electric field at the source channel tunnel junction at zero bias. Therefore, its derivative is given by:

$$\mathrm{Lim}_{V_{GS}\to V_{OFF}}\left(\frac{\partial \xi}{\partial V_{GS}}\right) = \xi_0\gamma_2. \quad (22)$$

D. g_m/I_d MODEL

Therefore, from (14), (20), and (22), we have all the terms required in (10) in order to estimate the $(g_m/I_d)_{MAX}$ value as defined by (8). To do this, for some particular TFET technologies, we will use the parameter values given in [7], which we list for convenience in Table 1.

TABLE 1. Summary of parameters from [7].

Parameter	InAs DG TFET	AlGaSb/InAs TFET
Γ(V)	0.06	0.046
γ_0	0.5	0.2
γ_1 (V^{-1})	0.01	0.1
γ_2 (V^{-1})	1.3	0.9
ξ_0 (MV/cm)	0.527	1
λ(V)	0.19	0.32
N	1.8	1.2
V_{OFF} (V)	0.01	0
V_{TH} (V)	0.17	0.08

Table 2 lists examples of $(g_m/I_d)_{MAX}$ for $V_{DS} = 0.1$V and $V_{DS} = 0.5$V for InAs DG TFET and AlGaSb/InAs TFET technologies.

TABLE 2. Obtained $(g_m/I_d)_{MAX}$ values from (8) with parameter values from [7].

TFET Device	V_{DS}=0.1V	V_{DS}=0.5V
InAs DG TFET	174 V^{-1}	178 V^{-1}
AlGaSb/InAs TFET	4056 V^{-1}	4057 V^{-1}

As can be noticed in Table 2, the AlGaSb/InAs technology might deliver larger $(g_m/I_d)_{MAX}$ values than the InAs DG technology. Moreover, it is noteworthy observing that GNR-TFET technologies might offer even higher values than these two-technologies. For instance, in [16] it is calculated a subthreshold swing of 0.19 mV/decade for $V_{DS} = 0.1$V, which, by using (1) results in $(g_m/I_d)_{MAX} = 12119$ V^{-1}. Such large values have advantages from a circuit design perspective and we will elaborate about this in Section IV.

Since the model is valid for $V_{GS} > V_{OFF}$, the estimated $(g_m/I_d)_{MAX}$ corresponds to the maximum of g_m/I_d in this voltage range; i.e., the model does not contemplate what happens for $V_{GS} < V_{OFF}$. However, for most applications, it might not be required to bias the device at such extremely reduced voltages. It should still be noticed that there is a numerical singularity when $V_{TH} = V_{OFF}$. From this point of view, precise numerical procedures to obtain reliable data in order to fit numerical simulations to models must be developed. Although theoretically TFETs might achieve very large g_m/I_d values, real constructive physical limitations including gate leakage, thermionic emission over the source-drain built-in potential, and so on, will practically result in lower g_m/I_d values and this issue should be a topic for intensive further future research.

IV. CIRCUIT DESIGN EXAMPLES

In this section, we analyze the design of two circuit topologies: *i)* a one-stage common-source amplifier, and *ii)* a two-stage OTA with Miller effect compensation, using the g_m/I_d method [4]. This analysis improves our previous work [12] since a wider set of technologies and a wider set of device models are studied. Several proposed TFET technologies are analyzed: at the 20-nm channel length node: (a) InAs DG TFET, and at the 15-nm gate length node: (b) GNR nano-ribbon TFET, (c) InAs/GaSb nano-wire TFET, and (d) Si-FinFET. We compare and discuss the circuit performance and in which way the g_m/I_d method encompasses a number of interrelated circuit features. Table 3 summarizes the analyzed TFET device geometries and the methods from where its I-V characteristics are obtained.

TABLE 3. Summary of TFET devices.

TFET Device	Geometry	Model
Si-FinFETs	15-nm gate length	Simulated employing curves extracted from [17].
GNR TFET	15-nm gate length, ribbon width of 2-nm, 0.5-nm (EOT).	Simulated employing curves extracted from the analytical method from [16].
InAs/GaSb nanowire TFETs	15-nm gate length, 3.5-nm diameter, 0.6-nm (EOT).	Simulated based on equations from the compact analytic model from [7-8], parameters extracted from TCAD simulations.
InAs DG TFET	20-nm gate length, 1-um width, 5-nm tch	Simulated based on equations from the compact analytic model from [7-8], parameters extracted from TCAD simulations.

The 15-nm gate length GNR TFETs were simulated employing an analytical method as reported in [16], with ribbon width of 2 nm, and 0.5 nm equivalent-oxide thickness (EOT). InAs/GaSb nanowire and InAs double-gate TFETs with 15-nm gate length, were simulated using Synopsis TCAD [7], [12], and modeled employing the analytical model proposed in [7] and [8]. Fig. 2 shows that, in analogy to traditional FETs, for a fixed V_{GS}, the g_m/I_d ratio only weakly depends on V_{DS}, i.e., it varies less than 10% for a given I_d/W; this allows for the use of the g_m/I_d design method as in [4] and [18]. Although g_m/I_d vs. V_{DS} and I_d/W is just depicted for the GNR TFET and the InAs DG TFET, the same phenomena was observed in the Si FinFETs as well as in the InAs/GaSb nanowire TFETs. Therefore, V_{DS} will be considered as fixed such that I_d depends only on V_{GS} (allowing saturation), unless otherwise noted. In all the following design examples: for a certain *GBW* (gain-bandwidth product) design target, current consumption will be minimized by using the g_m/I_d circuit design method.

Shown in Fig. 3 is the g_m/I_d ratio as function of current per unit width I_d/W for the four analyzed transistor technologies. The GNR TFETs provide superior current drive relative to the other TFET technologies due to its intrinsic 1D transport and narrow bandgap [16]. Moreover, Fig. 3 also shows that

the current densities of the GNR TFETs for a given g_m/I_d ratio are always larger than those attainable in the Si FinFET.

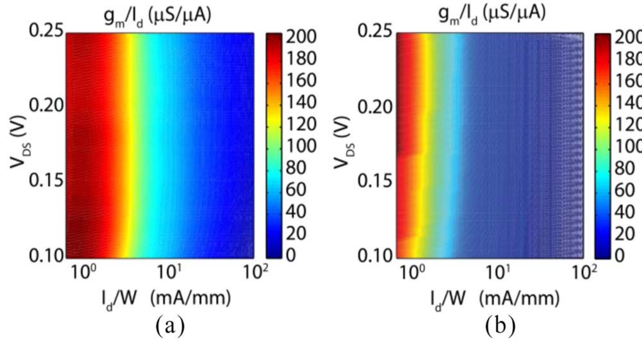

FIGURE 2. False-color plot of g_m/I_d versus V_{DS} and I_d/W for (a) GNR TFET and (b) InAs TFET.

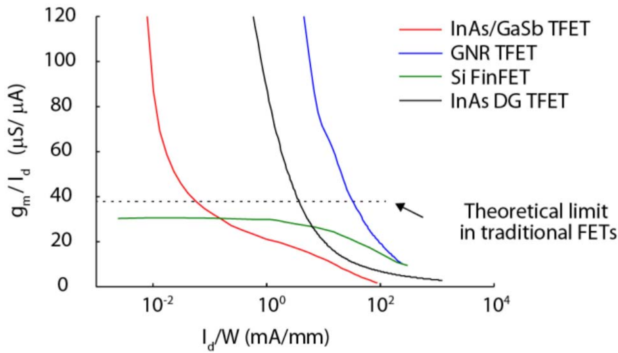

FIGURE 3. g_m/I_d versus I_d/W for the analyzed transistor technologies.

A. ONE-STAGE COMMON-SOURCE AMPLIFIER

Shown in Fig. 4(a) is the schematic of a one-stage common-source amplifier (common source amplifier with active and capacitive load C_L -see [18]). In this configuration, the current consumption, as a function of the transistor g_m/I_d, can be expressed as:

$$I_d = \frac{2\pi \; GBW \; C_L}{\frac{g_m}{I_d} - \frac{2\pi \; GBW \; C_{d0}}{I_d/W}}, \tag{23}$$

where the gain-bandwidth product (GBW) and C_L are set by the design requirements, and I_d/W and C_{d0} are functions of g_m/I_d as shown in Figs. 3 and 4(b). C_d is defined as the capacitance seen from the transistor drain to ground in the absence of load capacitance. $C_{d0} = C_d/W = (C_{gd}+C_{bd})/W$ in traditional FETs, where C_{bd} is the bulk-to-drain capacitance and approximately equal to C_{gd0} in TFETs, with C_{gd0} being the gate-to-drain capacitance per unit width. Note that C_{gd} is added to C_{bd} since the transistor gain is large enough. The circuit current consumption is proportional to the load capacitance as seen in (23). Therefore, although in all the following discussion a 1pF load capacitance will be assumed, the conclusions drawn from our analysis are general enough and independent of the particular choice of load capacitance. Besides scaling linearly with C_L, the circuit current consumption depends on g_m/I_d as seen in (23). To minimize current consumption for a given GBW, the denominator of (23), which is independent of C_L, needs to be maximized. Therefore g_m/I_d should be set, in principle, as high as possible. However, driving the parasitic capacitances requires a certain current consumption for every g_m/I_d, which increase as g_m/I_d increases, as shown in Fig. 4(b). From this point of view, for certain GBW design targets, there is an optimal g_m/I_d that delivers the minimum circuit current consumption. When comparing the current consumption in one-stage common-source amplifiers, it is observed that for low GBW design targets, e.g., 10 MHz, all the TFET technologies promise lower current consumption than the FinFET as depicted in Fig. 4(c). This is due to the possibility of biasing TFETs with very large g_m/I_d above 38.5V^{-1}. From this point of view, under low GBW constraints, the optimal g_m/I_d that delivers the minimum circuit current consumption is the largest g_m/I_d attainable on each technology, and thus the most power efficient technologies are the ones achieving the largest $(g_m/I_d)_{MAX}$.

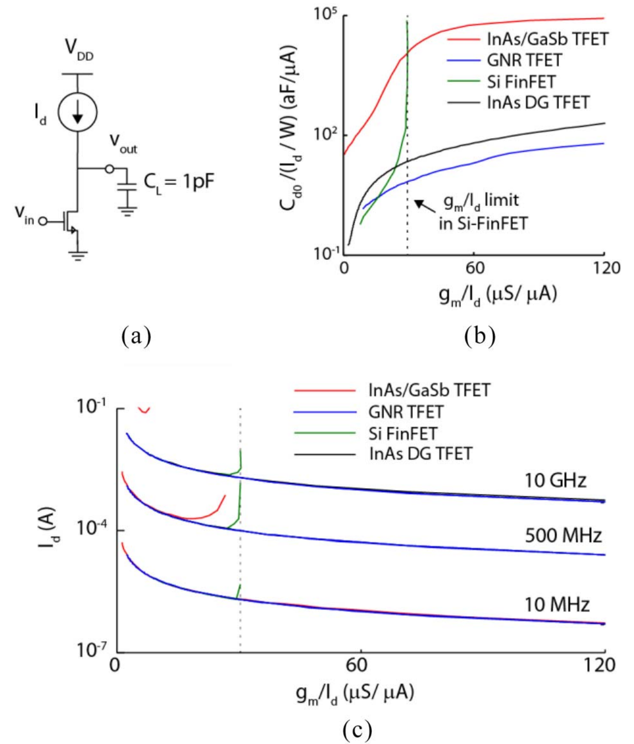

FIGURE 4. (a) Schematic of a one-stage common-source amplifier. (b) $C_{d0}/(I_d/W)$ versus g_m/I_d. (c) Current consumption versus g_m/I_d for different GBW design targets.

As shown in Fig. 4(c), the current consumption increases with increasing GBW. For GBW above 10 GHz, the key to minimize current consumption is to employ a technology with high g_m/I_d while keeping $C_{d0}/(I_d/W)$ as low as possible as dictated by the denominator of (23), and as above discussed. To this end, we plot $C_{d0}/(I_d/W)$ vs. g_m/I_d in Fig. 4(b) for the four analyzed transistor technologies; the advantages of the GNR TFET becomes clearly evident.

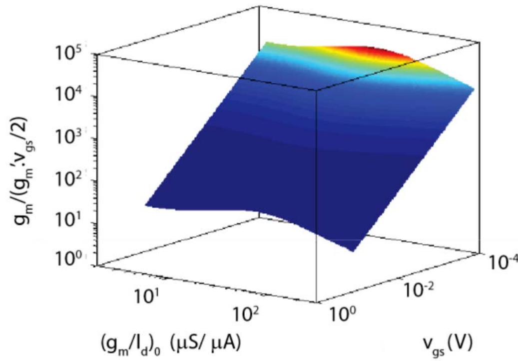

FIGURE 5. $g_m/(V_{GS}.g_m'/2)$ **as a function of the amplitude of the incremental change in gate-to-source voltage (**V_{GS}**) and (**g_m/I_d**)**$_0$ **for an InAs DG TFET.**

In this case, for a given g_m/I_d, because of the larger attainable I_d/W in the GNR TFET, the second term in the denominator of (23) is the smallest for GNR TFETs even though TFETs tend to have higher C_{gd0} than conventional FETs [19]. For InAs DG TFETs it is observed in Fig. 3 a lower current thus larger $C_{d0}/(I_d/W)$ than that in GNR TFETs, therefore, current consumption results slightly larger. In addition, due to their superior current drives (I_d/W) for a given g_m/I_d, the GNR TFETs allow for the smallest device areas for a given design specification.

Since simulations for InAs DG TFETs were performed employing a compact analytical model, further analysis was performed in order to observe the linear range that this technology can provide. The mathematical relationship between I_d and an incremental change in the gate-to-source voltage (v_{gs}) can be expanded from a Taylor series around a certain operating point (V_{GS0}). Let's then consider the first and second derivative terms of the current I_d, g_m and $g_m'/2$, where g_m satisfies (5). Both terms are defined in an interval around V_{GS0}. For this V_{GS0}, a g_m/I_d value $(g_m/I_d)_0$ is associated. Strong nonlinear effects are associated with small $g_m/(v_{gs}.g_m'/2)$ ratios. Fig. 5 shows $g_m/(v_{gs}.g_m'/2)$ as a function of the amplitude of the incremental change in gate-to-source voltage (v_{gs}) and $(g_m/I_d)_0$. It is noticed that for large v_{gs} ($v_{gs} \gg 80$mV) and high $(g_m/I_d)_0((g_m/I_d)_0 \gg 200\text{V}^{-1})$ the $g_m/(v_{gs}.g_m'/2)$ ratio is <10, and therefore the device becomes strongly non-linear. Design in this region can take advantage of both non-linearity and low current consumption. This can be very useful in applications where proper operation relies on nonlinearity. For instance, in [15] the optimization of a TFET-based differential drive rectifier is presented.

In terms of more complex circuits, a TFET differential folded cascode OTA is presented in [14] to show the benefits of TFETs having a higher g_m/I_d than traditional FETs. At a given bias current, the DC gain, bandwidth, noise performance and offset improve by increasing the transconductance of the input transistors. Work by Trivedi *et al.* [13] shows that TFETs can reduce the power of analog amplifiers since the same transconductance as in a MOSFET based designs is achieved at lower powers through a higher g_m/I_d. In the present work a two-stage OTA with Miller effect compensation is designed by using the g_m/I_d method.

B. TWO-STAGE OTA WITH MILLER EFFECT COMPENSATION

The two-stage amplifier shown in Fig. 6(a) was analyzed at the 15-nm technology node employing GNR TFETs as well as Si FinFETs. GNR TFETs are chosen over other TFET technologies because of their large subthreshold current densities as previously discussed, but also because they provide similar characteristics for both n- and p-type transistors resulting from the symmetric band structure of graphene, which is desirable for circuit design. This amplifier topology has two poles and a right half plane zero; usual requirements for more than 60° phase margin (PM) in this circuit are: $NDP = \omega_{NDP}/GBW = 2.2$ and $Z = \omega_Z/GBW = 10$, where NDP is the ratio between the frequency of the non-dominant-pole (ω_{NDP}) and the *GBW*, and Z is the ratio between the frequency of the zero (ω_Z) and the *GBW*. In order to determine the amplifier design achieving the minimum current consumption, the synthesis mechanism described in [18] was employed. The current consumption in this circuit is:

$$I_d = 2I_{d1} + I_{d2} = \frac{2GBW}{\left(\frac{g_m}{I_d}\right)_1} C_m + \frac{ZGBW}{\left(\frac{g_m}{I_d}\right)_2} C_m, \tag{24}$$

where I_{d1} is the DC current through the transistors at the input differential pair (T_{1a}, T_{1b}), I_{d2} is the current through the transistor in the output stage (T_2), and C_m is the Miller compensation capacitance, which is calculated as:

$$C_m = \frac{NDP}{2Z}\left(C_1 + C_2 + \sqrt{(C_1 + C_2)^2 + \frac{4ZC_1C_2}{NDP}}\right), \tag{25}$$

where $C_2 = C_{out} + C_L$ is the total output capacitance of the amplifier (C_{out} is the capacitance seen looking from the node V_{out} to ground in the absence of load capacitance), and C_1 is the effective capacitance from the gate of T_2 to the AC ground. From (24) and (25) we observe that the minimum achievable current consumption in a two-stage amplifier with ideal traditional FETs, i.e., the current consumption considering the transistors with zero capacitances and maximum g_m/I_d, is given by:

$$I = \frac{2+Z}{Z}.GBW.C_L.NDP.U_t. \tag{26}$$

Depicted in Fig. 6(b) is the design space exploration for GNR and Si FinFETs for a 30GHz *GBW* target. For each technology and GBW target, an optimal transistor biasing configuration (i.e., $(g_m/I_d)_1$, $(g_m/I_d)_2$ pair) exists that leads to minimum current consumption. In the same way as for the one-stage common-source amplifier, although the minimum current scales with C_L, this optimal biasing configuration is independent of the value of C_L, i.e., it occurs at the same point regardless of the value of C_L. Therefore, although in

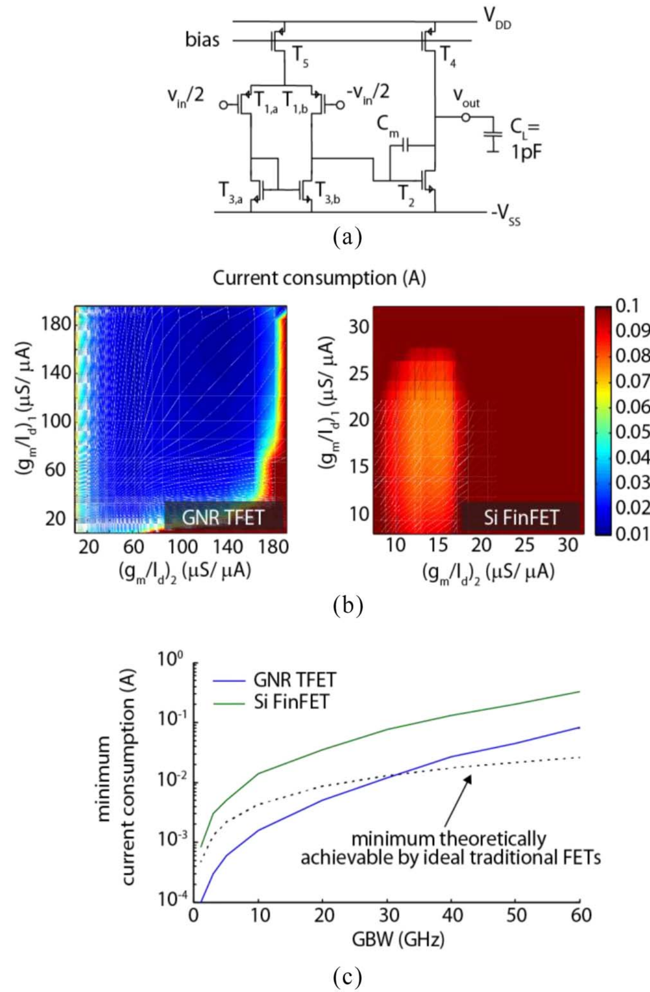

FIGURE 6. **(a) Schematic of a two-stage OTA with Miller effect compensation. (b) Design space exploration for GNR and Si-FinFET technologies at the 15-nm node for a 30 GHz GBW target. (c) Optimal (minimum) current consumption as a function of GBW.**

all our discussion a 1pF load capacitance is assumed, the conclusions drawn from our analysis are general enough and independent of the particular choice of load capacitance.

For a $GBW < 30$ GHz, the optimal current consumption employing 15-nm-gate GNR TFETs was found to be smaller than both the minimum consumption by the Si FinFETs and the minimum current theoretically achievable by ideal traditional FETs under the same design constraints (Fig. 6(c)). When setting the GBW requirement to 30GHz, the current consumption employing GNR TFETs was found to be about the minimum theoretically achievable in this circuit if employing ideal traditional FETs; however, for $GBW > 30$GHz the minimum power consumption employing GNR TFETs becomes larger than this limit due to heavy influence of the parasitic capacitances. It is observed that for all the analyzed GBW targets, the current consumption employing GNR TFETs is over 5X smaller than that by optimal designs using same gate-length FinFET technologies which is owed to: *i)* the possibility of biasing the device at a higher g_m/I_d, and *ii)* the superior current drive (I_d/W) for a given g_m/I_d in these devices. When considering the consumption in terms of power, since GNR TFETs allow for 3X lower V_{DD}, the optimal power consumption can be around 15X smaller.

Analysis of the slew rate deserves attention in circuit designs involving transistors biased at high g_m/I_d. The slew rate (SR) is defined as the minimum between the internal slew rate (SR_1) and the external slew rate (SR_2) as follows [20]:

$$SR = min\{SR_1, SR_2\}, \tag{27}$$

where:

$$SR_1 = \frac{2I_{d1}}{C_m} = \frac{2GBW}{\left(\frac{g_m}{I_d}\right)_1}, \tag{28}$$

and:

$$SR_2 = \frac{I_{d2}}{C_2} = \frac{ZGBW}{\left(\frac{g_m}{I_d}\right)_2}\frac{C_m}{C_2}. \tag{29}$$

At the optimal biasing point, the calculated slew rate for the GNR TFET based OTA is $SR = 2.44$ V/ns, whereas for the Si-FinFET based OTA is $SR = 15.78$ V/ns. In this regard, it is worth noticing that SR is inversely proportional to g_m/I_d as dictated by (28) and (29). However, it is also possible to design the OTA taking into account the slew rate as a design constraint as discussed in [20].

V. CONCLUSION

Since TFETs can operate in the sub-threshold region with larger g_m/I_d than traditional FETs, low power analog circuits with lower current consumption can be designed using these transistors. The g_m/I_d method, inherited from traditional MOSFETs, has been successfully discussed to design a one-stage common-source amplifier and a two-stage OTA with Miller effect compensation. A compact analytical model was discussed and proven to be compatible with the g_m/I_d method. In particular, an analytical expression for the maximum theoretically achievable value of g_m/I_d was derived based on the model parameters by performing a limit analysis. Both GNR TFETs and InAs DG TFETs, have a weak dependence of g_m/I_d on V_{DS}, which can enable circuit designs where transistors are operating at very low bias operating points. Based on the results from applying the g_m/I_d method, GNR TFETs seem to be very promising among all the field effect transistors proposed to-date for ultra-low power high-frequency analog applications. We conclude that GNR TFETs in general promise large bandwidth at low voltage drive due to their high current density in the subthreshold region.

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