

Received 18 November 2014; revised 8 February 2015; accepted 23 February 2015. Date of current version 22 April 2015.  
The review of this paper was arranged by Editor E. Sangiorgi.

Digital Object Identifier 10.1109/JEDS.2015.2409023

# Nature and Characteristics of a Voltage-Biased Varistor and its Embedded Transistor

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This work was supported by the National Science Foundation under Grant ECCS-1025395.

**ABSTRACT** An unorthodox approach for producing simple and yet practical transistors based on ceramic platforms is discussed in this paper. To achieve this, we modify the original nonlinear current-voltage ( $I$ - $V$ ) characteristics of a varistor by superimposing a biasing voltage ( $V_b$ ). This leads to the formation of a hybrid device consisting of a biased varistor and transistor. The studies were done under two experimental conditions; first, when the ratio between the drain current ( $I_d$ ) and the bias current ( $I_b$ ) is of the order of  $10^3$  or more, and second when it is less than  $10^2$ . The transistors embedded in the hybrid device exhibit the typical attributes of a conventional transistor. The transistors are analogous to the well-established bipolar junction transistors and yet different because they are based on different physical principles. These transistors can meet the requirements of many general purpose applications and can also function satisfactorily as low-pass filters. The specialized applications could be under hazardous conditions such as at high temperatures, in radiation-filled environments such as outer space, and possibly in bio systems. The biased varistor assumes the property of mutual conductance like a transistor as well as becomes a good signal amplifier.

**INDEX TERMS** Varistors, transistors, signal amplification, transconductance.

## I. INTRODUCTION

Varistors are simple two terminal bipolar diodes which are almost exclusively fabricated using ceramic substrates as opposed to traditional diodes for which the substrate materials used are commonly bulk single crystals and epitaxial films of silicon and other conventional semiconductor materials. Varistors are essential components of almost all electronic and microelectronic circuits where they perform the important function of circuit protection from sudden surges in voltage. Normally they act as a passive component in a circuit until a surge occurs because of weather conditions or some failure mechanism in the power supply. At that point the varistor becomes active and absorbs the excess voltage that would have otherwise destroyed the electronic components in the circuit. They are connected in parallel to the load (that is, the circuit to be protected) and function like a shunt.

In spite of the important function they perform, varistors are under appreciated electronic components compared to

diodes and transistors. It is interesting to note that already in 1947-48 its strong relationship with the newly discovered solid state device was realized when the name “transistor” was coined in Bell Labs where it was invented and patented. Out of six possible alternatives that were proposed by a team of engineers and scientists at Bell Labs it was settled that the new device be called, “transistor”. It is the abbreviation for “transconducting varistor” which was one of the six possible choices.

In order to understand the nature and properties of a varistor which can also transconduct we chose to study the effect on its current-voltage ( $I$ - $V$ ) characteristics when they are modified by the superposition of a bias voltage.

Once the contributions of the biasing voltages on the total output currents are extracted using simple equations the resulting  $I$ - $V$  plots are analogous to those of a transistor. An analysis of these  $I$ - $V$  characteristics are provided in this paper identifying the contributions made by these simple devices to the existing transistor technology. Considering the

practicality of these new devices which are based on simple structures they should be straight forward to produce in large volumes inexpensively.

## II. RELEVANT PROPERTIES OF SUBSTRATE MATERIAL

The varistors studied here are based on ceramic substrates having the composition of 55 atomic % ilmenite ( $\text{FeTiO}_3$ ) and 45 atomic % hematite ( $\text{Fe}_2\text{O}_3$ ) which is commonly referred as IHC45. It is both magnetic and semiconductor in nature and is classified as a room temperature wide band gap magnetic oxide semiconductor. Nominally it can be represented by the chemical formula of  $\text{Fe}_{1.45}\text{Ti}_{0.55}\text{O}_3$ . It is a prominent member of the ilmenite-hematite (IH) solid solution family which is expressed as  $(1-x)\text{FeTiO}_3 - x\text{Fe}_2\text{O}_3$  with  $0 < x < 1$ . It was first identified as an interesting magnetic and semiconductor system [1], [2]. Although both ilmenite and hematite are antiferromagnetic insulators, the IH solid solution series is strongly ferrimagnetic in the composition range of  $0.05 < x < 0.5$ . Many members of this series have magnetic Curie points above room temperature. Equally interesting is the semiconductor nature of the IH series; it can be made either as an n-type material or a p-type material simply by controlling the concentration  $x$  of hematite. The transition from p-type to n-type occurs around  $x = 0.20$  [2].

Since its recent identification as a room temperature wide band gap magnetic semiconductor the IH system has become a technologically important system. So far the number of papers published on IH system deals extensively with the magnetic properties rather than with its electrical properties [1], [3]–[10].

Another interesting feature of the IH system is the range of band gap varying between 2.4 to 3.3 eV which is strongly dependent upon the processing conditions such as annealing temperature, atmospheric conditions, and whether the sample is bulk ceramic or an epitaxial or textured film [8], [9]. In comparison, the band gap of the end members of the series is 2.54 eV for ilmenite and 2.00 eV for hematite [9], [11]. The compositions most studied in the recent past for their magnetic and electrical properties have been ceramic and films of IHC 33 ( $x = 0.33$ ) and IHC 45 ( $x = 0.45$ ) because they have been identified to have desirable magnetic and semiconducting properties for fundamental studies and applications. They also exhibit remarkable tolerance when exposed to radiations of neutrons, protons and heavy ions [10], [12], [13].

IHC 45 is a stable high temperature material with excellent semiconducting properties up to 700 °C. From the temperature dependence of the electrical resistivity, the band gap of bulk ceramic IHC 45 is determined to be 2.28 eV which is comparable to the values reported in literature for other iron titanates [14]. It is strongly ferrimagnetic with room temperature saturation magnetization,  $M_s \approx 19.4$  emu/g, coercivity,  $H_c \approx 250$  Oe, and the Curie temperature at 610 K [10]. From the capacitance vs. voltage (C-V) measurements the carrier concentration of IHC 33, which is similar to IHC 45

in many respects, was estimated to be of the order of  $10^{17}$   $\text{cm}^{-3}$  [15]. In comparison, for zinc oxide, ZnO, which is the leading varistor material the carrier concentration is approximately  $10^{18}$   $\text{cm}^{-3}$  [16].

## III. SAMPLE PROCESSING

High density bulk ceramic samples were processed using the standard steps of ball milling, sintering, pressing at high pressures, and finally annealing at high temperatures in air. The detailed steps were followed very closely as described in reference [7]. The x-ray diffraction analysis (XRD) analysis confirmed the sample to be hexagonal in agreement with references [1], [7]. The energy dispersive x-ray diffraction analysis (EDAX) revealed that the samples were deficient in iron by about 5 atomic %, whereas both titanium and oxygen were in excess by less than 2 atomic %. Such minor deviations from ideal composition are common for oxide ceramics [17].

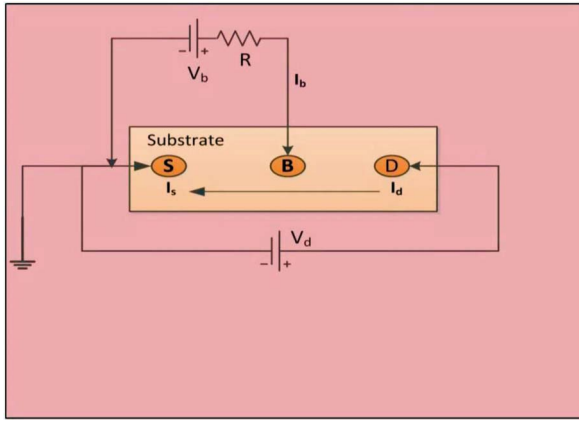
The 4-point resistivity measurements at room temperature gave a value of 2.28  $\Omega\cdot\text{cm}$ ; and the value for the Seebeck coefficient,  $\kappa = +170\mu\text{V} \cdot \text{K}^{-1}$  [14]. The positive sign of the Seebeck coefficient points to the p-type nature of IHC 45. Initially the sample was n-type and highly resistive. In order to reduce its resistance for  $I$ - $V$  measurements it was annealed in flowing argon around 1000 °C for many hours. This resulted in the conversion of IHC 45 from an n-type material to a p-type material. Such transformations are common with oxides. Extensive annealing also affects such fundamental properties as donor density, density of states, and barrier heights [18], [19].

Samples for studying the  $I$ - $V$  characteristics were cut as rectangular slabs from the ceramic pellets and polished on opposite major surfaces. The samples for experimental studies had usually the dimensions of about 8 mm long x 3 mm wide x 1-1.5 mm in thickness. Before putting contacts each sample was examined under an optical microscope to assure that there were no micro cracks.

## IV. DEVICES, PROPERTIES, AND APPLICATIONS

### A. EXPERIMENTAL DESIGN FOR $I$ - $V$ MEASUREMENTS

Preliminary experiments were done to identify a contact metal that could produce nonlinear  $I$ - $V$  characteristics with IHC 45 using silver, gold and aluminum. All produced linear  $I$ - $V$  plots with four point probe (4 pp) resistivity measurements but only silver exhibited well defined nonlinear  $I$ - $V$  characteristics with two point probe (2pp) measurements. Rectifying nature of the  $I$ - $V$  curve using silver contacts suggested the possibility of electron migration from the metal side to the semiconductor by overcoming the potential barrier that might exist at the interface between the metal contacts and substrate. From C-V measurements using an impedance analyzer ((HP-4192A LF, Hewlett Packard Company, Palo Alto, CA), it was determined that the substrate material was depleted underneath the silver contacts. This provided a basis for assuming the presence of a Schottky



**FIGURE 1.** Common source circuit configuration for  $I$ - $V$  determination of a varistor (based on common emitter configuration used for  $I$ - $V$  determination of an n-p-n BJT transistor using a parametric analyzer). Here,  $S$ ,  $B$ , and  $D$  refer to source, bias, and drain terminals, respectively.

barrier at the interface enabling the nonlinear  $I$ - $V$  characteristics to emerge which is the signature of a varistor device.

Two silver contacts of approximately 1 mm in diameter and 3 mm apart were put on the top surface of the rectangular slab using conducting silver epoxy. After air drying the samples were annealed at approximately 250 °C for 30-45 minutes. This allowed the silver contacts to bind strongly with the substrates and organic epoxy to burn off. For 2-point probe  $I$ - $V$  measurements one contact was assigned the label of source ( $S$ ) and the other drain ( $D$ ). The samples were mounted on the test fixture of a precision semiconductor parametric analyzer (HP-4145 B, Hewlett Packard Company, Palo Alto, CA) using fine silver wires. The test fixture was closed during the data collection to prevent interference from light and for rejecting electronic noise from any other equipment present in the laboratory. In order to apply a biasing voltage between the source ( $S$ ) and drain ( $D$ ) terminals of the sample a third silver contact was put at the center so that the three terminals were evenly spaced. The central terminal was assigned the label of  $B$  (for bias).

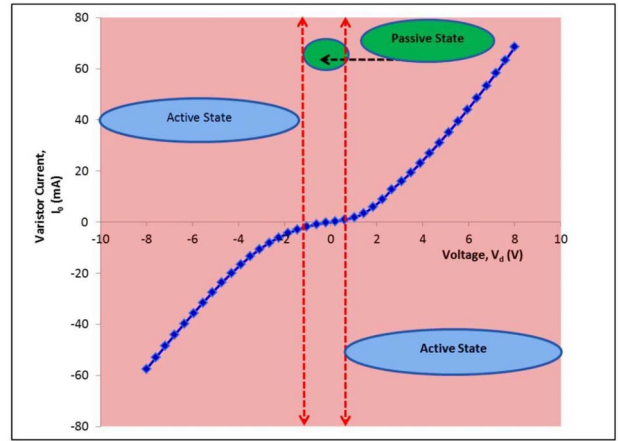
The circuit configuration, shown in Fig. 1, was used for the determination of  $I$ - $V$  characteristics of IHC 45 samples. Here we are essentially dealing with three interconnected varistors which are:  $S$ - $D$ ,  $D$ - $B$  and  $B$ - $S$ . According to Kirchhoff's law:

$$|I_d| \approx |I_s| + |I_b| \quad (1)$$

where,  $I_d$ , is the drain current,  $I_s$  the source current and  $I_b$  the bias current.

### B. TWO TERMINAL I-V CHARACTERISTICS OF VARISTOR

The two terminal  $I$ - $V$  characteristic of an IHC 45 varistor is shown in Fig. 2. This is the typical representation of the  $I$ - $V$  characteristic of a varistor which exhibits some unique features making a varistor a special class of diode.



**FIGURE 2.** Current-voltage characteristics of a two terminal varistor showing passive and active regions and switching voltages.

The two dashed parallel lines symmetrically situated to each side of the (0,0) origin of the plot represent the switching voltages,  $\pm V_s$ , of the varistor. These are equivalent to threshold potentials that must be overcome before the varistor becomes active. The region shown in green covering the range between the two dashed lines is the passive state in which the varistor impedance is high. Therefore, the initial output current is very small and the device acts as a passive component. Once the driving potential greater than  $\pm V_s$  is applied the device switches to the active state where the device impedance is low with the consequence of output currents rising rapidly. Normally a varistor remains in its passive state but as soon as the voltage or current exceeds the prescribed limits of the electronic components (for example, diodes, transistors etc.) in the circuit the varistors switches to its active state and thereby offering protection to the circuit elements. It remains in this mode until the transient surge ceases to exist. Then it returns to its passive state.

The current-voltage relationship of a varistor is given by a simple power law which states that

$$I \propto V^\alpha \quad (2)$$

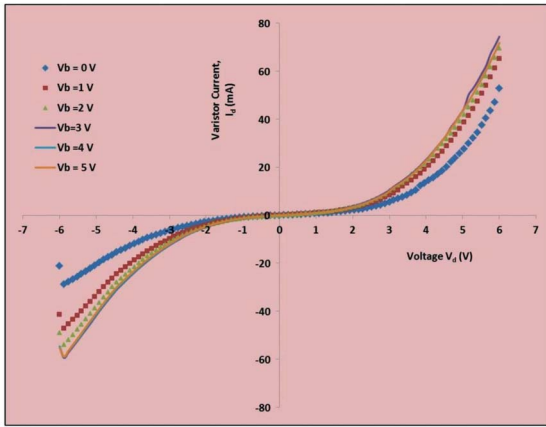
where,  $\alpha$  is called the nonlinear coefficient (NLC) of the device and can assume values ranging in single or double digits. The value of the NLC which is also the figure-of-merit of the device is defined by equation (3):

$$\alpha = \frac{\ln I_1 - \ln I_2}{\ln V_1 - \ln V_2} \quad (3)$$

The NLC for our two terminal varistor is 3.28 and the switching voltages,  $V_s \approx \pm 1V$ . These two parameters are favorable for using IHC 45 varistors in microelectronic circuits with silicon devices for which the maximum operating limit is approximately 5 V.

### C. CASE I: THREE TERMINAL VARISTOR DEVICE AND ITS EMBEDDED TRANSISTOR WHEN $I_d \geq 10^3 I_b$

Based on multiple experiments using the three terminal configuration we realized that the nature and properties of  $I$ - $V$



**FIGURE 3.** Bias voltage modified  $I$ - $V$  characteristics of a varistor with  $I_d \geq 10^3 I_b$ .

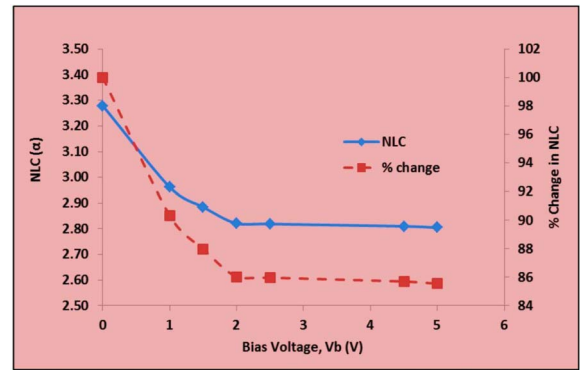
plots are dependent upon the ratio between the drain current ( $I_d$ ) and the bias current ( $I_b$ ). For understanding its importance and its impact the experiments were done under two sets of conditions which are: when (a) when  $I_d \geq 10^3 I_b$  and (b) when  $I_d \leq 10^2 I_b$ . These conditions are achieved by adjusting the value of resistance ( $R$ ) in Fig. 1 with respect to the varistor resistance between S and D contacts at  $V \approx 0$  V.

First we discuss the case of the  $I$ - $V$  characteristics determined when  $I_d \geq 10^3 I_b$ . In Fig. 3 these plots are shown as a function of the applied bias voltages. We notice from this figure that the largest change in current occurs as soon as  $V_b = 1$  V is applied. The increase in output current follows the increasing driving potentials. However, the actual quantitative increments in currents become smaller and smaller resulting in crowding of the  $I$ - $V$  plots for bias potentials,  $V_b > 2$  V.

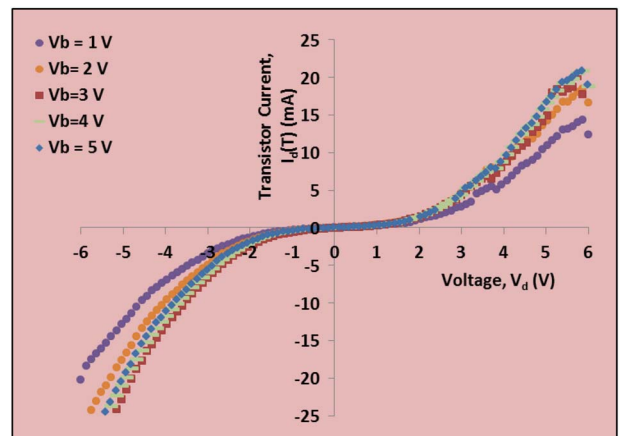
This phenomenon we believe is associated with the change in the potential barrier heights with respect to the applied bias potentials. Furthermore, we observe that each  $I$ - $V$  plot passes through the origin (0,0) of the x and y- axes without suffering any distortions in its shape which we will find is not the case when  $I_d \leq 10^2 I_b$ .

The impact of the bias voltage is noticeable on the non-linear coefficient (NLC) of the device as can be seen from Fig. 4. It decreases rapidly from its initial value of 3.28 at  $V_b = 0$  V to about 2.85 at  $V_b = 2$  V. For  $V_b > 2$  V it decreases with increasing bias rather monotonously making the change rather insignificant. Apparently for  $V_b > 2$  V the potential barrier might be reaching a state of equilibrium resulting in quasi saturation of output current as reflected in Fig. 3.

The same pattern is naturally repeated for the percentage change in NLC when normalized to 100 with respect to its original value at  $V_b = 0$  V. The maximum loss in NLC amounts to approximately 14 %. This is not a large loss in efficiency of the device and we believe the varistor could still be of practical interest as a circuit protector.



**FIGURE 4.** Bias-voltage dependence of the nonlinear coefficient,  $\alpha$ , and its percentage change with respect to its initial value of 3.28 at zero bias with  $I_d \geq 10^3 I_b$ .



**FIGURE 5.** Current-voltage characteristics of an embedded transistor with  $I_d \geq 10^3 I_b$ .

In a three terminal device we encounter three types of currents out of which two are measured directly and the third is embedded which must be filtered out. The measured currents are the modified currents ( $I_d$ ) for biased varistors, and ( $I_0$ ) the initial current of unbiased varistor. The embedded current is the contribution made by the applied bias potentials to the original current  $I_0$  and is assigned the symbol of  $I_d(T)$ .

Equation (4) gives the relationship between these three types of currents.

$$I_d(T) = I_d - I_0 \tag{4}$$

Once filtered out from net  $I_d$  the  $I_d(T)$ - $V$  behavior resembles that of a typical transistor. They are shown in Fig. 5. Like in the case of the parent varistor curves (see Fig. 3) here too the clustering effect begins to appear once  $V_b > 2$  V. However, the  $I$ - $V$  plots remain distinguishable from each other especially in the reverse mode of the device.

From Figs. 3 and 5 we observe that for both varistor and its embedded transistor the output currents increase in response to an increase in biasing potentials. The varistor current

is obviously much larger in magnitude than the transistor current. The maximum signal amplification,  $S(A)$ , for both the devices amounts to about 160% with drain voltage being kept constant at  $V_d = +5$  V. We can conclude from this that both devices can be used as simple voltage controlled signal amplifiers. The signal amplification as a function of the bias potential is computed by normalizing the final current with respect to the initial currents using the relationship:

$$\begin{aligned} \text{Signal Amplification, } S(A) &= \frac{\text{final current at a constant drain voltage}}{\text{initial current at the same drain voltage}} \\ &= \frac{I_{d,\text{final}}}{I_{d,\text{initial}}} \times 100 \end{aligned} \quad (5)$$

A transistor distinguishes itself from many other switching devices with respect to its unique capability for being able to “transconduct”. Using the standard definition of transconductance,  $G_m$ , we can express it with the help of equation (6) for our devices:

$$G_m = \frac{\text{transistor drain current}}{\text{bias voltage}} = \frac{I_d(T)}{V_b} \approx \left( \frac{\Delta I_d(T)}{\Delta V_b} \right) \quad (6)$$

The inverse of  $G_m$  gives the associated value for the mutual resistance,  $R_m$ .

These parameters are technically important for designing a transistor for current amplification or voltage amplification. A large value of  $G_m$  is desired for a good current amplifier whereas a large value of  $R_m$  is good for voltage amplification. We determine  $G_m = 1.62$  mS for the transistor with drain voltage,  $V_d$ , kept constant at + 5 V; making the transresistance,  $R_m$  to be equal to 617  $\Omega$ . These values are comparable to the values for Si based bipolar junction transistors (BJT). Based on these favorable parameters we can conclude that the IHC45 ceramic transistors when  $I_d \geq 10^3 I_b$  could be a good candidate for developing practical devices. In the reverse mode as well for which the applied potentials are negative, we determine that with  $V_d = -5$  V constant the transconductance,  $G_m = 3.24$  mS and  $R_m = 308$   $\Omega$  indicating that the transistor in the reverse mode is a better “mutual transconductor” than its counterpart. From this we can infer that the bias potentials in the reverse mode of the device lead to the decrease in the barrier heights favoring an increase in electron migration from metal to semiconductor. In the reverse mode, the signal amplification for varistor can be as high as 200 % making it a good candidate for designing a simple signal booster device. However, its value for the transistor remains unchanged at about 160%.

#### D. CASE II: THREE TERMINAL VARISTOR: DEVICE AND ITS EMBEDDED TRANSISTOR WHEN $I_d \leq 10^2 I_b$

Under the experimental condition of ( $I_d \leq 10^2 I_b$ ) the original two terminal varistor  $I$ - $V$  curve undergoes major changes leading to some interesting results of practical importance.

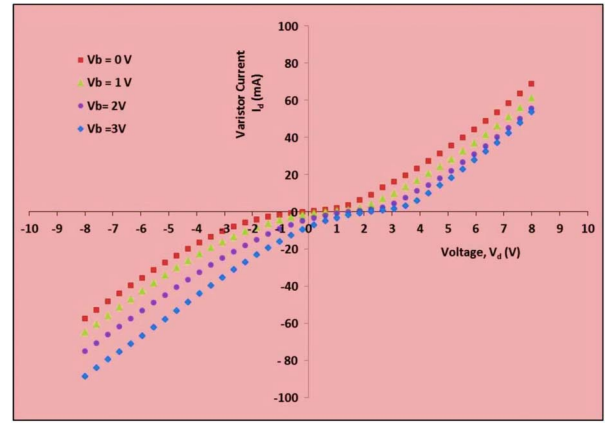


FIGURE 6. Current-voltage characteristics of a three terminal varistor when  $I_d \leq 10^2 I_b$ .

In Fig. 6 the resulting modified  $I$ - $V$  plots are given. From this we can identify a few significant changes taking place because of the application of the bias potential. First, the origin of the  $I$ - $V$  curve deviates from the (0,0) point and appears to be shifting toward the positive drain voltages ( $V_d$ ); second, the switching voltage becomes bias dependent, and third, larger signal amplification is produced by the device for negative values of the drain current than for its positive values.

As already discussed it appears that the bias potentials favor the changes in the potential barrier resulting in enhanced currents. In this mode also each  $I$ - $V$  plot is clearly distinguishable without any tendency for clustering. So far as the efficiency (NLC) of the varistor is concerned it is affected rather drastically. The value of nonlinear coefficient,  $\alpha$ , reduces from its maximum value of 3.28 at  $V_b = 0$  V to 2.22 at  $V_b = 2$  V amounting to a reduction of about 68 % rendering it practically useless for circuit protection. Nevertheless its potential as a signal amplifier remains intact and approximately at the same level as for the varistor discussed in case I.

Once again, as the contributions of the bias potentials are extracted from the net drain currents,  $I_d$ , we encounter the presence of an embedded transistor. However, to obtain the representative  $I$ - $V$  characteristics, we need to modify equation (4) to be consistent with the sign convention followed in practice. To achieve this we can rewrite equation (4) as a set of two equations:

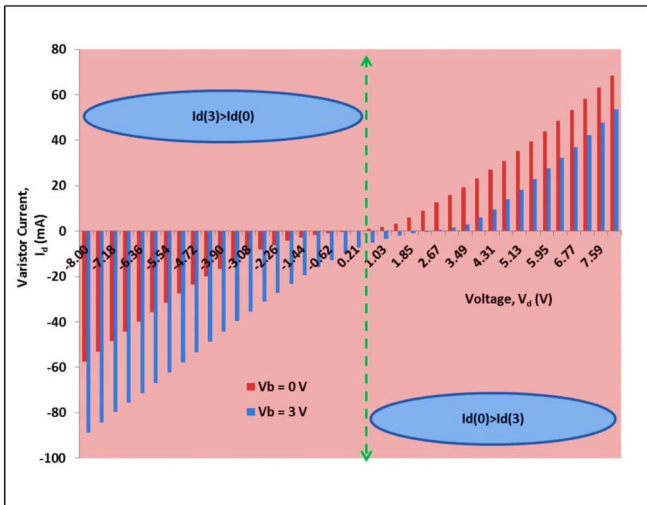
(a) for  $I_d(T)$  corresponding to positive values of  $V_d$ :

$$+I_d(T) = (I_0 - I_d) \quad (7)$$

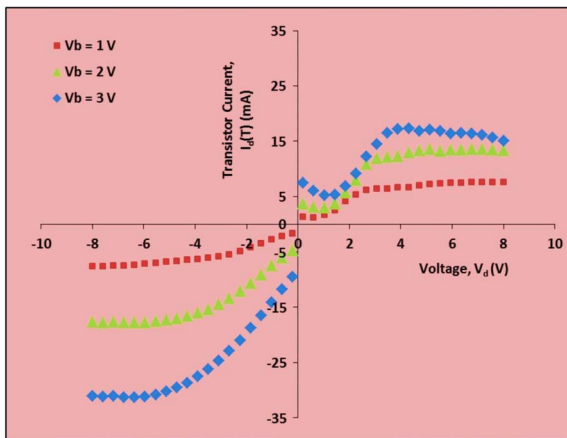
(b) for  $I_d(T)$  corresponding to negative values of  $V_d$ :

$$-I_d(T) = (I_d - I_0) \quad (8)$$

The validation of this approach is provided graphically in Fig. 7 where we compare the  $I$ - $V$  plots corresponding to  $V_b = 0$  and  $V_b = 3$  V, respectively. From the figure we can see that  $I_d(0) > I_d(3)$  for the forward mode of the



**FIGURE 7.** Columnar representation of varistor currents as a function of driving voltages for bias voltages equal to 0 and 3 V when  $I_d \leq 10^2 I_b$ .



**FIGURE 8.** *I-V* characteristics of an embedded transistor when  $I_d \leq 10^2 I_b$ .

device resulting in a positive value of  $I_d(T)$ ; whereas in the reverse mode  $I_d(0) < I_d(3)$  yielding a negative value of  $I_d(T)$ .

The bipolar *I-V* characteristics of the embedded transistor which is shown in Fig. 8 is readily obtained by applying the two equation (7) and (8) to the varistor output currents of Fig. 6.

Contrary to the characteristics of the transistor shown in Fig. 5 we find in Fig. 8 that for each individual value of the bias potential the *I-V* curve reaches the state of saturation, which is the hallmark of a conventional transistor.

Using once again equation (6) we determine the values for the mutual transconductance,  $G_m$ , for the varistor and transistor. Similarly their signal amplification,  $S(A)$ , was obtained using equation (5).

For both the devices these two parameters were determined while keeping the drain voltage constant at - 6V which falls in the saturated region of the *I-V* plots. The values for transconductance,  $G_m$ , are found to be 12 mS for the transistor and 10.8 mS for the varistor. These are the highest

values obtained so far for the bias induced varistor-transistor hybrid devices ( $V_b$ -VTH). The signal amplification,  $S(A)$ , for each of the two devices at  $V_d = -6$  V are 450 % for the transistor and 150 % for the varistor. It can be claimed that a  $V_b$ -biased transistor produced under the condition of ( $I_d \leq 10^2 I_b$ ) would be capable of exhibiting an impressive level of signal amplification which would compare favorably with the amplification provided by established BJT devices. On the other hand, under the same conditions varistor can amplify the signal just by 150 % which is roughly the same as the varistor under the conditions described in Case I.

Detailed results pertaining to transconductance, signal amplification and potential applications are summarized in Table 1 for both varistors and their embedded transistors discussed under the two cases. In a separate paper we have reported the frequency response of the devices similar to the ones discussed in this section [14]. The bandwidth for varistor was found to be 780 kHz while it was 310 kHz for the embedded transistor resulting into the conclusion that both varistors and transistors would perform well as a low pass filter [14].

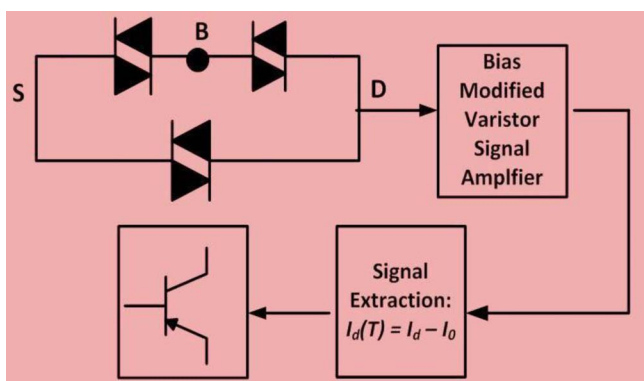
### V. COMPARISON BETWEEN VOLTAGE-BIASED TRANSISTOR AND BJT TRANSISTOR

The transistors described here are analogous to the well-known bipolar junction transistors (BJT). While the nature of the *I-V* characteristics of the two devices and their attributes bear resemblance to each other the physical principles involved in their origins and current transport mechanisms are distinctly different. The transistors discussed in this paper have their origin in varistors whose *I-V* characteristics are modified by superimposing a bias potential. For the embedded transistors the source (S), drain (D) and bias (B) contacts are simple metallic contacts which are made on a uniformly p-type substrate with no presence of any n-type of region either implanted or diffused. They cause depletion layer to form and a potential barrier to develop at the interface enabling the *I-V* characteristics to be non-linear. The thermionic emission is the underlying process responsible for current transport in a varistor similar to that in a Schottky diode. On the other hand a BJT structure consists of p-n-p or n-p-n configuration in which the charge carriers are also thermally generated. The current transport in a  $V_b$ -biased transistor is based on the so-called G-GB-G (grain-grain boundary-grain) process which is universally present in a metal oxide ceramic varistor. The theory of Schottky barrier formation for a metal oxide varistor (especially ZnO) is treated in [16]. In comparison, in a BJT device the current transport is because of the injection of charge carriers at the “base” terminal which are subsequently collected at the “collector” terminal resulting in enhanced current. In a  $V_b$ -biased transistor the drain current is controlled by the input of the potential at the “bias” terminal similar to as in BJT devices the current at the “collector” is controlled by the potential applied at the

**TABLE 1. Device properties and potential applications.**

Devices	Maximum Signal Amplification	Transconductance $G_m$	Transresistance $R_m$	Applications
<b>Case I. Devices with <math>I_d \geq 10^3 \times I_b</math></b>				
Drain voltage kept constant at +5 V				
(a) Varistor	163%	undetermined	undetermined	signal booster
(b) Transistor	160%	1.62 mS	617 $\Omega$	CCVS; Transresistance Amplifiers
Drain voltage kept constant at -5 V				
(a) Varistor	196%	undetermined	undetermined	signal booster
(b) Transistor	158%	3.24 mS	308 $\Omega$	CCVS; Transresistance Amplifiers
<b>Case II. Devices with <math>I_d \leq 10^2 \times I_b</math></b>				
Drain voltage kept constant at +6 V				
(a) Varistor	160%	7.17 mS	139 $\Omega$	VCCS ; Transconductance Amplifiers
(b) Transistor	220%	4.48 mS	223 $\Omega$	VCCS ; Transconductance Amplifiers
Drain voltage kept constant at -6 V				
(a) Varistor	150%	10.8 mS	92.5 $\Omega$	VCCS ; Transconductance Amplifiers
(b) Transistor	450%	12 mS	83 $\Omega$	VCCS ; Transconductance Amplifiers

(Note: CCVS stands for current controlled voltage source and VCCS for voltage controlled current source).



**FIGURE 9. Block diagram showing three interconnected varistors, a varistor signal amplifier, and a transistor. The labels S, B, and D refer to source, bias, and drain, respectively (as in Fig. 1).**

“base” terminal. We make use of the block diagram shown in Fig. 9 to illustrate how the three interconnected varistors give rise to a varistor based signal amplifier and an embedded transistor. Clearly the mechanics how the bias

induced transistor evolves is different from that for a BJT. Nevertheless, both transistors are superficially similar in many aspects.

## VI. CONCLUSION

The objective of this paper has been to determine the effect of a biasing voltage on the output current of a varistor by superimposing a bias potential between the source and the drain of the varistor structure. The experiments were done under two conditions: (1) when the ratio between the drain current ( $I_d$ ) and bias current ( $I_b$ ) is approximately  $\geq 10^3$ ; and (2) when it is  $\leq 10^2$ . For the first case the varistor remains useful for circuit protection applications whereas for the second case its efficiency is drastically compromised making it practically unsuitable for circuit protection. Nevertheless, the varistors assume the capacity to amplify signals under both these conditions and can be used as simple current amplifiers. When the modified current-voltage characteristics are analyzed for the biased varistors, the presence of an embedded transistor is revealed. Once the contributions

made by the bias voltages ( $V_b$ ) are separated from the modified drain current ( $I_d$ ) we get the typical  $I$ - $V$  characteristics of a transistor. It is established that these transistors possess all the attributes commonly found in a conventional transistor. Like a conventional transistor these new devices can provide signal amplification and transconductance. A strongly coupled nature of a varistor and a transistor is experimentally established in this paper providing a foundation for a new class of device. The novelty of these devices lies in the fact that they are hybrid in nature and are built on a single platform. The substrate material is the ceramic of an oxide wide band gap semiconductor with the chemical formula of  $\text{Fe}_{1.45}\text{Ti}_{0.55}\text{O}_3$  (IHC45). Some relevant properties of modified varistors and their embedded transistors have been ascertained and their potential applications proposed. These transistors can meet the requirements of many general purpose applications. Their specialized applications could be under hazardous conditions such as at high temperatures, in radiation filled environments such as outer space, and possibly in bio systems. Being based on ceramic these devices would be rugged and capable of withstanding abuses found normally under field conditions.

## ACKNOWLEDGMENT

The authors would like to thank Prof. W. Geerts of the Department of Physics at Texas State University for allowing them the extensive use of the facilities available in his semiconductor characterization laboratory.

## REFERENCES

- [1] Y. Ishikawa, "Magnetic properties of the  $\text{FeTiO}_3$ - $\text{Fe}_2\text{O}_3$  solid solution series," *J. Phys. Soc. Jpn.*, vol. 12, no. 10, pp. 1083–1098, 1957.
- [2] Y. Ishikawa, "Electrical properties of  $\text{FeTiO}_3$ - $\text{Fe}_2\text{O}_3$  solid solution series," *J. Phys. Soc. Jpn.*, vol. 13, no. 1, pp. 37–42, 1958.
- [3] G. Shirane, D. E. Cox, W. J. Takei, and S. L. Ruby, "Mossbauer study of isomer shift, quadrupole interaction, and hyperfine field in several oxides containing Fe57," *Phys. Rev.*, vol. 125, no. 4, pp. 158–161, 1962.
- [4] W. H. Butler, A. Bandyopadhyay, and R. Srinivasan, "Electronic and magnetic structure of a 1000K magnetic semiconductor: Alpha-hematite (Ti)," *J. Appl. Phys.*, vol. 93, no. 10, pp. 7882–7884, 2003.
- [5] D. M. Allen *et al.*, "Chemical ordering in ilmenite-hematite bulk ceramics through proton irradiation," *Appl. Phys. Lett.*, vol. 85, no. 24, pp. 5902–5904, 2004.
- [6] H. Hojo, K. Fujita, K. Tanaka, and K. Hirao, "Room-temperature ferrimagnetic semiconductor of  $0.6\text{FeTiO}_3$ - $0.4\text{Fe}_2\text{O}_3$  solid solution thin films," *Appl. Phys. Lett.*, vol. 89, no. 14, 2006, Art. ID 142503.
- [7] L. Navarrete *et al.*, "Magnetization and curie temperature of ilmenite-hematite ceramics," *J. Amer. Ceram. Soc.*, vol. 89, no. 5, pp. 1601–1604, 2006.
- [8] J. Dou *et al.*, "Preparation and characterization of epitaxial ilmenite-hematite films," *J. Appl. Phys.*, vol. 101, no. 5, 2007, Art. ID 053908.
- [9] J. Dou *et al.*, "Magnetic properties of ilmenite-hematite films and bulk samples," *J. Appl. Phys.*, vol. 103, no. 7, 2008, Art. ID 07D117.
- [10] R. K. Pandey *et al.*, "Novel magnetic-semiconductors in modified iron titanates for radhard electronics," *J. Electroceram.*, vol. 22, nos. 1–3, pp. 334–341, 2009.
- [11] Z. Dai, H. Naranato, K. Narazumi, S. Yamamoto, and A. Miyashita, "Structural, optical and electrical properties of laser deposited  $\text{FeTiO}_3$  films on C- and A-cut sapphire substrates," *J. Appl. Phys.*, vol. 85, no. 10, pp. 7433–7437, 1999.

- [12] P. Padmini *et al.*, "Influence of proton radiation on the nonlinear current-voltage characteristics of pulsed laser deposited ilmenite-hematite thin films," *J. Electron. Mater.*, vol. 34, no. 8, pp. 1095–1098, 2005.
- [13] P. Padmini, M. Pulikkathara, R. Wilkins, and R. K. Pandey, "Neutron radiation effects on the nonlinear current-voltage characteristics of ilmenite-hematite ceramics," *Appl. Phys. Lett.*, vol. 82, no. 4, pp. 586–588, 2003.
- [14] R. K. Pandey, W. A. Stapleton, I. Sutanto, A. A. Scantlin, and S. Lin, "Properties and applications of varistor-transistor hybrid devices," *J. Electron. Mater.*, vol. 43, no. 5, pp. 1307–1316, 2014.
- [15] C. Lohm *et al.*, "IV and CV characteristics of multifunctional ilmenite-hematite  $0.67\text{FeTiO}_3$ - $0.33\text{Fe}_2\text{O}_3$ ," in *Functionalized Nanoscale Materials, Devices and Systems* (NATO Science for Peace and Security Series B: Physics and Biophysics). Dordrecht, The Netherlands: Springer, 2008, pp. 419–424.
- [16] L. Hozer, *Semiconductor Ceramics: Grain Boundary Effects*. New York, NY, USA: Ellis Horwood, 1994, pp. 53–59.
- [17] R. K. Pandey, W. A. Stapleton, I. Sutanto, A. A. Scantlin, and S. Lin, "Configurations, characteristics and applications of novel varistor-transistor hybrid devices using pseudobrookite oxide semiconductor ceramic substrates," *Ceram. Trans.*, vol. 249, pp. 175–196, Oct. 2014.
- [18] M. R. Cassia-Santos *et al.*, "Recent research developments in  $\text{SnO}_2$ -based varistors," *Mater. Chem. Phys.*, vol. 90, no. 1, pp. 1–9, 2005.
- [19] C.-W. Nahm, "Electrical properties and dielectric characteristics CCT-doped Zn/Pr-based varistor with sintering temperature," *Trans. Elect. Electron. Mater.*, vol. 10, no. 3, pp. 80–84, Jun. 2009.



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