Received 7 September 2014; revised 17 October 2014 and 3 November 2014; accepted 10 November 2014. Date of current version 22 April 2015.
The review of this paper was arranged by Editor D. Esseni.

Digital Object Identifier 10.1109/JEDS.2015.2390591

Tunnel Field-Effect Transistors: Prospects and Challenges

UYGAR E. AVCI, DANIEL H. MORRIS, AND IAN A. YOUNG

Components Research in Technology and Manufacturing Group, Intel Corporation, Hillsboro, OR 97124 USA

CORRESPONDING AUTHOR: U. E. AVCI (e-mail: uygar.e.avci@intel.com)

ABSTRACT The tunnel field-effect transistor (TFET) is considered a future transistor option due to its steep-slope prospects and the resulting advantages in operating at low supply voltage (V_{DD}). In this paper, using atomistic quantum models that are in agreement with experimental TFET devices, we are reviewing TFETs prospects at $L_G = 13$ nm node together with the main challenges and benefits of its implementation. Significant power savings at iso-performance to CMOS are shown for GaSb/InAs TFET, but only for performance targets which use lower than conventional V_{DD}. Also, P-TFET current-drive is between 1× to 0.5× of N-TFET, depending on choice of I_{OFF} and V_{DD}. There are many challenges to realizing TFETs in products, such as the requirement of high quality III–V materials and oxides with very thin body dimensions, and the TFET's layout density and reliability issues due to its source/drain asymmetry. Yet, extremely parallelizable products, such as graphics cores, show the prospect of longer battery life at a cost of some chip area.

INDEX TERMS Tunnel field-effect transistor (TFET), steep-slope.

I. INTRODUCTION

Reducing supply voltage (V_{DD}) while keeping leakage current low is critical for minimizing energy consumption and improving mobile device battery life. The thermal limit of MOSFET subthreshold swing (SS) restricts lowering threshold voltage (V_t), causing significant performance degradation at low V_{DD}. A Tunneling Field Effect Transistor (TFET) is not limited by this thermal tail and may perform better at low V_{DD}.

Since the first experimental proof of subthreshold swing (SS) < 60mV/dec [1], TFET's prospects have attracted the interest of researchers. Silicon's large indirect bandgap and large carrier mass means drive-current for Si TFET is very low. But due to the availability of high-quality material together with years of know-how, Si and Si/Ge TFETs have been studied the most, with [2] showing the first of many devices with SS < 60mV/dec. III-V material for TFETs attracted attention because of its low bandgap and carrier mass and eventually broken bandgap hetero-junctions were shown to have the highest TFET drive-current [3]. However, few demonstrations [4]–[6] of steep SS III-V TFETs exist due to the immaturity of bulk semiconductor and gate-oxide quality of these novel materials and the difficulty to realize thin-body geometry.

In this paper, a comprehensive model that is in agreement with experimental devices is used to compare a high current capable GaSb/InAs TFET to Si CMOS at an $L_G = 13$nm technology node. The operating region where TFET would be beneficial is explained including considerations for variation. Challenges for realization of steep SS and issues with TFET circuit layouts are discussed. In the last section opportunities offered by TFET transistors for products are explained.

II. DEVICE MODELS AND TFET DEVICE DESIGN

A. DEVICE MODELS

In order to model TFET characteristics, we used an atomistic quantum mechanical device simulator that calculates carrier density self consistently with the Poisson equation [7]. The band structures are calculated using the sp3s* tight-binding model with spin-orbit coupling and the transport is assumed to be ballistic. In order to verify the validity of a ballistic approach, effects of polar optical phonon (POP) and optical deformation potential (ODP) scattering are modeled using a two-band tight-binding approximation [8]. Although there is a slight current loss due to phonon scattering, the overall

2168-6734 © 2015 IEEE. Translations and content mining are permitted for academic research only.
Personal use is also permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

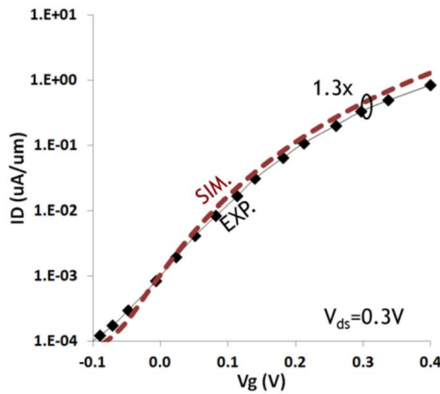

FIGURE 1. I–V characteristics show the similarity of a 20 nm-thick TFET modeled with atomistic quantum simulations and a 60 μm-thick experimental TFET both with InGaAs channel, $L_{eff} = 100$ nm, EOT = 1.4 nm at $V_{DS} = 0.3$ V.

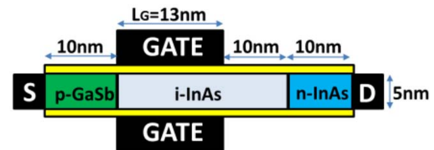

FIGURE 2. TFET structure cross section is simulated using atomistic quantum simulations. A 5 nm thin nanowire body and a 10 nm drain underlap is required to achieve steep SS at $L_G = 13$ nm. Gate oxide is 0.8 nm thick with relative permittivity of 3.9 and the source junction is aligned with the gate edge.

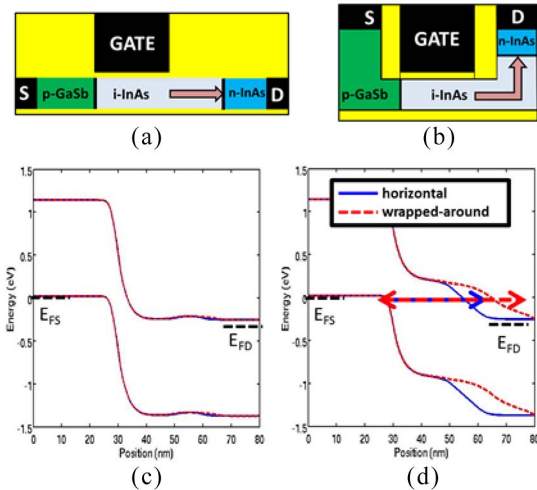

FIGURE 3. Two approaches to build the TFET drain underlap are shown for a 5 nm thick body TFET. (a) Horizontal. (b) Wrapped-around. Electrostatic potential profiles of TFET for two structures when the gate is (c) on and (d) off show that although on-state profile does not change, off-state profile has a longer tunneling path and thus lower leakage for wrapped-around drain. The wrapped-around drain TFET structure also has the advantage of fitting into a MOSFET-like gate-pitch.

effect of phonon scattering on Het-j TFET characteristics is inconsequential.

This quantum model is used to characterize I-V and C-V behavior of both the Si MOSFET and the GaSb/InAs TFET (Het-j TFET) which are the main subjects of this paper. Other TFET materials such as Ge, GeSn, InAs and InGaAs are also modeled to help determine the optimum TFET material choice. A detailed comparison between InGaAs TFET's experimental characteristics and atomistic quantum mechanical predictions has verified the validity of the atomistic models [9]. Simulations did not employ any fitting parameters to match the experimental data, but instead used only material and geometry parameters as inputs. The results show that the experimental and simulation characteristics are in reasonable agreement, suggesting that the atomistic simulations have good predictability (Fig. 1). Although non-idealities such as defects and non-abrupt band-edges are of critical importance, the differences between scaled TFET predictions and published large dimension experimental TFET devices have been shown to be due to the sub-optimal geometry of experimental devices [9].

B. DEVICE DIMENSIONS FOR ITRS NODE AT YEAR 2018

One of the main requirements of a state-of-the-art semiconductor technology is the dimension of the unit transistor, which directly determines the total area of the electronic chip, and thus the cost of the product. Although higher cost may in some cases be acceptable for uniquely low power devices, we investigate here the possibility of the TFET as an iso-gate-pitch transistor option to the MOSFET.

According to the ITRS roadmap [10], the 2018 Low Operating Power transistor target requires L_G=13nm to enable the necessary gate-pitch scaling. With the ITRS' recommended 8.7nm multi-gate MOSFET body thickness, the MOSFET would not have a close-to-ideal SS. Nor with a 5nm body thickness would a double-gate Het-j TFET achieve sub-60 mV/dec SS along with an I_{OFF} below 1nA/μm. Specifying a square NW geometry device with a body thickness ~5nm gives a Het-j TFET SS significantly below 60mV/dec and I_{OFF}~10pA/μm, while it also gives a MOSFET close to ideal SS (Fig. 2).

One concern about fitting a TFET transistor into the same gate-pitch as a MOSFET is TFET's drain underlap requirement [11]. To achieve reasonable short-channel behavior at L_G=13nm node, TFET requires a 10nm undoped drain region between the gate edge and the doped drain region. One way to implement this is to use undoped drain epi-growth for the region under the spacer (5nm) and then another 5nm in vertical direction, before continuing with doped drain epi-growth (Fig. 3). It can be shown that due to the additional gate control through the spacer, this new geometry has better electrostatics than the horizontal drain-underlap design. Thus, the drain-underlap requirement of the TFET does not prevent a TFET from being implemented at the same gate-pitch as a MOSFET.

C. I-V AND C-V CHARACTERISTICS

Comparison of Si MOSFET at L_G=13nm node to N-TFETs of different materials shows each has advantages over MOSFET at different current levels [Fig. 4(a)] [8].

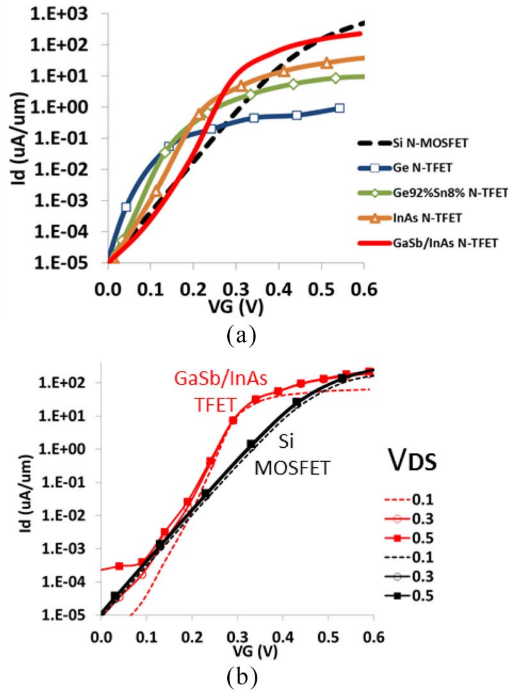

FIGURE 4. **(a) I–V characteristics of N-TFETs using different channel materials are compared to MOSFET. GaSb/InAs (Het-j) N-TFET has the highest drive-current and the highest crossover voltage with MOSFET. (b) I–V characteristics illustrate V_{DS} dependence of short channel length Het-j N-TFET compared to Si MOSFET. Steepest region of TFET and MOSFET I–Vs have SS of 41 and 63 mV/dec, respectively.**

The crossover supply voltage is an inexact but practical measure of the V_{DD} value under which TFET power-performance would be beneficial over MOSFET. The crossover is highest for the Het-j TFET due to its high tunneling current capability. This makes the Het-j TFET the more practical option for designers, with its performance capability closest to state-of-the-art CMOS operating points.

I-V characteristics of Het-j TFET are compared to Si MOSFET in Fig. 4(b). One important point is that TFET I_{OFF} shows strong V_{DS} dependence. Even with 10nm drain-underlap and low drain doping, Het-j TFET I_{OFF} increases significantly as V_{DD} increases beyond 0.3V. Whereas Het-j TFET can support $I_{OFF} < 10$pA/um at 0.3V, the lowest I_{OFF} achievable at 0.5V is 1nA/um. Another major difference is that Het-j TFET has lower total gate-capacitance than Si MOSFET due to low density-of-states (DOS) of the InAs conduction band. This is an important factor for lowering dynamic power and circuit delay.

D. P-TFET CHARACTERISTICS

Some materials such as Si, Ge and GeSn show comparable I-V characteristics for both P-TFET and N-TFET. But although Het-j N-TFET is capable of steep SS, III-V P-TFET designed without optimized source doping has just SS$\sim$60mV/dec. This is due to large Fermi degeneracy of the source creating a region where SS is determined by the thermal tail [12]. It is possible to improve Het-j P-TFET SS

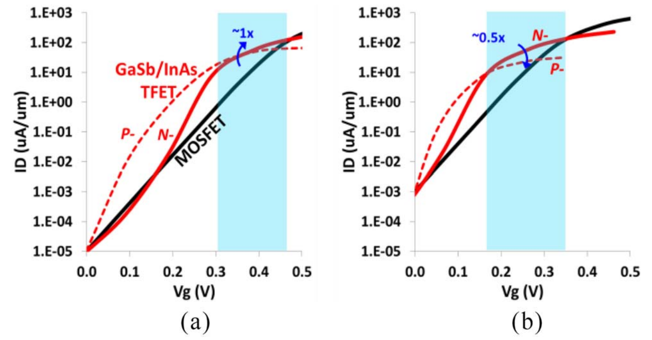

FIGURE 5. **I–V characteristics of *P* (dashed red line) and *N* (solid red line) type Het-j TFET compared to MOSFET (black line) at two different IOFF targets. (a) 10 pA/μm. (b) 1 nA/μm. Whereas high source doping ($\sim$7e19) is used for N-TFET, optimum source doping of 1$\sim$2e19 is used for P-TFET. Depending on specific IOFF and VDD target, P-TFET drive current is 0.5$\sim$1$\times$ of N-TFET.**

by lowering source doping, and thus the Fermi degeneracy. However, the doping level has to be carefully designed, so that the electric-field does not decrease significantly at the source-channel junction and lower the drive-current. Fig. 5 shows that an optimum level of source doping lies around 1$\sim$2e19cm^{-3} for Het-j P-TFET. Especially for lower I_{OFF} targets, P-TFET can have comparable drive-current to N-TFET. And for most relevant I_{OFF} and V_{DD} target ranges, P-TFET would be no less than 0.5x the drive current of N-TFET. Although this is not preferred, it is not a major limitation for the design of complementary TFET circuits.

III. CIRCUIT POWER-PERFORMANCE

A. CIRCUIT MODELS AND POWER PERFORMANCE COMPARISON

Lookup table based SPICE models generated from current and capacitance characteristics of atomistic models of the nanowire Lg=13nm ITRS 2018 technology node are used to simulate fanout=4 (F04) inverter circuits. To compare power-performance of CMOS and TFET logic, V_t and V_{DD} are used as free parameters [8]. To combine leakage power and dynamic power components, activity factors are used which represent different product usage scenarios. As explained in Section II-D, Het-j P-TFET drive currents are between 1x and 0.5x the Het-j N-TFET drive currents, depending on the operating region. To emphasize two possible extremes, we focus on two pull-up transistor options: (a) an ideal P-TFET with current symmetric to Het-j N-TFET and (b) a PMOSFET paired with a Het-j N-TFET. Whereas option (a) is plausible in some operating regions, option (b) is more realistic for high V_{DD} and I_{OFF} conditions.

Fig. 6 shows a power-performance comparison for the ideal case (option (a)). In contrast to CMOS, TFET logic cannot achieve very high performance and so the ITRS High Performance target ($V_{DD}\sim$0.73V) is well beyond the TFET-CMOS crossover point. However, the ITRS Low Operating-Power target ($V_{DD}\sim$0.57V for ITRS year 2018), which is most important for products requiring especially low dynamic power ($\sim$CV^2), is very close to the crossover

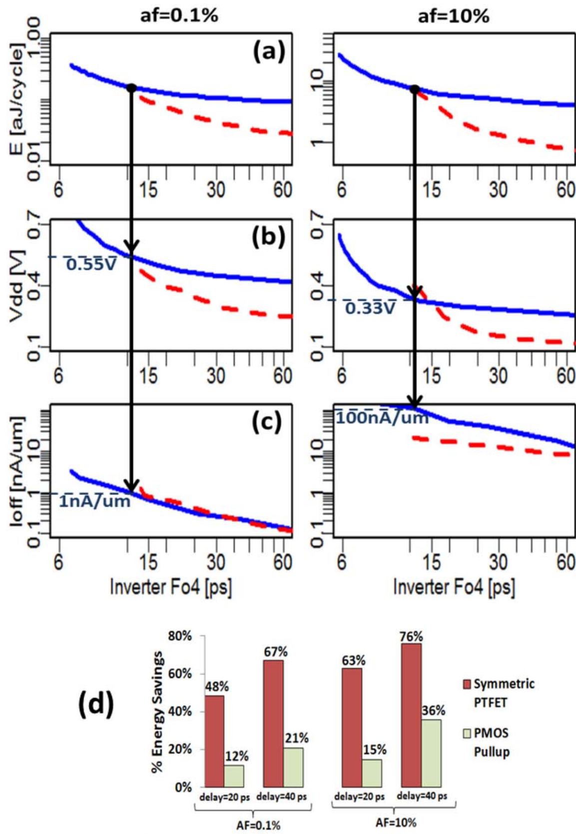

FIGURE 6. (a) Comparison of CMOS (solid line) and TFET (dashed line) minimum energy versus delay curves for 0.1% (left) and 10% (right) logic activity factor (AF). (b) V_{DD} and (c) I_{OFF} at the optimum energy points. Note that V_{DD} and I_{OFF} at the energy crossover points are shown with arrows. (d) TFET logic energy savings compared to CMOS, assuming the pull-up transistor is either a P-TFET symmetrical to Het-j N-TFET (red) or a PMOSFET (green). Average savings over four different operating regions is 64% for symmetric case and 21% for pMOS pull-up case.

point with I_{OFF} ~1nA/um. For designs that require even lower power, TFET power can be about 1/2 to 1/4 the total CMOS power with iso-performance at a 20ps~40ps inverter delay range. For option (b), where a PMOSFET is the pull-up transistor paired with a Het-j N-TFET, the heterogeneous pull-up and pull-down pair show ~3/4 of the power of CMOS alone [Fig. 6(d)].

B. EFFECT OF DEVICE VARIATION

Effects of device variations on I-V characteristics are studied assuming 10% variation for device dimensions and A_{Vt}~1 for work-function variation (WFV) [13]. With predicted process variation levels, WFV is the leading source of variation for both MOSFET and TFET. The TFET is more susceptible to higher leakage current variation, but the MOSFET's drive current variation is larger. Note that in the case of significant improvement in WFV, TFET would have higher device variation than MOSFET because TFET's secondary sources of variation, such as source random dopant fluctuation (RDF), are larger than those of the MOSFET.

The effect of device variations on circuit power-performance is projected by Monte Carlo simulation of

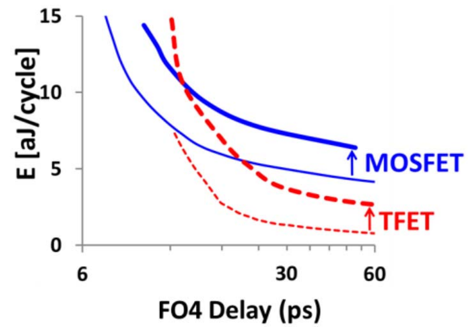

FIGURE 7. Power-performance without (thin lines) and with (thick lines) device variations is shown for a 10% logic activity factor. TFET energy savings are slightly lowered with variations.

circuits with random V_t modeling. Supply voltage and I_{OFF}, are treated as free variables for variation-aware V_{DD} and V_t optimization. The optimum V_{DD} increases for both devices due to increased degradation of performance at low V_{DD}, highlighting obstacles facing low-voltage logic. When variations are included, TFET logic still shows better energy-efficiency than CMOS, but the energy savings are reduced from 76% to 54% for the case where AF=10% and delay=40ps (Fig. 7).

IV. DEVICE AND DESIGN CHALLENGES

A. SS DEGRADATION DUE TO NONIDEALITIES

Results presented in previous sections assume an ideal semiconductor bandstructure with no defects within the semiconductor body or at the gate oxide interface, and no band-tails extending into the bandgap. In actual semiconductor materials, the crystal structure has non-uniformities such as vacancies, interface states and impurities including dopants that are implanted as part of the desired structure. The main consequence of these non-uniformities is to add new electron/hole states inside the ideal bandgap, weakening the energy filtering which the TFET uses to achieve steep SS.

Defects can be modeled by introducing trap states into the existing band structure and allowing transport through these states having trap lateral size and energy spectrum varying with the defect type (Fig. 8). Not all traps have equal effect on TFET sub-threshold and off-current characteristics. The TFET is more susceptible to trap-induced degradation than the MOSFET, if the location and energy of the traps are assumed closer to N-TFET's worst case point such as inside the channel with energy levels 0.1~0.2V below the conduction band [14]. However, this issue is not limited to the TFET; the same trap-assisted tunneling process would cause leakage issues in a MOSFET through the GIDL (gate-induced drain leakage) process when traps are extended along the channel-drain junction of the transistor. Thus, the specific energy and location distribution of traps in the experimental devices will determine the level of SS degradation in the MOSFET and TFET I-V characteristics [15].

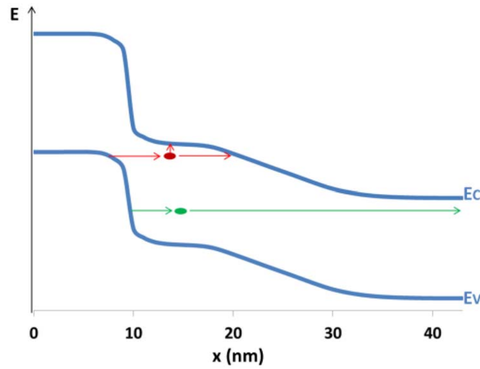

FIGURE 8. Average channel potential along the TFET transistor is shown for $V_{DS} = 0.3$ V and $V_G = 0$ V. A defect center that is close to conduction band (red dot), increases leakage tunneling current significantly due to the short distance to source and drain and possible scattering to the conduction band. Tunneling through a defect at other energy and spatial points (e.g., the green dot on the figure) will have a much smaller effect due to the still insignificant tunneling rate at long tunneling distances.

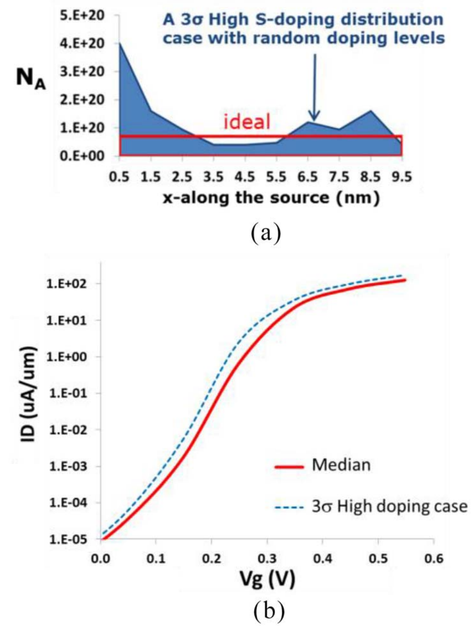

FIGURE 9. (a) Source doping profile and (b) its effect on I–V characteristics are compared for the ideal (red) and a 3 sigma random doping distribution case (blue). Even with such a significant tail case, increase of leakage current is much lower than expected from standard device parameter variation cases such as WFV.

Some experimental publications suggest, through temperature-dependent measurements, that the main reason for degraded TFET SS is the trap-assisted tunneling, which is in line with the theoretical studies [3]. The issue is inflated by the fact that the materials required for high drive-current TFETs are not the conventional Silicon, but instead are more novel materials that currently have high bulk and interface defects, and are yet to reach the maturity of Silicon. The experimental realization of TFET's significant SS advantage over MOSFET strongly depends on progress in the quality of these novel materials.

Another non-ideality concern is the density-of-states (DOS) extending in to the bandgap (band-tail) due to high doping density. This effect is due to the non-homogenous distribution of dopant atoms, creating different local potentials than that of a homogenous distribution. When statistically modeled over large areas, this effect can be represented as an exponential decay of DOS into the bandgap [16]. Since the TFETs considered for future technology nodes have very small cross-sections (5nm NW), the averaging effect is not valid. A more appropriate approach is to consider this issue as a part of source doping variation and study its effect on I_{OFF} variation. Although a more thorough analysis requires atomistic modeling of dopant atoms, here a 3σ case of random dopant defined source region potentials is studied to understand the effect of high-doping induced potential variation on TFET characteristics (Fig. 9). Results show that although TFET leakage current increases for this case study, the increase is significantly lower than any I_{OFF} increase due to 3σ V_t variation, implying that the high-doping induced band-tail is not the most critical issue TFET is facing. This statement is true for a high quality epitaxial layer where dopants are at the interstitial locations; defect generation due to heavy doping implant or low-quality epi-growth is expected to bring the same problems as those the presence of traps creates.

Other sources of recombination/generation mechanisms (such as SRH) are also sources of leakage and strongly depend on the material quality.

B. SCALING REQUIREMENTS

In TFETs with narrow bandgap and long gate-length, ambipolar leakage is the main reason for SS degradation and high-I_{OFF}. However, in short gate-length TFETs, the shorter tunneling path between source and drain aggravates direct source-to-drain tunneling leakage, while the increased bandgap due to confinement reduces the ambipolar leakage problem [Fig. 10(a)] [17]. Unlike in the MOSFET, oxide scaling does not improve short-channel-effects in the TFET significantly; instead body thickness scaling is the most important parameter. This is illustrated clearly in Fig. 10(b), when the device geometry is changed from double-gate to a gate-all-around. Although MOSFET subthreshold characteristics do not improve because they are already close to ideal, the TFET improves significantly. Thus, the body thickness requirement is much tighter for TFET than MOSFET, with 3nm nanowire recommended for $L_G = 9$nm. As L_G scaling continues, two-dimensional semiconductors with intrinsically superior electrostatics may be the better choice for TFETs [18].

C. TFET CIRCUIT LAYOUT ISSUES

The main challenge for TFET circuit layout arises from non-identical TFET source and drain contacts which require different doping type (p vs. n), doping levels (high vs. low) and materials (GaSb vs. InAs). This device design can

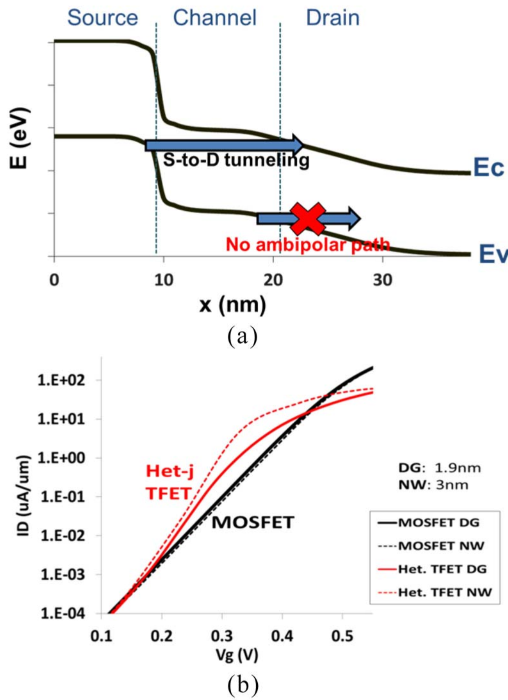

FIGURE 10. **(a) Band diagram for a $L_G = 13$ nm Het-j TFET with an undoped drain underlap, showing leakage current tunneling path directly from source to drain and no ambipolar leakage path at $V_{DS} = 0.3$ V and $V_G = 0$ V. (b) I–V characteristics after V_t adjustment for $L_G = 9$ nm TFET and MOSFET, each with DG and NW geometries. NW geometry provides better TFET characteristics whereas MOSFET is unchanged.**

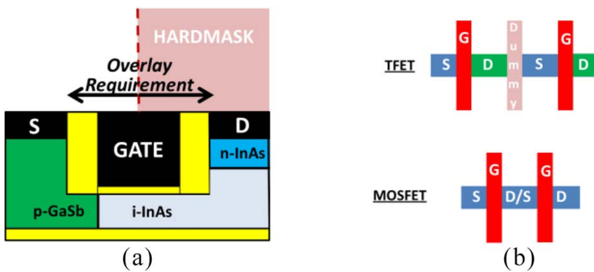

FIGURE 11. **(a) In order to process source and drain of a TFET separately, a lithography step with overlay alignment within the top of the gate and spacer region is required. (b) For logic circuits that have a serial connection of the same type of transistors (*N* or *P*), the TFET requires an additional contact region to accommodate connection of the drain of one transistor to the source of the other transistor.**

be fabricated using separate lithography steps for source and drain followed by etch and regrowth of the desired material. Overlay alignment of these lithography processes must stay within the width of the top of the gate, without encroaching the opposite contact for a ±Pitch/4 overlay requirement [Fig. 11(a)]. According to the ITRS Roadmap for 2018 technology node, the quarter pitch requirement is equal to ±7.5nm. This tight alignment rule may be a yield and cost concern for the TFET compared to the MOSFET, which does not require the different n+/p+ S/D.

The asymmetry of TFETs also has consequences for circuit layout density. Logic gates routinely require two or more N-type or P-type devices to be connected in series (i.e. the drain terminal of one device is connected to the source terminal of another device). This circuit arrangement has an efficient layout in a MOSFET technology because the source-to-drain connections of two series MOSFETs can share a single contact. This layout, however, is not possible with TFETs because the source drain contacts use different materials [Fig. 11(b)]. As a consequence, extra space is needed to achieve a series of two TFETs source-to-drain connection, reducing the density of basic TFET logic cells by an amount strongly dependent on the specific design rules of the technology node.

Although a vertical transistor architecture is possible for building TFET circuits [3], [4], this approach has its own challenges including the design and fabrication of the bottom contact. In this paper, we considered the conventional horizontal transistor architecture, which is a less disruptive approach to implement with respect to the state-of-the-art CMOS baseline.

D. CONSEQUENCES FOR UNI-DIRECTIONAL CONDUCTION

In contrast to MOSFETs which have symmetric I-V behavior, the TFET's source-channel-drain P-I-N structure results in vastly different I-V characteristics with positive or negative V_{DS} bias. An N-TFET with low negative V_{DS} bias has low conduction because the intrinsic P-I-N diode is forward biased below its turn-on voltage. An analogous condition exists for the P-TFET under positive V_{DS}. This V_{DS} dependence results in devices that only substantially conduct with a single V_{DS} polarity. As a consequence, for circuits whose operation requires bidirectional conduction, alternative topologies are required (See for example 6T SRAM cell [19]).

The V_{DS} dependence can result in subtle circuit differences as well. In both CMOS and TFET logic, switching voltages on wires and transistor terminals can capacitively transfer charge and create transient noise voltages. In CMOS, the charge transferred can be discharged though a MOSFET under both positive and negative drain-source biases, limiting noise voltage magnitude and duration. But in TFET logic, when the noise voltage forward biases its P-I-N structure (e.g. negative V_{DS} for N-TFET), the TFET has low conduction and cannot quickly dissipate the charge. The voltage on the signal may transition substantially above V_{DD} or below ground [20] and may cause timing errors and reliability concerns if not properly handled by design techniques. Reliability concerns need further study but are minimal because of TFET's lower supply voltages compared to those for conventional CMOS.

In other circuits, logic gates can benefit from uni-directional conduction. TFET's conductivity asymmetry with V_{DS} enables design of new MUX circuits with fewer transistors, lower power and better performance than CMOS implementations [20]. It remains to be seen if benefits from such circuits can compensate for the other problems

caused by source and drain asymmetry. Yet, the TFET's unique I-V characteristics opens up new avenues for circuit designers to make novel and significant improvements.

V. WHAT DOES TFET OFFER FOR PRODUCTS

The power-performance characteristics of the TFET present not only the opportunity of power reduction through low voltage operation but also present the challenge of meeting requirements on die size and peak performance. Clearly, chips only requiring frequencies lower than the TFET-CMOS crossover frequency can benefit from a TFET implementation, since for these frequencies the TFET provides lower power at iso-performance or higher performance at iso-power [Fig. 12(a)]. Also, an opportunity exists to provide benefits in higher performance products where the computation platforms impose a maximum power budget on the integrated circuit. For example a thin fan-less tablet computer can only dissipate so much power before it is too hot for handheld use. For these power-limited systems, increasing performance per Watt by reducing V_{DD} is essential for increasing total performance. This remains true even if operating frequencies decrease [Fig. 12(b)]. Without minimizing performance per Watt, it may not be possible to continuously power the entire integrated circuit. TFETs provide an option to enable continued voltage scaling for logic and a solution to this 'Dark Silicon' problem [21].

When considering die size and cost, the choice between MOSFET and TFET becomes more complicated. For applications that are efficiently parallelizable, a tradeoff exists between core count and core voltage (or frequency). Operating a circuit at a low frequency and low voltage improves performance per Watt but decreases performance per area (i.e. more cores are needed for iso-performance). For applications that are not entirely parallelizable, heterogeneous integration of high frequency CMOS cores with TFET cores was proposed as an effective approach [21].

The use of Turbo mode voltages in products presents another important challenge for the application of TFETs. In state-of-the-art CMOS, providing a short burst of high voltage/high frequency operation provides brief bursts of performance and side steps the steady-state thermal budgets or the need to grow die size. Due to the limited drive-current of TFET, CMOS provides higher peak performance for the high voltage Turbo mode operation.

VI. CONCLUSION

Device models generated from atomistic simulations are used to compare power-performance of CMOS and TFET logic. GaSb/InAs P-TFET drive-current is 1x to 0.5x of its N-TFET counterpart depending on the operating region. The complementary-TFET logic consumes only 54% of total CMOS power at iso-performance for the case where AF is 10%, circuit delay is 40ps and the effects of variation is included. There are many challenges to realizing TFETs in products including i) the requirement of high quality III-V materials and its oxides to remove the effects of trap-assisted tunneling and ii) very thin body dimensions to achieve good electrostatics. Also, TFET's layout density and circuit reliability issues due to its source/drain asymmetry need special attention. If these can be solved, TFETs offer longer battery life at a cost of some chip area, especially for extremely parallelizable products.

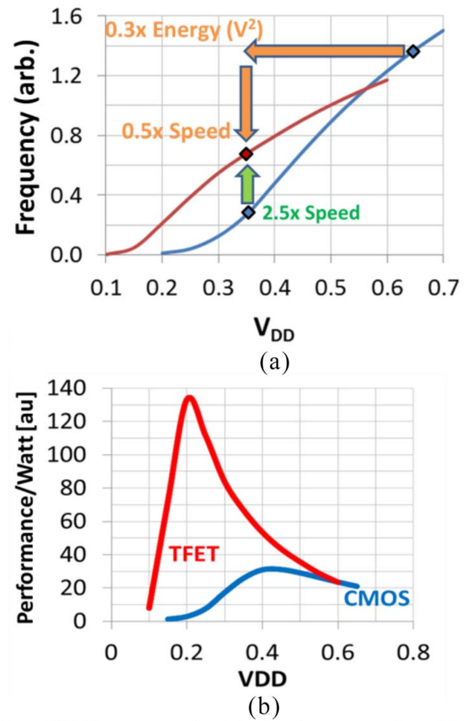

FIGURE 12. (a) Frequency of example CMOS and TFET logic is shown as a function of V_{DD}. TFET can operate at higher frequency than MOSFET with a V_{DD} below the crossover point. (b) Energy efficiency including leakage power of the logic operation versus V_{DD}. TFET's higher performance per watt than near-threshold CMOS means higher throughput is possible with parallelization in power-limited applications.

ACKNOWLEDGMENT

The authors would like to thank Raseong Kim for electrostatic simulations.

REFERENCES

[1] J. Appenzeller, Y.-M. Lin, J. Knoch, Z. Chen, and P. Avouris, "Comparing carbon nanotube transistors—The ideal choice: A novel tunneling device design," *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2568–2576, Dec. 2005.

[2] W. Y. Choi, B.-G. Park, J.-D. Lee, and T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007.

[3] D. K. Mohata *et al.*, "Demonstration of MOSFET-like on-current performance in arsenide/antimonide tunnel FETs with staggered hetero-junctions for 300mV logic applications," in *Proc. IEEE Electron Devices Meeting (IEDM)*, Washington, DC, USA, 2011, pp. 33.5.1–33.5.4.

[4] G. Dewey *et al.*, "Fabrication, characterization, and physics of III–V heterojunction tunneling field effect transistors (H-TFET) for steep sub-threshold swing," in *Proc. IEEE Electron Device Meeting (IEDM)*, Washington, DC, USA, 2011, pp. 33.6.1–33.6.4.

[5] K. Tomioka, M. Yoshimura, and T. Fukui, "Steep-slope tunnel field-effect transistors using III–V nanowire/Si heterojunction," in *Proc. VLSI Technol. (VLSIT) Symp.*, Honolulu, HI, USA, 2012, pp. 47–48.

[6] B. Ganjipour, J. Wallentin, M. T. Borgström, L. Samuelson, and C. Thelander, "Tunnel field-effect transistors based on InP-GaAs heterostructure nanowires," *ACS Nano,* vol. 6, no. 4, pp. 3109–3113, 2012.

[7] M. Luisier and G. Klimeck, "Simulation of nanowire tunneling transistors: From the Wentzel–Kramers–Brillouin approximation to full-band phonon-assisted tunneling," *J. Appl. Phys.*, vol. 107, no. 8, pp. 084507–084507-6, Apr. 2010.

[8] U. E. Avci *et al.*, "Energy efficiency comparison of nanowire heterojunction TFET and Si MOSFET at Lg=13nm, including P-TFET and variation considerations," in *Proc. IEEE Electron Devices Meeting (IEDM)*, Washington, DC, USA, 2013, pp. 33.4.1–33.4.4.

[9] U. E. Avci *et al.*, "Understanding the feasibility of scaled III–V TFET for logic by bridging atomistic simulations and experimental results," in *Proc. VLSI Technol. (VLSIT) Symp.*, Honolulu, HI, USA, 2012, pp. 183–184.

[10] *ITRS Roadmap.* [Online]. Available: http://www.itrs.net/reports.html

[11] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, "Tunnel field-effect transistor without gate-drain overlap," *Appl. Phys. Lett.*, vol. 91, Jun. 2007, Art. ID 053102.

[12] U. E. Avci, R. Rios, K. J. Kuhn, and I. A. Young, "Comparison of power and performance for the TFET and MOSFET and considerations for P-TFET," in *Proc. IEEE Conf. Nanotechnol. (IEEE-NANO)*, Portland, OR, USA, 2011, pp. 869–872.

[13] Y. X. Liu *et al.*, "On the gate-stack origin threshold voltage variability in scaled FinFETs and multi-FinFETs," in *Proc. VLSI Technol. (VLSIT) Symp.*, Honolulu, HI, USA, 2010, pp. 101–102.

[14] M. G. Pala and D. Esseni, "Interface traps in InAs nanowire tunnel-FETs and MOSFETs—Part I: Model description and single trap analysis in tunnel-FETs," *IEEE Trans. Electron Devices*, vol. 60, no. 9, pp. 2795–2801, Sep. 2013.

[15] Y. Qiu, R. Wang, Q. Huang, and R. Huang, "A comparative study on the impacts of interface traps on tunneling FET and MOSFET," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1284–1291, May 2014.

[16] P. Van Mieghem, "Theory of band tails in heavily doped semiconductors," *Rev. Mod. Phys.*, vol. 64, pp. 755–793, Jul. 1992.

[17] U. E. Avci and I. A. Young, "Heterojunction TFET scaling and resonant-TFET for steep subthreshold slope at sub-9nm gate-length," in *Proc. IEEE Int. Electron Devices Meeting (IEDM*), Washington, DC, USA, 2013, pp. 4.3.1–4.3.4.

[18] R. K. Ghosh and S. Mahapatra, "Monolayer transition metal dichalcogenide channel-based tunnel transistor," *IEEE J. Electron Devices Soc.*, vol. 1, no. 10, pp. 175–180, Oct. 2013.

[19] D. Kim *et al.,* "Low power circuit design based on heterojunction tunneling transistors (HETTs)," in *Proc. ACM/IEEE Int. Symp. Low Power Electron. Design (ISLPED)*, Rome, Italy, 2009, pp. 219–224.

[20] D. H. Morris, U. E. Avci, R. Rios, and I. A. Young, "Design of low voltage tunneling-FET logic circuits considering asymmetric conduction characteristics," *IEEE J. Emerg. Sel. Topics Circuits Syst.,* vol. 4, no. 4, pp. 380–388, Dec. 2014.

[21] K. Swaminathan *et al.*, "Steep-slope devices: From dark to dim silicon," *IEEE Micro*, vol. 33, no. 5, pp. 50–59, Sep./Oct. 2013.

UYGAR E. AVCI received the B.S. degrees in physics and electrical engineering from Bogazici University, Istanbul, Turkey, and the M.S. and Ph.D. degrees in applied physics from Cornell University, Ithaca, NY, USA, in 2003 and 2005, respectively. He joined Intel's Components Research Group, Hillsboro, OR, USA, in 2005, where he was leading floating body cell (FBC) memory experimental device design and scaling that demonstrated industry-leading FBC memory cells. His current research interests include the opportunities that beyond-CMOS devices offer to either replace or augment CMOS. He is currently the Principal Engineer, leading the research for charge-based beyond-CMOS devices and circuits. He was the recipient of Bogazici University President's Award. He served as the Fundamentals Class Chair and the Short Course Chair of the International SOI Conference in 2012 and 2013, respectively. He is an Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES.

DANIEL H. MORRIS received the B.S. degree from Northwestern University, Evanston, IL, USA, and the M.S. and Ph.D. degrees in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, USA. In 2012, he joined the Exploratory Integrated Circuit Group in the Components Research Department of the Intel Corporation, Hillsboro, OR, USA. At Intel, he works on the circuit and architectural aspects of beyond-CMOS logic and memory. His research interests include design-technology cooptimization, low power design, the tunneling FET and other charge- or spin-based logic and memory technologies.

IAN YOUNG received the bachelor's degree in electrical engineering and the master's degree in engineering science specialized in microwave communications from the University of Melbourne, Melbourne, VIC, Australia, and the Ph.D. degree in electrical engineering from the University of California, Berkeley, Berkeley, CA, USA. He joined Intel Corporation, Hillsboro, OR, USA, in 1983, and is currently a Senior Fellow and the Director of Exploratory Integrated Circuits in the Technology and Manufacturing Group, where he leads the research group exploring the future options for the integrated circuit in the beyond CMOS era. While he was at the University of California, Berkeley, he contributed to the pioneering research on the MOS switched-capacitor filter. Prior to Intel, he worked at Mostek Corporation, Carrollton, TX, USA. His contributions to Intel have been in the design of DRAMs, SRAMs, microprocessor circuit design, phase locked loops and microprocessor clocking, mixed-signal circuits for microprocessor high speed I/O links, RF CMOS circuits for wireless transceivers, and research for chip to chip optical I/O. He was the recipient of the 2009 International Solid-State Circuits Conference's Jack Raper Award for Outstanding Technology Directions Paper. He served on the Technical Program Committee of the ISSCC from 1992 to 2005, and as a Technical Program Committee Chairman in 2005. He served on the Symposium on VLSI Circuits Technical Program Committee from 1991 to 1998 and as its Technical Program Committee and Symposium Chairman. He was the Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS thrice and the Guest Editor of the IEEE JOURNAL OF SPECIAL TOPICS IN QUANTUM ELECTRONICS. He is currently the Editor-in-Chief of the IEEE JOURNAL OF EXPLORATORY SOLID-STATE COMPUTATION DEVICES AND CIRCUITS.