Received 1 October 2014; revised 21 November 2014; accepted 27 December 2014. Date of current version 22 April 2015.
The review of this paper was arranged by Editor A. C. Seabaugh.

Digital Object Identifier 10.1109/JEDS.2015.2388793

Vertical InAs-Si Gate-All-Around Tunnel FETs Integrated on Si Using Selective Epitaxy in Nanotube Templates

DAVIDE CUTAIA[1], KIRSTEN E. MOSELUND[1] (Senior Member, IEEE), MATTIAS BORG[1] (Member, IEEE), HEINZ SCHMID[1] (Member, IEEE), LYNNE GIGNAC[2], CHRIS M. BRESLIN[2], SIEGFRIED KARG[1], EMANUELE UCCELLI[1], AND HEIKE RIEL[1] (Senior Member, IEEE)

1 IBM Research—Zurich, Rüschlikon 8803, Switzerland
2 IBM Thomas J. Watson Research Center, Yorktown Heights, NY 10598 USA

CORRESPONDING AUTHOR: D. CUTAIA (e-mail: dcu@zurich.ibm.com)

This work was supported by the EU project E2SWITCH under grant agreement no. 619509.

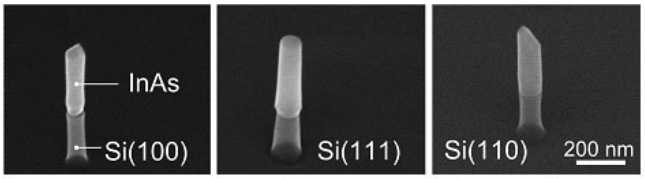
ABSTRACT In this paper, we introduce *p*-channel InAs-Si tunnel field-effect transistors (TFETs) fabricated using selective epitaxy in nanotube templates. We demonstrate the versatility of this approach, which enables III–V nanowire integration on Si substrates of any crystalline orientation. Electrical characterization of diodes and of TFETs fabricated using this method is presented; the TFETs exhibit a good overall performance with on-currents, I_{on} of 6 μA/μm ($|V_{GS}| = |V_{DS}| = 1$ V) and a room-temperature subthreshold swing (*SS*) of ~160 mV/dec over at least three orders of magnitude in current. Temperature-dependent measurements indicate that *SS* is limited by traps. We demonstrate improved TFET I_{on} performance by 1–2 orders of magnitude by scaling the equivalent oxide thickness from 2.7 to 1.5 nm. Furthermore, a novel benchmarking scheme is proposed to allow the comparison of different TFET data found in literature despite the different measurement conditions used.

INDEX TERMS Heterojunctions, III–V semiconductor materials, nanowires, tunnel diode, tunnel transistor, low-power electronics.

I. INTRODUCTION

The tunnel field-effect transistor (TFET) is considered the most promising electrical switch for ultra low-power electronics, because it should enable sub-k_BT/q switching and low-voltage operation. In general, TFETs are based on a gated *p-i-n* structure and can benefit from the immense technological development already done for MOSFET devices based on *n-i-n* or *p-i-p* structures for *n*- or *p*-type devices [1], [2]. Therefore, Si-based TFET technologies are the most mature and most scaled, and simple circuits have been demonstrated based on strained Si nanowires (NWs) [3]. Although the steepest subthreshold swings (*SS*) have been obtained in Si [4], [5], it likely will be difficult to achieve sufficiently high on-currents in pure Si devices because of the the large bandgap (E_G) of Si. Thus, boosters such as heterostructures are needed to lower the effective tunnel barrier and enable high on-currents. III-V TFETs based on different material systems have already been demonstrated and exhibit good performance metrics [6], [7]. However, integration of different material sets for both *n*- and *p*-channel TFETs on/with Si is a major challenge for III-V-based technologies. Here we explore the integration and performance of the InAs-Si material system as a *p*-channel TFET device. This heterojunction provides a small effective tunneling bandgap, which should result in high I_{on}, whereas the larger bandgap of Si in the channel and drain region gives a low I_{off} and lower interface trap density (D_{it}) than a low-bandgap III-V channel. Moreover, working on a Si platform allows us to benefit from all the established standard CMOS processes.

In this paper, we present a new approach to integrate individual InAs-Si heterostructure NW TFETs onto Si using selective epitaxy in nanotube templates (tmpl.NW). This approach allows the integration of NW TFETs on



	Tmpl. NW growth	Conv. NW growth
Substrate	Si (100), Si (110), Si (111)	Si (111) for vertical NWs
Device orientation	Defined by template layout	Along <111> growth direction
Device geometry & scaling	Defined by nanotube template, demonstrated 20nm NW diameter [8]	Scaling limited by growth kinetics
Heterostructure	Broad material set	Limited material set
Integration potential for TFET	High	Moderate

FIGURE 1. Top: example of InAs NWs grown vertically, independent of Si substrate orientation. Bottom: evaluation of the integration potential for template-assisted NW epitaxy compared with conventional NW epitaxy on Si.

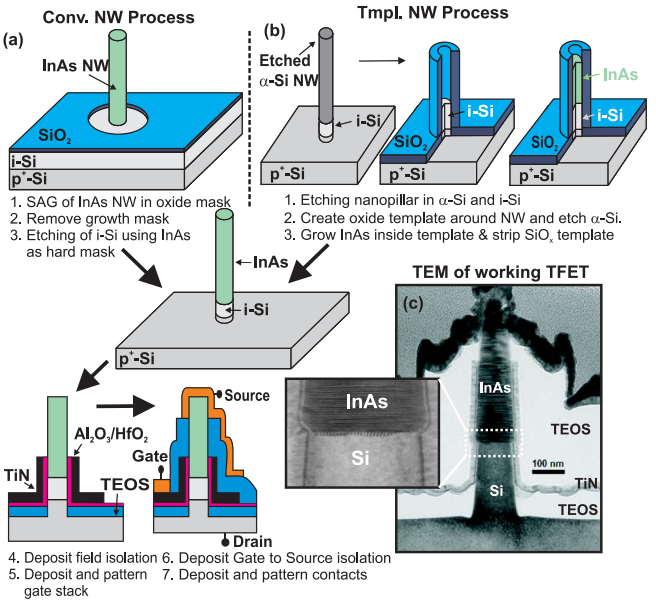


FIGURE 2. Schematic illustrating the two different integration methods. In conv.NW growth (a), InAs NWs are grown by selective area epitaxy in oxide openings and subsequently used as a hard mask for dry-etching into the Si. In the template-assisted method (b), InAs is grown selectively within an oxide tube. After NW growth, the two processes merge: a bottom field oxide is deposited as isolation and a gate stack is deposited and patterned, followed by isolation between gate and source and metal contacts. (c) Cross-sectional transmission electron microscopy (TEM) of a finished (tmpl.NW) device is shown including a magnification of the InAs/Si interface in the inset.

Si of any crystalline orientation. The basis for it is the template-assisted growth of vertical III-V NWs on Si substrates with (111), (110) and (100) orientations which we recently demonstrated (see Fig. 1) [8]. Former InAs-Si NW *p*-type TFETs we have demonstrated [9] are based on selective area growth (SAG) of InAs NWs within patterned thin oxide films. This conventional NW (conv.NW) process allows the growth of only (111) InAs NWs and thus requires Si (111) substrates. Compared with conv.NW growth, the template-assisted approach provides a much greater processing window as the dimensions and orientations are pre-determined by the template and parasitic radial growth is eliminated [10]. This provides a higher potential for NW diameter scaling than the conv.NW approach. The advantages of the tmpl.NW integration approach with respect to conv.NW growth are summarized in Fig. 1.

Here, we show the first *p*-type InAs-Si TFETs based on this new template-assisted epitaxial growth. These TFETs are initially benchmarked against InAs-Si TFETs fabricated using conv.NW growth [9]. Furthermore, by scaling the equivalent oxide thickness (EOT) from 2.7 to 1.5 nm, the I_{on} performance of tmpl.NW devices is improved by about two orders of magnitude. Based on the template-assisted method, we demonstrate in addition the possibility of a source replacement approach which could simplify co-integration of *p*-type and *n*-type III-V TFETs onto the same Si substrate. Finally, we also propose an alternative benchmarking of TFETs, allowing a better comparison of devices measured at different biasing conditions.

II. DEVICE FABRICATION

The main device processing steps are illustrated in Fig. 2. The process flow for the conv.NW device is described in more detail elsewhere [9]. In both cases, the intrinsic Si channel (*i*-Si, $N_A \sim 10^{15}$ cm^{-3}) is first grown by molecular beam epitaxy (MBE) at 750°C on heavily doped *p*-type Si wafers (drain). For the nanotube template process, sacrificial NWs are defined by electron-beam lithography and HBr:O_2 etching of a 500-nm-thick deposited amorphous Si (α-Si) layer, 120 nm *i*-Si channel and 80 nm of *p*-Si substrate (see Fig. 2). SiO_x nanotubes with an inner diameter of 100 nm are created by coating the Si NWs using plasma-enhanced chemical vapor deposition (PECVD) of Tetraethyl orthosilicate (TEOS) at 400°C and opening the top part of the oxide by dry etching. Subsequently, the α-Si is etched selectively with respect to the Si (111) using 25% Tetramethylammonium hydroxide (TMAH) at 80°C. The Si (111) substrate is chosen based on greater etch selectivity in the TMAH etching step, which allows us to define the channel length accurately; but the process is compatible with standard Si (100) substrates as shown in Fig. 1, making our approach CMOS compatible.

Si-doped (*n*-type) InAs NWs (source) are then selectively and epitaxially grown inside the nanotubes at 520°C. From earlier calibrations [11], we estimate an InAs doping concentration of around 4×10^{17} cm^{-3}. The oxide template is removed around the InAs NWs, and a gate-all-around (GAA) gate stack of Al_2O_3 (5.5 nm) or Al_2O_3/HfO_2 (2.2 nm, 2.4 nm) for the scaled EOT devices and TiN/SiO_2 (20 nm, 20 nm) is deposited by atomic layer deposition (ALD) at 250°C and 300°C, respectively. Then, photoresist is spin-coated and etched back by RIE to define the gate length. The SiO_2 cap is dry etched and the resist is stripped in acetone to reveal the top part of TiN, which is wet

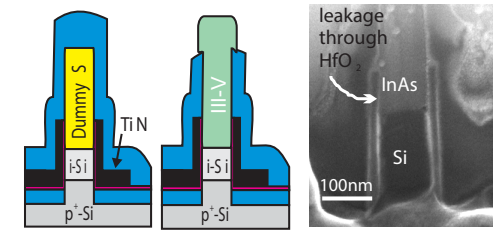


FIGURE 3. **Replacement source process: schematic image illustrating the additional process steps for a replacement source process. The numbering refers to the initial steps listed in Fig. 2. Scanning electron micrograph showing the cross section of the finalized device.**

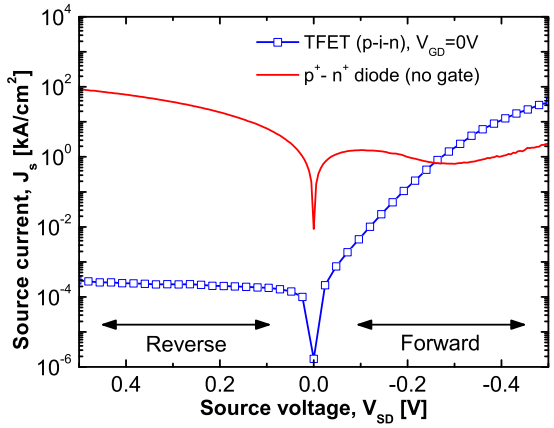


FIGURE 4. **Diode characteristics measured on TFET (p-i-n) structure at V_{GD} = 0 V (blue squares). A fabricated p^+-n^+ NW diode (without gate) with NDR is shown for reference.**

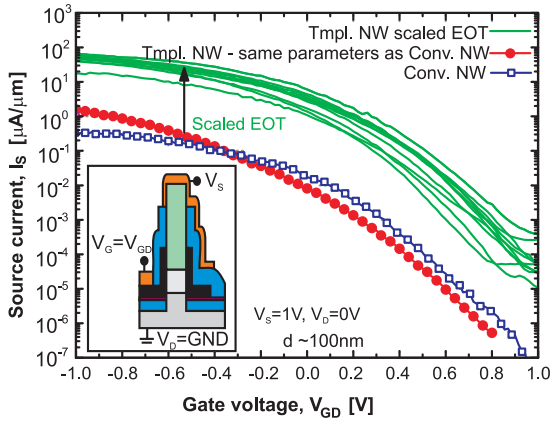


FIGURE 5. **Comparison of *p*-type TFETs made by the tmpl.NW and the conv.NW integration approach. For tmpl.NW TFETs, the performances match that of the conv.NW devices—as expected, because no other parameters were changed. The green lines without symbols correspond to a batch of tmpl.NW TFETs with scaled EOT = 1.5 nm versus EOT = 2.7 nm for the other devices. To comply with previous measurements, the Si (drain) is grounded, whereas a bias is applied to the InAs (source). Inset shows biasing scheme.**

etched using an ammonium peroxide mixture (APM) solution of NH_3(29%):H_2O_2:DI (1:2:5) at 60°C. The remaining SiO_2 layer protects the TiN etching on the sidewall. Subsequently, the gate is isolated from the source using PECVD of TEOS at 350°C. Then, resist is spin-coated and etched back by RIE, followed by wet etching of TEOS in BHF (7:1) solution to open the top part of the InAs NW. Metal evaporation of Ni/Au contacts and lift-off finalize the device.

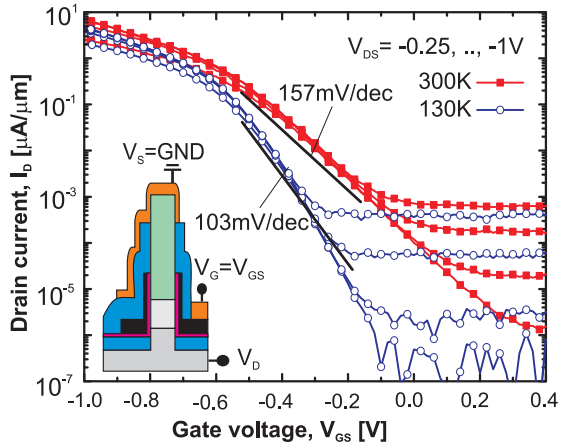
Alternatively, we explored the fabrication of a source-replacement TFET, using a dummy source that was replaced by InAs after full gate stack formation, see illustration in Fig. 3. In this case, a dielectric gate stack consisting of SiO_2/Al_2O_3/HfO_2 (2 nm, 3 nm, 2 nm) was deposited on the Si dummy source. After etching of the Si dummy source in TMAH and a HF clean, the InAs source was selectively grown in place. Although the full process flow could be finalized, electrical measurements on current devices revealed a large leakage path through the remaining HfO_2 dielectric in the top part of the InAs segment so that proper TFET functionality could not yet be established.

III. ELECTRICAL CHARACTERIZATION

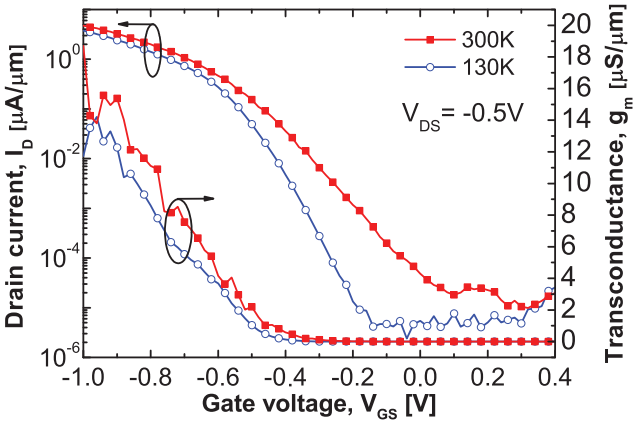
Traditionally the presence of a region of negative differential resistance (NDR) in the output characteristics of a TFET device has served as means for verifying whether the measured current in fact originates from the tunnel junction. Such a characteristic is shown for a Si-InAs p^+-n^+ diode in Fig. 4 (solid red line). However, the TFETs reported here are all based on *p-i-n* structures with a lower doping in the InAs part than the p^+-n^+ diode [12], which will therefore not exhibit an NDR unless biased at very large negative gate potential. $I(V)$ characteristic for the fabricated *p-i-n* TFET is reported in Fig. 4.

In Fig. 5 the performance of the tmpl.NW TFETs (red solid circles) is compared with the conv.NW TFETs (blue open squares). Both types of TFETs having the same parameters such as diameter, gate stack, etc achieve the same performance. The results manifest that the same quality of heterojunction is obtained by the templated approach as has been also seen in InAs-Si tunnel diodes before [8]. The green solid lines correspond to tmpl.NW TFETs with the EOT scaled to 1.5 nm. The EOT scaling boosts the current of the tmpl.NW devices by about one to two orders of magnitude to 50 μA/μm at $V_{GS} = V_{DS} = |1$ V|. Since InAs is a direct bandgap material with its lowest E_G at the Γ-valley, the ON state can be described in a first approximation by the Wentzel–Kramers–Brillouin (WKB) method. Scaling the EOT from 2.7 nm to 1.5 nm should increase the tunneling probability by a factor of 40X, which qualitatively fits well to our experimental data. However, also the OFF state current increases due to large leakage at this high voltage bias ($|V_{DS}| = 1$ V).

The biasing scheme in Fig. 5 used a positive V_S bias to the InAs source (negative bias region for the *p-i-n* diode), while grounding the substrate (drain). In this configuration, the barrier at the tunnel junction is highly dependent on V_S as a change in V_{SD} also results in a direct change in V_{GS},



(a)



(b)

FIGURE 6. **(a) $I_D(V_{GS})$ at 300 K and 130 K of 100-nm-diameter GAA NW *p*-type TFET with EOT ~ 1.5 nm. The source (n-InAs) is grounded, while the drain (p-Si) is swept with −0.25 V bias step, see inset for biasing. I_{on} maximum of 6 μA/μm at $V_{GS} = V_{DS} = -1$ V is measured at 300 K. (b) Normalized transconductance at 300 K and 130 K for $|V_{DS}| = 0.5$ V and the respective transfer characteristic.**

causing a threshold voltage shift (V_t). This increases the I_{on} measured compared to normal TFET operation. For real device operation, a more appropriate biasing scheme (used in the subsequent figures) is based on the use of a negative V_D combined with a grounded source potential. In this case, the V_{GS} value determining the position of the bandgap in the channel is no longer directly influenced by the value of V_{DS}, thus the shift in the transfer characteristics disappears [Fig. 6(a)].

The transfer characteristics, $I_D(V_{GS})$, and normalized transconductance, g_m, are shown in Fig. 6(b) for two different temperatures. We measured an I_{on} of ~ 0.2 μA/μm at $|V_{GS}| = |V_{DS}| = 0.5$ V and I_{on} of ~ 6 μA/μm at $|V_{GS}| = |V_{DS}| = 1$ V and an I_{on}/I_{off} ratio of ~10^6. The steeper *SS* obtained at 130 K is evidence of the presence of traps, both at the InAs-Si junction [13] and at the gate dielectric–semiconductor interface, which limits sub-60mV/decade operation. As the temperature is reduced, the traps are gradually frozen out

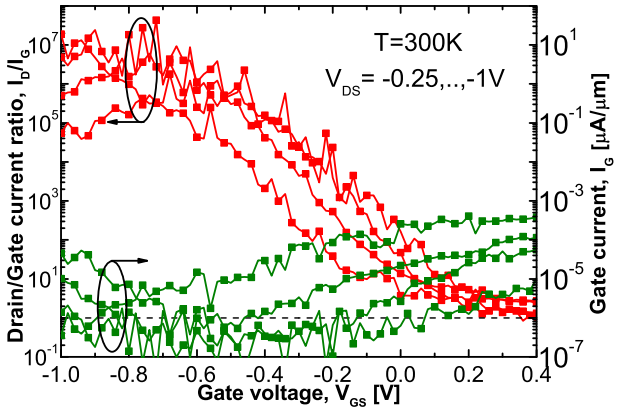


FIGURE 7. **Ratio of drain and gate currents (red) and gate leakage I_G(green) of the device shown in Fig. 6(a) at 300 K. Gate leakage does not dominate device performance. The dotted line indicates $I_D/I_G = 1$.**

which explains the improvement of the *SS* at lower temperatures. Concerning the traps stemming from dislocations at the InAs-Si junction, these may be reduced by scaling the nanowire diameter below a critical dimension, as have been shown in [14]. Traps at the high-*k*/semiconductor interface are responsible for the large value of extracted D_{it}, around 10^{12} cm^{-2}·eV^{-1} for single Si NWs, which is about an order of magnitude larger than for planar references with the same gate stack, and ~10^{13} cm^{-2}·eV^{-1} for InAs NWs [15]. To some extent these traps could explain the rather large value of *SS*. Thus, diameter scaling and gate stack optimization could be both beneficial to obtain a sub-60 mV/dec slope.

Fig. 7 shows I_D/I_G vs. V_{GS}, indicating that gate leakage is not a limiting factor in the region of interest for these devices, although the gate leakage limits the minimum I_{off} for large V_{DS}. The increase of I_{off} seen in Fig. 6(a) is not due to the intrinsic device performance but it is a result of gate leakage in this region. The TEM image in Fig. 2 shows that the gate has a substantial overlap on the InAs segment (source), hence it "collects" leakage from a greater region than the "active" region around the tunnel junction. Moreover, this overlap, and hence gate leakage, may vary among devices. However it only plays a role in the OFF state and does not influence the subthreshold swing outside of this region.

In Fig. 8 *SS* is displayed as a function of I_D at $V_{DS} = -0.25$ V; about a value of 160 mV/dec for more than three decades of current at 300 K is reached. The TFET output characteristic exhibits excellent current saturation and is not limited by series resistance in the linear region (Fig. 9). The I_{on} is almost independent of the temperature as expected for a band-to-band tunneling (BTBT) regime, which is consistent for both conv.NW and tmpl.NW devices (Fig. 10).

IV. TUNNEL FET BENCHMARKING

TFET benchmarking is extremely challenging because the biasing conditions and hence the cited values of *SS*, I_{on} etc. differ. Thus, references often cite only selected figures of merit, such as a small *SS* or a large I_{on}, which do not

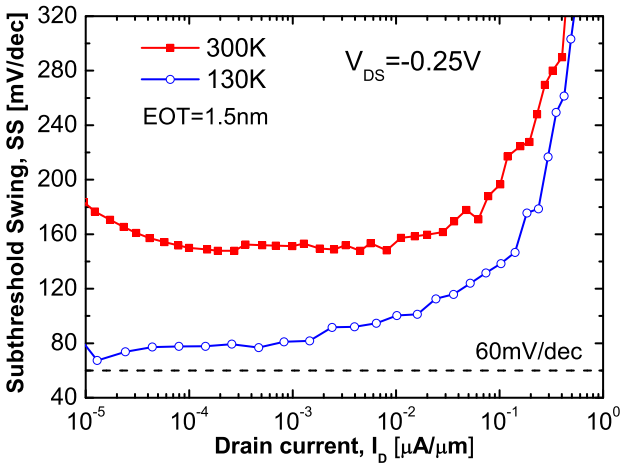


FIGURE 8. SS versus I_D for the device shown in Fig. 6(a), at 300 K and 130 K. At 130 K, the average SS is reduced to 75 mV/dec over the exponential tail.

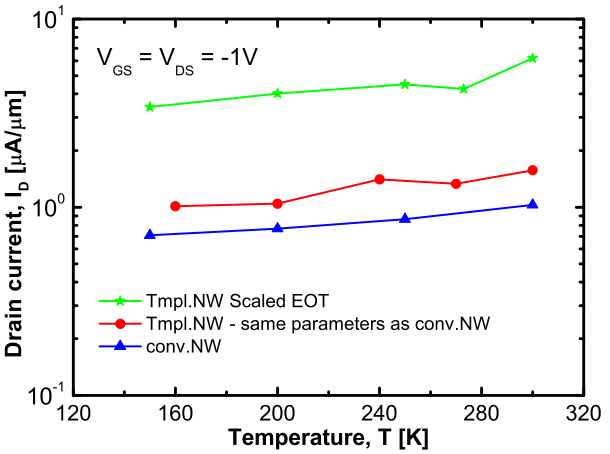


FIGURE 10. I_{on} dependence on temperature for conv.NW and tmpl.NW TFET batches. As expected for a TFET, all devices exhibit no significant change in I_{on} with temperature since BTBT dominates in this region.

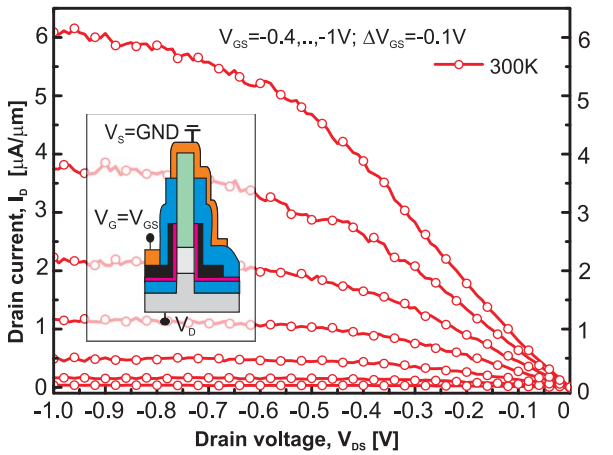


FIGURE 9. Output characteristics of 100-nm-diameter GAA NW TFET. The source (n-InAs) is fixed to ground, and a voltage bias is applied on the drain (p-Si) side. Current saturation demonstrates good electrostatic control of the Si:InAs junction. Inset shows biasing scheme.

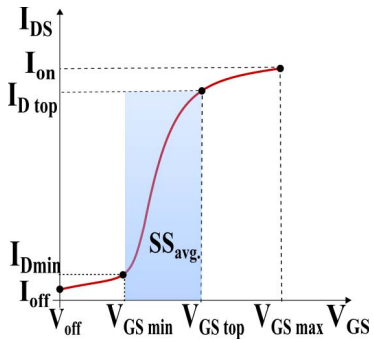


FIGURE 11. Schematic illustrating the corresponding parameters used for the calculation of *SS* in Eq. 1.

give the full picture. This aggravates a fair benchmarking. In addition, usually only the minimum *SS*, which is not a useful figure of merit for actual device operation, is reported. Here, we attempt a fair benchmarking approach by plotting *SS* as

$$SS = \left(\frac{V_{GS} - V_{GS\,\min}}{\log\left(\frac{I_D}{I_{D\,\min}}\right)} \times 1000 \right) \qquad (1)$$

where I_{Dmin} is the minimum chosen I_D value, and V_{GSmin} is the corresponding V_{GS} value (see Fig. 11). *SS* is then plotted vs. I_D/V_{DS}, as shown in Fig. 12. As most values of I_D of interest lie within the linear region, this should reduce the effect of choosing a different V_{DS} value. For this particular figure, we used the average *SS* ($SS_{avg.}$) extracted over the entire part of the exponential slope of I_D until the latter starts to flatten out (I_{Dtop}) and measured it from I_{Dmin} vs. I_D/V_{DS} for a large number of references. The results are displayed using an exponential scale for *SS*, as this highlights the differences in the low *SS* regime better.

All TFETs in the benchmarking plot are biased at $|V_{DS}| \geq 0.25$V. The choice of a lower V_{DS} could impact *SS* since lower V_{DS} provides in principle lower I_{Dmin}, thus also the average slope would be reduced. However, this is only true when I_{Dmin} has not reached a saturation value, I_{off}, which is determined by intrinsic device physics and/or gate leakage. Hence, if a device at low V_{DS} exhibits a small I_{off}, steeper *SS* and high I_{on}, then it will show the best performance tradeoff. Thus, the criteria to achieve a small I_{off} is already taken into account in this benchmarking method. Moreover, we consider it as a fair benchmarking plot for TFETs since a low V_{DS} operation is desirable for low-power applications, while still the devices being able to achieve high currents in the ON state. Determining the point of I_D at the top of the slope is somewhat subjective, but should have been counteracted by the measures discussed before. If one chooses a larger I_D value (higher V_{GS} and/or V_{DS}), this will be offset by a deteriorated *SS*. As a result, individual values will change, but when comparing devices, the general picture does not change significantly, i.e., it is still

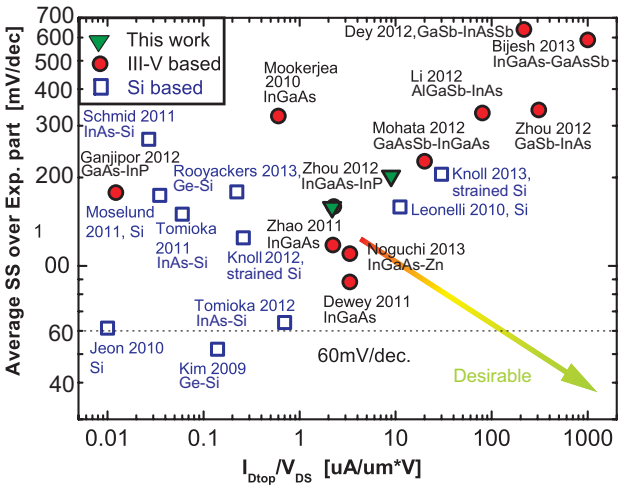


FIGURE 12. **Average *SS* measured over the entire exponential rise of current from I_{Dmin} (chosen to give the steepest slope) versus I_D/V_{DS} plotted for a number of published TFET data; *SS* shown on log scale. If a larger value of I_{Dtop} is chosen, this will be penalized by a correspondingly higher *SS*. All data points are measured at room temperature and DC biased. The green triangles denote two different tmpl.NW devices with scaled EOT.**

clear which devices are better since here the new performance metric is the trade-off between high I_{on} and small *SS*. Therefore, we believe this new benchmarking to be a fair comparison. In a similar fashion, one may choose to plot the values obtained over three decades of current or measured to the maximum value of I_D. We must stress though that it is important to evaluate devices on the same basis, i.e., choosing an appropriate number of decades of current. Moreover, different technologies provide a varying degree of potential for further scaling and device optimization, which is not taken into account here. Data points are estimated from published graphics, based on our best efforts, thus this can provide a source of variability. Also, values may deviate from cited data if the biasing conditions used were not the same, for example different V_{DS} or V_{GS}. All data points are measured at room temperature, DC-biased and taken from the "best device."

V. CONCLUSION

We have reported *p*-channel InAs-Si TFETs based on NWs fabricated inside nanotube templates and integrated on Si. First we demonstrated that the performance of the devices fabricated using nanotube templates match that of devices based on conventional nanowire growth process. Secondly, we boosted the I_{on} current to 6 μA/μm by scaling the EOT. Furthermore, we have introduced a "fair" benchmarking of TFET devices, and found that the performance of our devices are comparable with that of other state-of-the-art TFETs, however their real merit lies in their integration potential. The new template approach provides a unique integration capability for GAA III-V heterostructure TFETs on Si of any crystalline orientation.

ACKNOWLEDGMENTS

The authors would like to thank L. Czornomaz and M. Tschudy for technical support and G. Signorello, A. M. Ionescu, and W. Riess for scientific discussions and support.

REFERENCES

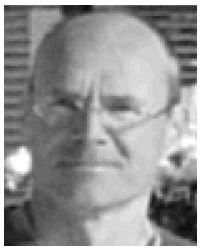
[1] A. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, Nov. 2011, pp. 329–337.
[2] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, Dec. 2010, pp. 2095–2110.
[3] L. Knoll *et al.*, "Demonstration of improved transient response of inverters with steep slope strained Si NW TFETs by reduction of TAT with pulsed I-V and NW scaling," in *Proc. Tech. Dig. IEEE Int. Electron Device Meeting (IEDM)*, Washington, DC, USA, 2013, pp. 4.4.1–4.4.4.
[4] K. Jeon *et al.*, "Si tunnel transistors with a novel silicided source and 46mV/dec swing," in *Proc. Symp. VLSI Tech.*, Honolulu, HI, USA, 2010, pp. 121–122.
[5] S. H. Kim, H. Kam, C. Hu, and T.-J. K. Liu, "Germanium-source tunnel field effect transistors with record high I_{ON}/I_{OFF}," in *Proc. Symp. VLSI Tech.*, Honolulu, HI, USA, 2009, pp. 178–179.
[6] G. Dewey *et al.*, "Fabrication, characterization, and physics of III-V heterojunction tunneling field effect transistors (H-TFET) for steep sub-threshold swing," in *Proc. Tech. Dig. IEEE Int. Electron Device Meeting (IEDM),* Washington, DC, USA, 2011, pp. 33.6.1–33.6.4.
[7] M. Noguchi *et al.*, "High Ion/Ioff and low subthreshold slope planar-type InGaAs tunnel FETs with Zn-diffused source junctions," in *Proc. Tech. Dig. IEEE Int. Electron Device Meeting (IEDM),* Washington, DC, USA, 2013, pp. 28.1.1–28.1.4.
[8] M. Borg *et al.*, "Vertical III-V nanowire device integration on Si (100)," *Nano Lett.*, vol. 14, no. 4, 2014, pp. 1914–1920.
[9] K. E. Moselund *et al.*, "InAs–Si nanowire heterojunction tunnel FETs," *IEEE Electron Device Lett.,* vol. 33, no. 10, Oct. 2012, pp. 1453–1455.
[10] P. D. Kanungo *et al.*, "Selective area growth of III-V nanowires and their heterostructures on silicon in a nanotube template: Towards monolithic integration of nano-devices," *Nanotechnology*, vol. 24, no. 22, 2013, Art. ID 225304.
[11] H. Ghoneim *et al.,* "In situ doping of catalyst-free InAs nanowires," *Nanotechnology*, vol. 23, no. 50, 2012, Art. ID 505708.
[12] H. Riel *et al.*, "InAs-Si heterojunction nanowire tunnel diodes and tunnel FETs," in *Proc. Tech. Dig. IEEE Int. Electron Device Meeting (IEDM)*, San Francisco, CA, USA, 2012, pp. 16.6.1–16.6.4.
[13] C. Bessire *et al.*, "Trap-assisted tunneling in Si-InAs nanowire heterojunction tunnel diodes," *Nano Lett.*, vol. 11, no. 10, 2011, pp. 4195–4199.
[14] K. Tomioka, M. Yoshimura, and T. Fukui, "Sub 60 mV/decade switch using an InAs nanowire-Si heterojunction and turn-on voltage shift with a pulsed doping technique," *Nano Lett.*, vol. 13, no. 12, 2013, pp. 5822–5826.
[15] P. Mensch *et al.,* "Interface state density of single vertical nanowire MOS capacitors," *IEEE Trans. Nanotechnol.,* vol. 12, no. 3, May 2013, pp. 279–282.
[16] R. Gandhi *et al.*, "Vertical Si-nanowire n-Type tunneling FETs with low subthreshold swing (50 mV/decade) at room temperature," *IEEE Electron Device Lett.*, vol. 32, no. 4, Apr. 2011, pp. 437–439.
[17] B. Ganjipour, J. Wallentin, M. T. Borgström, L. Samuelson, and C. Thelander, "Tunnel field-effect transistors based on InP-GaAs heterostructure nanowires," *ACS Nano*, vol. 6, no. 4, 2012, pp. 3109–3113.
[18] G. Zhou *et al.*, "Novel gate-recessed vertical InAs/GaSb TFETs with record high ION of 180 μA/μm at VDS = 0.5 V," in *Proc. Tech. Dig. IEEE Int. Electron Device Meeting (IEDM)*, San Francisco, CA, USA, 2012, pp. 32.6.1–32.6.4.
[19] G. Zhou *et al.*, "InGaAs/InP tunnel FETs with a subthreshold swing of 93 mV/dec and I_{ON}/I_{OFF} ratio near 10^6," *IEEE Electron Device Lett.*, vol. 33, no. 6, Jun. 2012, pp. 782–784.

[20] S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, and S. Datta, "Temperature-dependent I–V characteristics of a vertical In0.53Ga0.47As tunnel FET," *IEEE Electron Device Lett.*, vol. 31, no. 6, Jun. 2010, pp. 564–566.
[21] R. Li *et al.*, "AlGaSb/InAs tunnel field-effect transistor with on-current of 78uA/um at 0.5 V," *IEEE Electron Device Lett.*, vol. 33, no. 3, Mar. 2012, pp. 363–365.
[22] H. Schmid *et al.*, "Fabrication of vertical InAs-Si heterojunction tunnel field effect transistors," in *Proc. Device Res. Conf.*, Santa Barbara, CA, USA, 2011, pp. 181–182.
[23] D. Mohata *et al.,* "Barrier-engineered arsenide–Antimonide heterojunction tunnel FETs with enhanced drive current," *IEEE Electron Device Lett.,* vol. 33, no. 11, Nov. 2012, pp. 1568–1570.
[24] D. Leonelli *et al.*, "Optimization of tunnel FETs: Impact of gate oxide thickness, implantation and annealing conditions," in *Proc. Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sevilla, Spain, 2010, pp. 170–173.
[25] K. Tomioka and T. Fukui, "Tunnel field-effect transistor using InAs nanowire/Si heterojunction," *Appl. Phys. Lett.*, vol. 98, Feb. 2011, Art. ID 083114.
[26] K. Tomioka, M. Yoshimura, and T. Fukui, "Steep-slope tunnel field-effect transistors using III-V nanowire/Si heterojunction," in *Proc. Symp. VLSI Technol.,* Honolulu, HI, USA, 2012, pp. 47–48.
[27] R. Rooyackers *et al.*, "A new complementary hetero-junction vertical tunnel-FET integration scheme," in *Proc. Tech. Dig. IEEE Int. Electron Device Meeting (IEDM)*, Washington, DC, USA, 2013, pp. 4.2.1–4.2.4.
[28] L. Knoll *et al.*, "Inverters with strained Si nanowire complementary tunnel field-effect transistors," *IEEE Electron Device Lett.,* vol. 34, no. 6, Jun. 2012, pp. 813–815.
[29] H. Zhao *et al.*, "InGaAs tunneling field-effect-transistors with atomic-layer-deposited gate oxides," *IEEE Trans. Electron Device*, vol. 58, no. 9, Sep. 2011, pp. 2990–2995.
[30] A. W. Dey *et al.*, "High-current GaSb/InAs(Sb) nanowire tunnel field-effect transistors," *IEEE Electron Device Lett.*, vol. 34, no. 2, Feb. 2013, pp. 211–213.
[31] R. Bijesh *et al.*, "Demonstration of In0.9Ga0.1As/GaAs0.18Sb0.82 near broken-gap tunnel FET with ION = 740 uA/um, GM = 700uS/um and gigahertz switching performance at VDs = 0.5V," in *Proc. IEEE Int. Electron Device Meeting (IEDM)*, Washington, DC, USA, 2013, pp. 28.2.1–28.2.4.

DAVIDE CUTAIA received the joint M.Sc. degree in nanotechnology engineering from the Politecnico di Torino, Turin, Italy, the Institut Polytechnique de Grenoble, Grenoble, France, and the Swiss Federal Institute of Technology in Lausanne (EPFL), Lausanne, Switzerland, in 2013. He was at IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA, as an intern and he is currently employed at IBM Research—Zurich, Zurich, Switzerland, as a Ph.D. student. He is pursuing the PhD degree with EPFL. His current research interests are the fabrication, characterization, and physical modeling of nanodevices.

KIRSTEN E. MOSELUND (SM'13) received the M.Sc. degree in engineering from the Technical University of Denmark, Kongens Lyngby, Denmark, and the Ph.D. degree in microelectronics from the Swiss Federal Institute of Technology in Lausanne (EPFL), Lausanne, Switzerland, in 2003 and 2008, respectively. In 2008, she joined IBM Research—Zurich, Zurich, Switzerland, where she is working as a Research Staff Member with Materials Integration and Nanoscale Devices Group. Her research interests include semiconductor physics, advanced transistor concepts, and nanoelectronic fabrication technology.

MATTIAS BORG (M'03) received the M.Sc. degree in engineering physics and the Ph.D. degree in physics from the Lund Institute of Technology, Lund, Sweden, in 2007 and 2012, respectively. He was a Post-Doctoral Researcher with IBM Research—Zurich, Zurich, Switzerland, for two years, where he is currently a Research Staff Member. His research interests include the synthesis and processing of advanced nanostructure devices for electronic applications.



HEINZ SCHMID (M'05) received his Physics apprenticeship diploma in 1988 and joined IBM Research - Zurich, Zurich, Switzerland in 1984, where he is currently a Senior Engineer. He has worked on low-energy electron holography and ion field emission sources, as well as on emerging lithographic techniques, including microfluidic systems. His current research interest comprises III–V devices and integration on Si.

LYNNE GIGNAC received the B.S. and M.S. degrees in ceramic engineering from the University of Illinois at Urbana-Champaign, Urbana, IL, USA, and the Ph.D. degree in materials science and engineering from the University of Arizona, Tucson, AZ, USA. In 1988, she joined IBM Systems and Technology Group, East Fishkill, NY, USA, and transferred to IBM Thomas J. Watson Research Center, Yorktown, NY, USA, in 1995. She is currently a Research Staff Member at IBM Thomas J. Watson Research Center where she studies semiconductor materials using electron microscopy. She was the recipient of the Microscopy Society of America Chuck Fiori Outstanding Technologist Award in 2009.

CHRIS M. BRESLIN received the B.S. degree in computer science and applied mathematics and the M.S. degree in nanoscale science and engineering from University at Albany, SUNY, Albany, NY, USA, in 2005 and 2011, respectively. His master's thesis project consisted of developing a model to determine the effects of secondary electron emission characteristics on charged matter beam induced depositions. He currently holds a position at the IBM Thomas J. Watson Research Center, Yorktown, NY, USA, supporting advanced research projects through TEM preparation and TEM preparation development techniques.

SIEGFRIED KARG received the Ph.D. degree in physics, specializing on the materials science of organic and polymer devices and resistive memories based on oxides. He joined IBM Research—Zurich, Zurich, Switzerland, in 2000. His current interests are electronic and thermoelectric properties as well as strain effects of semiconducting nanowires and their applications. He has authored over 80 publications and holds over 30 patents.

EMANUELE UCCELLI received the B.S. and M.S. degrees in materials science from the University of Milano-Bicocca, Milan, Italy, in 2004, and the Ph.D. degree in physics from the Technical University of Munich, Munich, Germany, specializing on the synthesis and characterization of InAs nanostructures arrays by molecular beam epitaxy, in 2008. In 2009, he joined the École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, as a Post-Doctoral Research Associate, working on GaAs nanowires heterostructures for solar cell applications. He joined IBM Research—Zurich, Zurich, Switzerland, in 2011, where he is currently working on the development of new materials and processes for the technology integration of III–V devices on silicon CMOS platform for both electronics and photonics applications.

HEIKE RIEL (SM'07) received the Ph.D. degree in physics from the University of Bayreuth, Bayreuth, Germany, specializing on the optimization of multilayer organic light-emitting devices, in 2002. She is a IBM Fellow and the Manager of Materials Integration and Nanoscale Devices with IBM Research—Zurich, Zurich, Switzerland. She joined IBM in 1997 as Diploma student, and then as Ph.D. student, and became a Research Staff Member in 2003. Her current research interests are semiconducting nanowires for various applications, including steep slope devices to improve power efficiency.