1T Capacitor-Less DRAM Cell Based on Asymmetric Tunnel FET Design

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ABSTRACT In this work we propose and demonstrate the use of a Tunnel FET (TFET) as capacitorless DRAM cell based on TCAD simulations and experiments. We report more experimental results on Tunnel FETs implemented as a double-gate (DG) fully-depleted Silicon-On-Insulator (FD-SOI) devices. The Tunnel FET based DRAM cell has an asymmetric body and a partial overlap of the top gate (L_{G1}) with a total overlap of the back gate over the channel region (L_{G2}). A potential well is created by biasing the back gate (V_{G2}) in accumulation while the front gate (V_{G1}) is in inversion. Holes from the p+ source are injected by the forward-biased source/channel junction and stored in the electrically induced potential well. Programming conditions and related transients are reported and the role of temperature is investigated.

INDEX TERMS Tunnel FET, DRAM, Capacitorless memory, 1T/0C

I. INTRODUCTION

As device geometries shrink, the scaling of the conventional 1Transistor/1Capacitor (1T/1C) Dynamic RAM (DRAM) has become increasingly difficult, in particular due to the capacitor which has become harder to scale. The memory industry has achieved a lot of success in packing more and more bits per unit area in a silicon die. We are fast approaching the scaling limits for the physical capacitor element in a 1T/1C DRAM, and new materials and new device and integration approaches are required to meet the market demands. The concept of capacitorless single-transistor (1T) DRAMs was first reported in the early 90's [1], [2], however they have attracted attention [3]–[6] in more recent times. This is due to the ability of (1T) DRAM to achieve higher memory cell density and to solve the problems associated with the scaling of a physical capacitor. These memory cells can be classified in different groups with according to the excess majority carrier generation method i.e., depending on how the 1-state is programmed. This extra charge can be achieved mainly by four ways: impact ionization [7], bipolar junction transistor (BJT) effect [8], band-to-band (B2B) tunneling generation [9] and gate tunneling current [5]. The (1T) DRAMs take advantage of the parasitic floating body effects in SOI transistors to store the information i.e., to hold the charge. In a nMOSFET based 1T-DRAM, the 1-state current level is triggered by the excess hole charge generated into the body by one of aforementioned techniques. However the read out operation is based on a MOSFET operation (drift/diffusion of carriers over a potential barrier) in all cases.

Tunnel FETs as steep slope switches are very promising devices to respond to the demanding requirements of future technology nodes [10], [11]. The benefits of Tunnel FETs are specially linked to their potential for its sub-60mV/decade subthreshold swing, a prerequisite for scaling the supply voltage well below 1V. While high-performance Tunnel FETs exploit InAs-Si hetero-structures on nanowires [12], the all-Si Tunnel FET family appears primarily to have a very high I_{ON}/I_{OFF} and the lowest I_{OFF} [13], but they fail to achieve the requirements of high I_{ON} for a particular technology node [14]. An interesting property of a Tunnel FET is the fact that its sub-threshold slope is weakly dependent on temperature [15]. Tunnel FETs can thus be considered as very good candidates for operating at higher temperature, without compromising reliability. In Section IV-B, we will see how the read-out operation of the memory cell is not degraded by temperature.
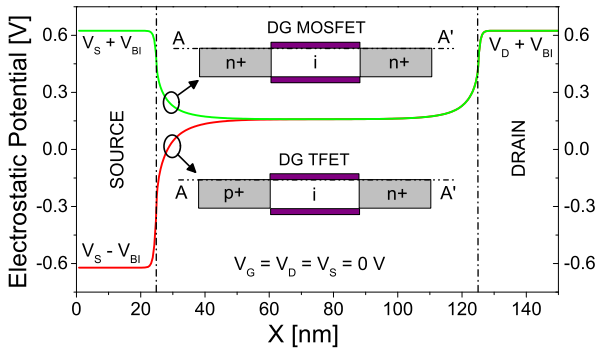
FIGURE 1. Simulated potential profile at 1 nm below the gate-oxide/channel interface for both DG-MOSFET and DG-TFET.

II. BACKGROUND

In this paper, we further build upon [16] that showed that all-Si double-gate (DG) Tunnel FET can serve for building a new class of devices: the capacitor-less Tunnel FET DRAM, where the very low I_{OFF} is offering low refresh rate and the zero-capacitor structure very high potential for scalability. We report a detailed simulation study and some experimental results on capacitorless Tunnel FET DRAM cell implemented as a double-gate fully-depleted Silicon-On-Insulator (FD-SOI) device. The device has an asymmetric design, with a partial overlap of the top gate (L_{G1}) and with a total overlap of the back gate over the channel region ($L_{G2}= L_{G1}+L_{IN}$), which creates the necessary condition to store holes injected from the source-to-body junction in an electrically induced potential well near the drain. The potential well is created by biasing the back gate (V_{G2}) in accumulation while the front gate (V_{G1}) is in depletion and/or inversion.

In Fig. 1 we see a comparison between the potential profiles at the surface of the channel for a DG-MOSFET and DG-Tunnel FET. The green line shows that, for the DG-MOSFET a potential well already exists which can hold the charges. The challenge in this case as discussed earlier is to generate the excess carriers. Whereas in case of a DG-Tunnel FET as shown by the red curve, there is no potential well by default due to the two different doping in the source and drain region. However, we do have a reservoir of both types of carriers in source/drain region which can easily brought to the body area by forward biasing the source/channel junctions. The challenge in case of a Tunnel FET is thus to create and maintain a potential well which could hold these extra charges. In the following section we will discuss about how we can design a structure which would facilitate the formation of a potential well and still work as conventional Tunnel FET.

III. FIN-TUNNEL FET AS 1T/0C DRAM

For this study the Tunnel FET architecture used is shown in Fig. 2(b). It is basically an independent gate Fin-Tunnel FET implementation of the FD-SOI devices shown in
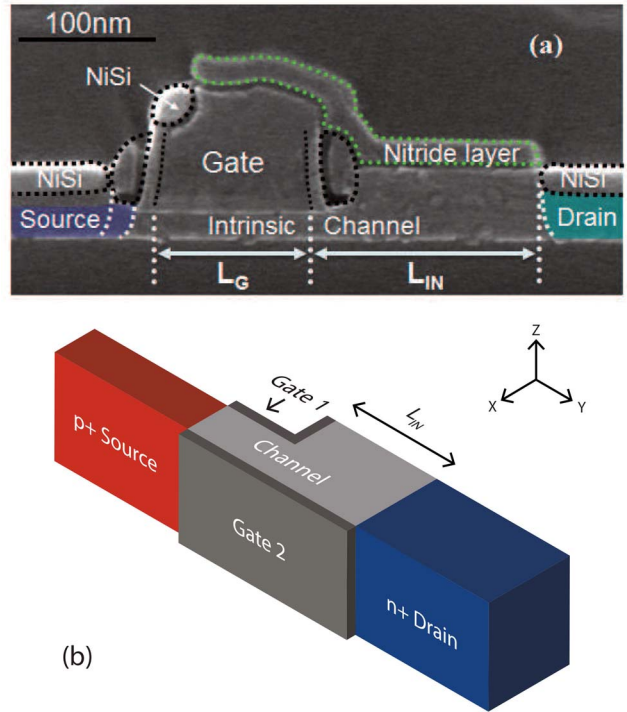

FIGURE 2. (a) SEM image of a fabricated FD-SOI Tunnel FET showing the top gate partially covering the channel. (b) Independent gate FinFET device structure for TFET based capacitorless DRAM.

Fig. 2(a) [13]. It is known that for efficient Tunnel FET operation a fully depleted body is required. However for charge storage in the body partial depletion is preferable. In order to meet both conditions a step like fin is used, which manages the trade-off between the electrostatic control of the Gate1 and the ability to store charges by Gate2. Simulations showed that 50-60nm fin widths for the partially depleted part were optimum. Gate1 partially covers the channel region and will be used as the main control gate for Tunnel FET operation. Gate2 on the other hand covers the entire channel region and as explained below will be used to induce a potential well in the channel region. This potential well will then be used to store charges for memory operation.

A. PRINCIPLE OF OPERATION

To understand the principle of operation let us take a 2D cut of the device shown in Fig. 2 along XY plane. Simulations were done in Synopsys Sentaurus TCAD [17]. The devices simulated were with fin width of 25nm in the source side and 50nm in the drain side, fin height = 65nm; Gate1 length (L_{G1}) = 80nm; Gate2 length (L_{G2}) = 200nm and a pocket length L_{IN} = 120nm, unless otherwise specified. A source/drain doping of $1 \times 10^{20} cm^{-3}$ of Boron/Arsenic was used. The channel was intrinsically doped. 3nm of SiO_2 gate oxide was used for both Gate1 and Gate2. The same metal work-function was used for both the gates. Fig. 3(a) shows the 2D hole-density plot with $V_{G1} = 2V$, $V_{G2} = -1V$, $V_D = 0V$, $V_S = 0V$. The memory operation is based on the
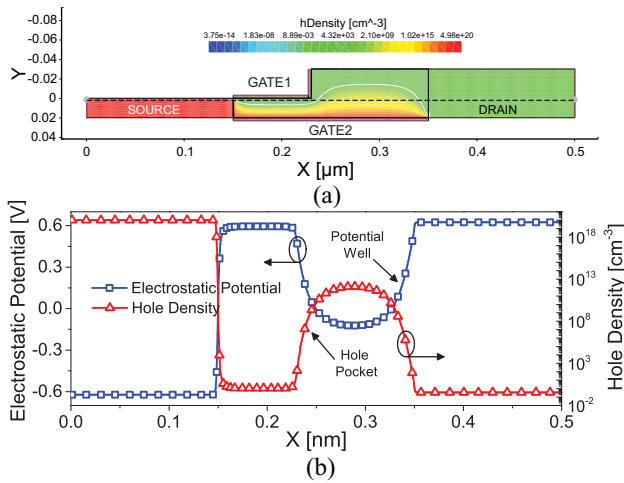
FIGURE 3. 2-D cross-section of the Fin-TFET showing the hole density at the end of a write "1" operation (top). Hole density and electrostatic potential at a cross section 1nm above the Gate2 showing the formation of potential well/hole pocket (bottom).

FIGURE 4. (a) Simulated transfer curves at various Gate2 bias. (b) Simulated hysteresis curves observed with varying L_{IN} with same biasing conditions. Devices with longer L_{IN} shows stronger hysteresis. $V_{G1} = 2$ V, $V_D = 1$ V.

creation of an induced potential well achieved by biasing Gate2 with a negative potential. A small positive bias on the source can help to flood the body with excess holes. These excess holes are then trapped in the potential well close to Gate2 as shown in Fig. 3 (top). Fig. 3(b) shows the cross-section at 1nm above the Gate2. We can clearly see the build-up of holes in the hole-density plot. The figure also shows an induced potential well where the holes can be stored. Hence, as the device turns on, the presence or absence of the excess carriers will affect the threshold voltage of the device indicating two different memory states.

The simulated transfer curves of the device in Fig. 1 is shown in Fig. 4(a). This is similar to what has been measured in [16] for FD-SOI devices. The principle of charge storage can be further verified by the hysteresis curves showed in Fig. 4(b). With $V_{G1} = 2$V and $V_D = 1$V, as the back gate bias is swept back and forth the charge storage in the partially depleted region results in two different current paths. When the V_{G2} goes from -1V to 2V in the first sweep, holes start to accumulate in the induced potential well in the body affecting the body potential, resulting in the lower branch on current in the plot. As V_{G2} increases to $+2$V, the accumulated holes are evacuated to the drain at this state. Now, as V_{G2} goes back to -1.5V in the following sweep, the drain current follows the top branch due to the lack of the excess charges in the body. Based on this observation, we can set the design a programming scheme of a memory cell with read potential at Gate2 at 1.5V. A fast sweep rate of 1mV/μsec was used in this transient simulation for convergence issues.

It is also interesting to note that the hysteresis is stronger for devices with longer L_{IN}. This is expected as length of the partially depleted region greatly influences the charge storage as also explained in [16]. So in this particular structure, the memory cell will loose its retention characteristics with gate
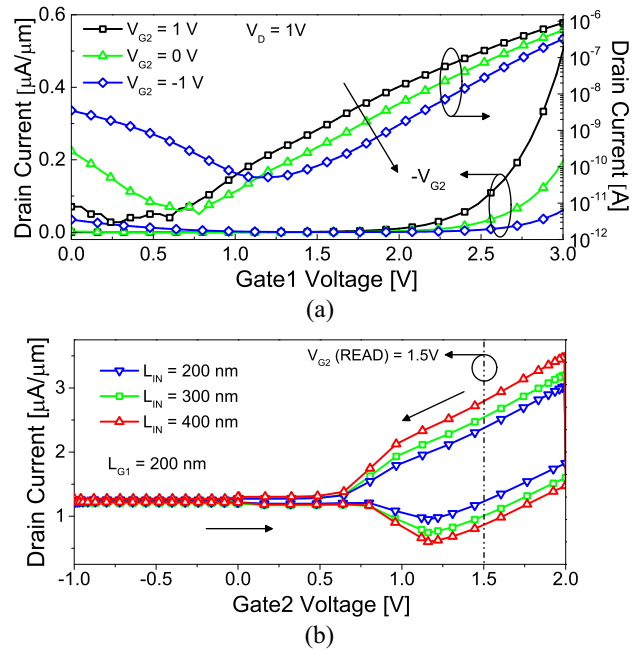
length scaling. There will be a minimum L_{IN} required for the memory cell to work satisfactorily.

The dependence of charge storage on L_{IN} is also observed in measurements from the devices described in [16]. The relaxation time is observed to be more prominent for devices with longer L_{IN}. Fig. 5(a) shows that depending on the length of the intrinsic region (L_{IN}) the discharge time varies. The device with longer $L_{IN} = 500$nm has a slower discharge than the device with $L_{IN} = 200$nm. This means that longer the L_{IN}, the more charge it stores and hence it takes longer to discharge. This experiment also demonstrates the importance of charge storage in the un-gated region. The discharge time can be related to the retention time of a conventional capacitorless DRAM, as it indicates how long the device can hold the charge once the write cycle is complete. In this context we observe a discharge time in the order of few milliseconds for devices with longer L_{IN}. The same principle can also be observed with steady state measurements in Fig. 5(b) and (c). The device with a longer L_{IN} clearly shows a stronger history effect. This observation validates the simulation results shown in Fig. 4.

B. PROPOSED PROGRAMMING SCHEME
The proposed programming scheme for the device in Fig. 3(a) is shown in Table 1.

(i) WRITE '1': The write "1" step involves biasing the source with a small positive voltage, together with a negative bias on Gate2. This would push holes into the body which will then be trapped in the induced potential well caused by Gate2 as shown in Fig. 3(b). Bias values used in simulation, $V_{G1} = 0$V, $V_{G2} = -1$V, $V_S = 0.25$V, $V_D = 0$V.

TABLE 1. Proposed Programming Scheme of Fin-TFET Based Capacitorless DRAM.

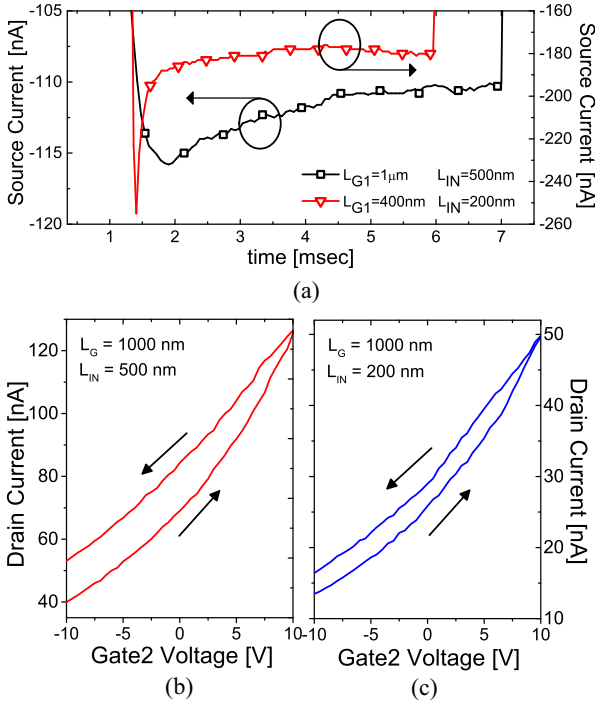| State	$V_D[V]$	$V_{G1}[V]$	$V_{G2}[V]$	$V_S[V]$
WRITE 1	0	0	negative bias to induce potential well/accumulation of holes	Small positive bias to push holes into the body
WRITE 0	0	0	Zero or small positive bias	Small negative bias to aid the erase process
HOLD	0	0	small positive bias to maintain the potential well	0
READ	VDD	$> V_{TH}$	Value at which maximum hysteresis observed (1.5V)	0

FIGURE 5. (a) Different relaxation times in the millisecond range are recorded when the back gate is biased at $V_{G2} = -10$ V (after writing 1), depending on the length of the L_{IN} region. The TFET with $L_{IN} = 500$ nm shows the longer discharge time while it is negligible in devices with $L_{IN} = 200$ nm. (b) & (c) Measured drain current with respect to back gate voltage at fixed front gate and drain voltages, $V_{G1} = 4.5$ V, $V_D = 4$ V.
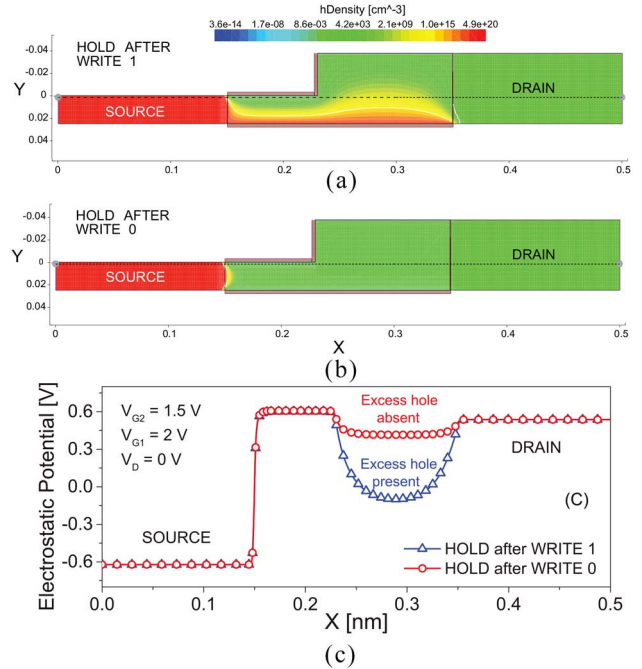

FIGURE 6. Simulated 2-D hole densities after a (a) WRITE 1 and (b) WRITE 0 operation. (c) Simulated potential profile at 1 nm below Gate1 showing the hole pocket.

(ii) WRITE '0'/ERASE: The write "0" step would simply mean putting a positive bias to the Gate2 (~2V). This will remove any induced potential well from the previous state and the holes in the body diffuse back to the source or recombine to drain. Bias values used in simulation, $V_{G1} = 0$V, $V_{G2} = 2$V, $V_S = -0.25$V, $V_D = 0$V.

(iii) HOLD: After the write '1' or '0' step the source goes back to zero and a small positive bias on Gate2 holds on to excess charges (if any) in the body. Bias values used in simulation, $V_{G1} = 0$V, $V_{G2} = 1.0$V, $V_S = 0$V, $V_D = 0$V.

(iv) READ: The readout operation is carried out via Tunnel FET operation with BTBT from p+ source to the intrinsic channel. For this, the drain is biased at V_{DD} and $V_{G1} >$ threshold voltage (V_{TH}) of the device. Source remains at zero bias for the read operation. Gate1 controls the read out current. The threshold voltage of the device is affected by the presence or absence of excess carriers in the body. Bias values used in simulation, $V_{G1} = 2$V, $V_{G2} = 1.5$V, $V_S = 0$V, $V_D = 1$V.

Transient simulations were done to observe the hole density in the body in HOLD mode preceded by WRITE "1"

and WRITE "0" operations. The results are given in Fig. 6. A clear difference is present showing that more holes are stored under the front gate after WRITE '1' compared to after WRITE '0' state. The same principle is also observed in the potential profiles at 1nm below the Gate1. After a WRITE 1 operation, there is a hole pocket present in the channel region. Similarly after a WRITE 0 operation, the hole pocket is much smaller. This hole pocket will primarily act as a resistance to current flow. Now as the device is turned on, the presence or absence of this excess carriers will affect drive current of the device indicating two different memory states.

IV. EXPERIMENTAL RESULTS
A. TRANSIENT MEASUREMENTS
Transient measurements were carried out FD-SOI Tunnel FET devices [13] with 20 nm Silicon layer thickness and 145 nm of BOX, according to the programming scheme is depicted in Table 2. This scheme is different from what was reported in [16] in order to better understand the principle of operation. The timing diagrams of READ and WRITE operations are shown in Fig. 7. The Gate1, Gate2 and drain were pulsed according to Fig. 7(a) below. The Agilent 4156C

TABLE 2. Programming Conditions for Indicated Operations of Capacitorless 1T TFET DRAM with L_{G1} = 400 nm, L_{IN} = 200 nm.

State	V_D [V]	V_{G1} [V]	V_{G2} [V]	V_S [V]
WRITE 1	0.5	0	-10	0
WRITE 0	0	0	+10	0
READ	4	4	-10	0

semiconductor parameter analyzer was used in sampling mode for the transient measurements. The source current was recorded at every 60μs (limited by the measurement setup).

During the WRITE cycle the Gate1/drain cycle is 50% phase shifted to the Gate2 pulse. This was to ensure that induced potential well stays as the device is turning ON after a WRITE 1. As highlighted in Fig. 7(b), after a WRITE 1 operation the Gate2 switches from −10V to +10V, with the device still ON the potential well ceases to exist and the stored charges can now escape. In other words the capacitor discharges as the Gate2 switches back to +10V. This capacitor discharge can be observed in the slow transient in Fig. 7(b). This experiment demonstrates the importance of the charge storage in the hole pocket outside the front gate overlap, controlled by V_{G2}. As shown in Fig. 7(d) a memory effect is thus observed.

During the ERASE cycle the Gate1/drain pulse is in opposite phase to the Gate2 pulse. Finally the READ cycle has the same biasing conditions (most negative Gate2 bias) for both WRITE and ERASE. The device turns ON at the most negative Gate2 bias i.e., −10V. Depending on the previous state, a clear difference in READ (source) current levels (ΔI_S) of 10nA is observed (Fig. 7(d)).

In the experimental setup, the biasing conditions are slightly different than what has been suggested in Section III-B. Most importantly a HOLD state could not be experimentally demonstrated, because of the very low ON current drive (~10nA) of the devices measured. The reported high values of V_{G2} in this section as compared to Section III-B is due to the fact that the measured device was a planar device on a SOI substrate with a 145nm BOX. Hence, a high V_{G2} was required to have the same effect as −2V (V_{G2}) in the simulated FinFET structure. Also it was not possible to measure the source current and at the same time pulse the source potential (V_S kept at a constant potential) due to the equipment limitations in the measurement setup. In erase operation, the influence of positive source is partially compensated by using highly positive gate bias at Gate2 (V_{G2}). In read operation drain and Gate1 potentials are chosen such that a desired ON current drive is achieved. Another difference in the biasing scheme can be observed in V_D for write operation. This has been done to stop the holes to recombine at the drain side. Also the Gate2 bias for read is different based on the observed hystory effect. At last Gate1 (V_{G1}) is biased positively in all the operation modes again due to the setup limitations. The reason of the low frequency choice is based on the ON current levels of the fabricated devices and the high parasitic capacitance contributed by non optimized test pads and the test instruments.
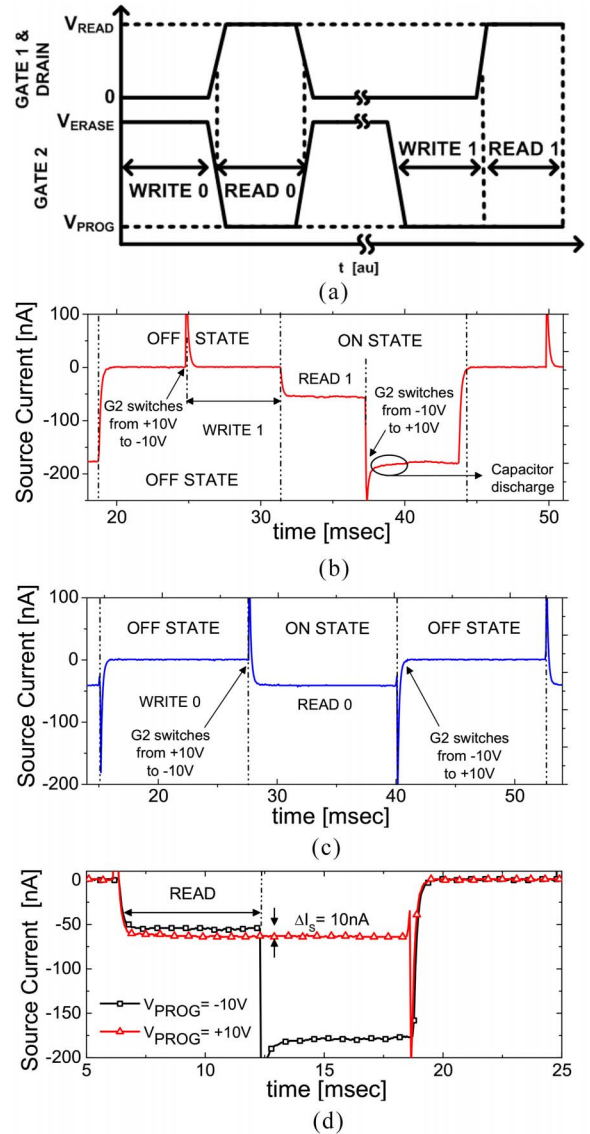
FIGURE 7. Timing diagram for different operations described in Table 2. Consecutive READ and WRITE operations for both states. The difference in READ current for states '1' and '0' is 10 nA, as highlighted, a memory effect is observed. Programming voltages are: V_{G2} = ±10 V for TFET with L_{G1} = 400 nm, L_{IN} = 200 nm.

B. TEMPERATURE DEPENDENCE

The transfer characteristics of the reported Tunnel FET devices have been measured from 25°C to 85°C and they show almost unchanged sub-threshold swing over the entire range as highlighted in the inset of Fig. 8(a) and low I_{OFF}. This is expected as band-to-band tunneling current is only weakly dependent on temperature [15]. Most importantly in Fig. 8(b), the discharge cycle (as highlighted in Fig. 7(b)) of the source current after a READ "1" operation, remains unaffected (at T = 25°C, 55°C, 85°C). This reflects the retention ability of the memory cell at high temperatures, in contrast with results reported on MOSFET-based solutions [8], [18], wherein the retention ability of the devices degrade with increasing temperature.
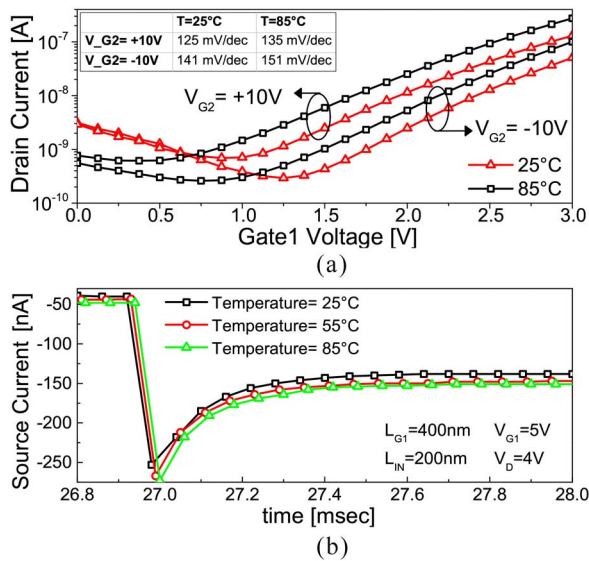
FIGURE 8. (a) Measured transfer characteristics with different Gate2 voltage at 25 °C and 85 °C temperature. As expected for a TFET the sub-threshold swing has a negligible temperature dependence. (b) Measured relaxation times as a function of temperature after a READ "1" operation. A minor dependence of the relaxation behavior on the temperature is experimentally demonstrated.

V. CONCLUSION

In summary we have presented simulation results on a new asymmetric Tunnel FET structure that can be used as a capacitorless DRAM. We have also experimentally demonstrated a scalable implementations of such 1T capacitorless DRAM cell based on DG Tunnel FET with a ΔI_S of 10nA. Retention times in the order of 100's of microseconds to few milliseconds, at room temperature in devices with channel length varying from 400nm to 1μm were observed. The discharge cycle was shown to be unaffected when the temperature varies between 25°C to 85°C.

ACKNOWLEDGEMENT

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