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A Silicon Biristor With Reduced Operating Voltage: Proposal and Analysis

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ABSTRACT In this paper, using 2-D simulations, we report a silicon biristor with reduced operating voltage using the surface accumulation layer transistor (SALTran) concept. The electrical characteristics of the proposed SALTran biristor are simulated and compared with that of a conventional silicon biristor with identical dimensions. The proposed device is optimized with respect to the device parameters to ensure a reasonable latch window while maintaining low latch voltages. Our results demonstrate that the SALTran biristor exhibits a latch-up voltage of 2.14 V and a latch-down voltage of 1.68 V leading to a 57% lower operating voltage compared to the conventional silicon biristor.

INDEX TERMS Biristor, bistable resistor, open-base breakdown, current gain, surface accumulation layer transistor (SALTran) effect, device optimization.

I. INTRODUCTION

The biristor is a bipolar junction transistor (BJT) with a floating-base electrode [1]–[6]. It is a two terminal device that has two stable resistance states, due to which it can be used as a memory device [1], [2]. Owing to its small size and low read/write time, the biristor can be used in high density and high speed memory applications. It can also be used as a current pulse generator due to its high rising rate of current and as a light trigger switch due to its optical response [1]. The biristor was studied as a biosensor [5] and can be a promising candidate in terms of CMOS compatibility, low-cost, and compact density. It is also free of cyclic endurance/reliability problems induced by hot-carrier injection due to the gateless structure, unlike 1T-DRAM [3].

In a biristor, switching from a high resistance state to a low resistance state occurs through the open base breakdown and switching from a low resistance state to a high resistance state occurs through the suppression of open base breakdown. This open base breakdown in a biristor arises through the impact ionization in the collector-base depletion region when the collector voltage is sufficiently large to trigger a breakdown. Since a large voltage is required to realize impact ionization in silicon devices, the reported latch-up voltages of a silicon biristor are considerably high, approximately 5.0 V [1], [2], [4], [6], making them less suitable for low voltage applications. It is, therefore, necessary to reduce the latch-up and latch down voltages for using the biristor as a memory device for practical purposes. Variations in doping profile of the base region have been proposed to control the latch characteristics. Similarly, using SiGe in the collector and the emitter regions of a biristor and a base made up of germanium in a biristor helped in reducing the latch voltages due to the smaller energy band-gap [6] of germanium or SiGe materials. A silicon biristor with an operating voltage less than 5 V has not been reported so far in the literature. With the advantages silicon has, such as wider band-gap, abundance and cheaper production compared to germanium, it is essential to realize a silicon biristor with a reduced operating voltage.

One of the ways to attain reduced operating voltages in silicon biristor is to increase its current gain (β), due to which open base breakdown occurs at a lower collector voltage. A well-known method of increasing the current gain is to use a SiGe base [7]. However, this requires using a hetero-junction and a complicated process for introducing germanium in the base region.

Recently, a new method of increasing the current gain has been reported using surface accumulation of carriers at the emitter contact known as the surface accumulation layer transistor (SALTran) concept [8] and has been extensively studied [9]–[13]. The SALTran concept involves electrostatically

inducing carriers in a lightly doped semiconductor using metal electrode contacts of appropriate work functions. The SALTran concept has also been used to demonstrate high current gain dopingless bipolar transistors [14]–[20]. Experimental validation of such electrostatically doped pn-junction has already been reported [21]. Electrostatic doping, such as the one used in a SALTran, has now become an important technique to demonstrate even steep subthreshold MOSFETs [22]–[25]. Therefore, in this paper, using the SALTran concept to increase the current gain (β) of a bipolar transistor, we demonstrate for the first time, a silicon biristor with a significantly reduced operating voltage. To distinguish the proposed biristor from the conventional biristor, we have named it as the SALTran biristor. Using 2D simulations [26], we report the latch-up voltage and latch- down voltage of the optimized SALTran biristor to be 2.14 V and 1.68 V, respectively. These are approximately 57% lower than the reported values for the conventional silicon biristor.

II. SURFACE ACCUMULATION LAYER TRANSISTOR (SALTRAN) CONCEPT

The SALTran effect can be understood from Fig. 1. The schematic band diagram at the metal-emitter contact of the SALTran is shown in Fig. 1(a) when the metal work function is lower than that of the n-type emitter [8]. The transfer of electrons from the metal into the semiconductor results in a surface accumulation of electrons in the semiconductor near the metal-semiconductor interface. The electrostatically accumulated surface electron concentration $n_S(x)$ reduces to the background electron concentration in the lightly doped emitter within about one Debye length [14].

Due to the non-uniform distribution of the electrostatically induced electrons $n_S(x)$, a built-in electric field E(x) is formed near the metal-emitter contact interface as shown in Fig. 1(b). The direction of this induced electric field due to the non-uniform distribution of the accumulated electrons is such that it opposes the flow of holes $p_E(x)$ entering the emitter from the base. As shown in Fig. 1(c), this decreases the gradient of the excess holes $p_E(x)$ in SALTran (solid line) compared to the excess hole gradient $p_E(x)$ in the conventional bipolar transistor (dashed line). However, the gradient of the excess electrons $n_E(x)$ injected from the emitter into the base region is not affected. This will lead to a reduction in the base current for a given collector current resulting in a significant enhancement in the current gain [8].

Therefore, by employing a lightly doped emitter in a bipolar transistor and an emitter metal contact with a work function lower than that of silicon, we can get a significantly higher current gain compared to a conventional bipolar transistor. If such a surface accumulation layer transistor (SALTran) with enhanced current gain is used in the open base configuration, we demonstrate that it would result in a reduction in the latch-up and the latch-down voltages of the silicon biristor.

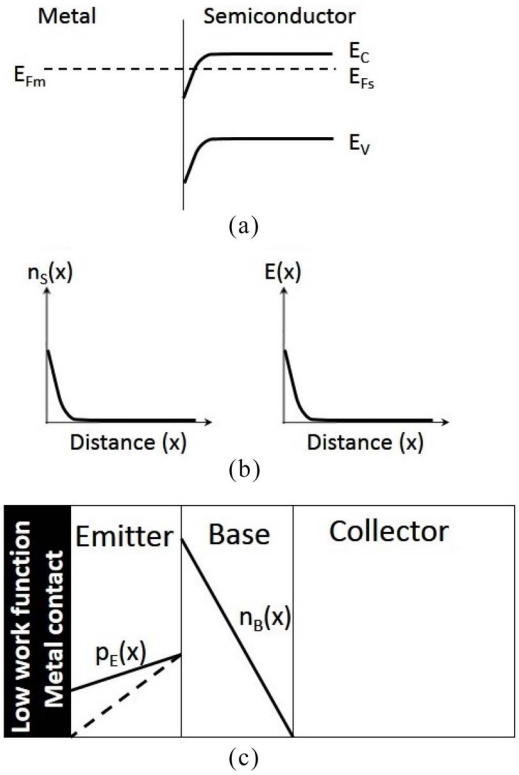

FIGURE 1. (a) Schematic band diagram at the metal-semiconductor junction. (b) Electrostatically accumulated surface electron concentration $n_S(x)$ and the built-in electric field E(x) near the metal-emitter contact interface. (c) Profile of excess holes $p_E(x)$ injected from the base into the emitter region for SALTran (solid line) and for a conventional BJT (dashed line).

III. DEVICE STRUCTURE AND SIMULATION PARAMETERS

The cross sectional view of the biristor is shown in Fig. 2. To preserve the excess holes generated by impact ionization, the biristor needs to be implemented using SOI technology [1]. The emitter, base and collector lengths are denoted by W_E, W_B and W_C respectively. The width of the device in z-direction is 1 μm. To calibrate our simulated latch voltages with the reported experimental results, we adapted the device structure and parameters of the biristor from [2] which are as follows: N^+ emitter/collector doping $N_D = 1 \times 10^{20}$ /cm^3, P base doping $N_A = 1 \times 10^{18}$ /cm^3, silicon film thickness $(T_{Si}) = 50$ nm, emitter/collector length $(W_E/ W_C) = 200$ nm and base length $(W_B) = 250$ nm. The simulation parameters for the SALTran biristor are same as above except for the emitter doping which is taken to be 4×10^{14} /cm^3 and the emitter electrode work function is taken to be 3.9 eV [8].

The models used in Atlas device simulation tool [26] include the concentration dependent Shockley–Read–Hall model, trap-assisted tunneling model, Masetti low field mobility model, parallel electric-field-dependent mobility model, band gap narrowing, energy balance model, and Toyabe impact ionization model. To simulate the breakdown phenomenon, the CURVETRACE algorithm was used. This algorithm can automatically switch smoothly between

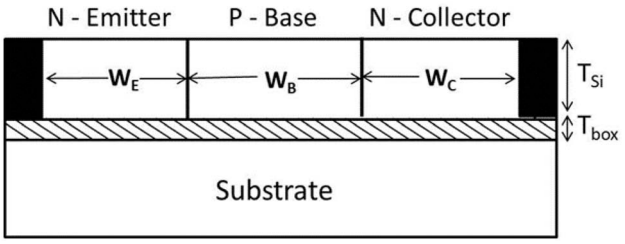

FIGURE 2. **Schematic cross-section of the biristor structure.**

voltage and current boundary conditions, which is essential in simulations involving snapback and breakdown [26].

The latch-up (V_{LU}) and latch-down (V_{LD}) voltages are estimated using the Toyabe (non-local) impact ionization model. In the Toyabe model, the impact ionization rates α_n and α_p for electrons and holes, respectively, are given by:

$$\alpha_n = ANexp\left(-\frac{BN}{E_{eff,\ n}}\right) \quad (1)$$

$$\alpha_p = APexp\left(-\frac{BP}{E_{eff,\ p}}\right) \quad (2)$$

where AN = 3.8 × 10^6 /cm, AP = 2.25 × 10^7 /cm, [27] and BN = 1.23 × 10^6 V/cm, BP = 1.69 × 10^6 V/cm are the default values from Atlas simulator [26]. For the conventional biristor with the device parameters given above, the values of V_{LU} and V_{LD} obtained by our simulations are 4.93 V and 3.32 V, respectively. These values match well with the experimental values of V_{LU} = 4.95 V and V_{LD} = 3.35 V reported in [2]. This confirms the accuracy of the impact ionization parameters used in our simulations. Using these calibrated model parameters, the latch voltages of the SALTran biristor can now be estimated accurately.

IV. RESULTS AND DISCUSSION

A comparison of the simulated β values of the SALTran and the conventional biristors, shown in Fig. 3, indicates that with the introduction of SALTran effect, there is an improvement in the value of the current gain β by at least 1000 times in the operating range of the collector current of the biristor. With such a high value of current gain, we can expect a higher impact ionization rate for the SALTran biristor compared to the conventional biristor for the same value of the collector voltage V_{CE}. To verify this, the impact ionization rates of the SALTran and the conventional biristor at V_{CE} = 2.36 V are shown in Fig. 4. These results indicate that the SALTran biristor has a maximum impact ionization rate and is approximately 1000 times higher than that of the conventional biristor in the base region. This higher impact ionization rate results in the presence of more number of excess holes in the SALTran biristor base region. Therefore, we can expect the latch voltages to be lower in a SALTran biristor compared to a conventional biristor.

To verify the effect of the enhanced impact ionization in the SALTran biristor, the I_C - V_{CE} characteristics of the SALTran biristor are compared with the conventional biristor

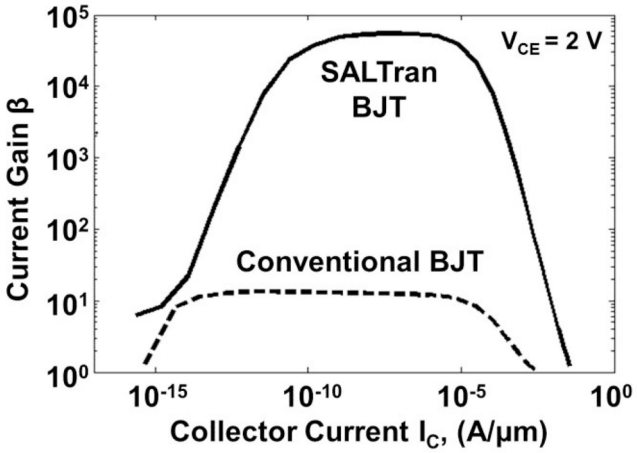

FIGURE 3. **Comparison of β vs I_C characteristics of the conventional BJT and the SALTran with dimensions same as those of their biristor counterparts.**

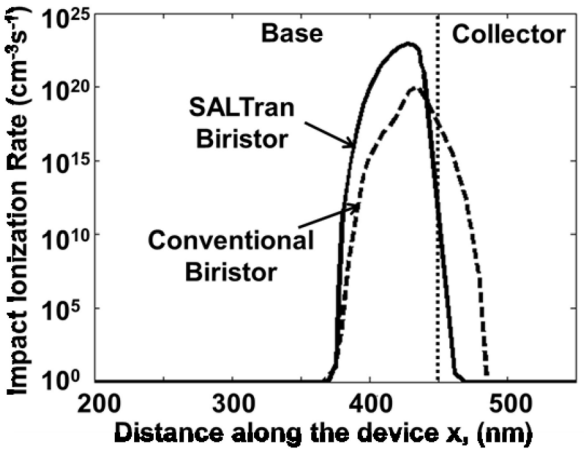

FIGURE 4. **Comparison of the impact ionization rates in the base region of the conventional and the SALTran biristors biased at V_{CE} = 2.36 V.**

in Fig. 5. The snapback in I_C - V_{CE} characteristics can be explained as follows. As we increase the collector voltage, the multiplication factor M approaches 1+1/β. This leads to breakdown resulting in a large collector current I_C. However, as I_C increases, the current gain β also increases, which means that M must decrease. Therefore, a drop in M corresponds to a drop in V_{CE}. As a result, as I_C increases, V_{CE} decreases and this results in a snapback.

For the conventional biristor, the latch-up and latch down voltages extracted from Fig. 5 are 4.93 V and 3.32 V, respectively. However, the latch up and latch-down voltages of the SALTran biristor in Fig. 5 are 2.36 V and 2.14 V, respectively. The SALTran biristor exhibits a reduction of about 52% in latch-up voltage and 35% in latch-down voltage as compared to the conventional biristor due to an increase in the current gain. However, the latch window (ΔV_L) of 0.22 V for the SALTran biristor is too small. Hence, the biristor parameters need to be optimized to achieve a reasonable latch window while maintaining lower latch voltages.

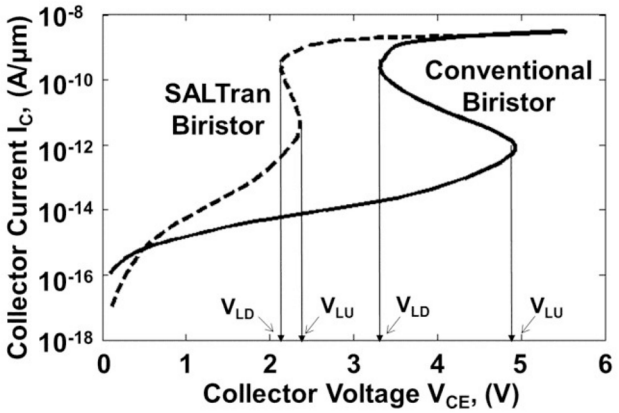

FIGURE 5. Simulated I_C-V_{CE} characteristics of the conventional and the SALTran biristors.

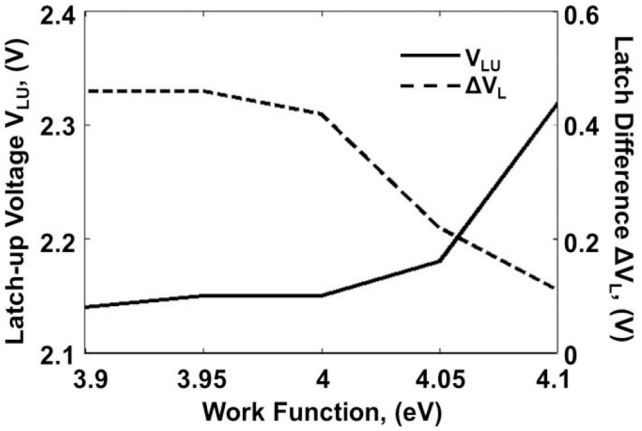

FIGURE 7. V_{LU} and ΔV_L versus emitter electrode work function of the SALTran biristor.

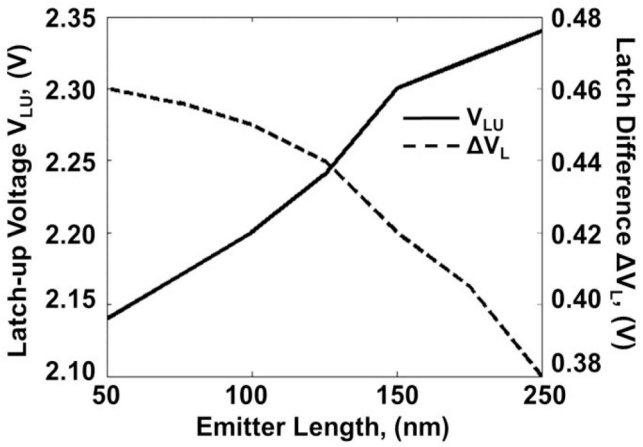

FIGURE 6. V_{LU} and ΔV_L versus emitter length of the SALTran biristor.

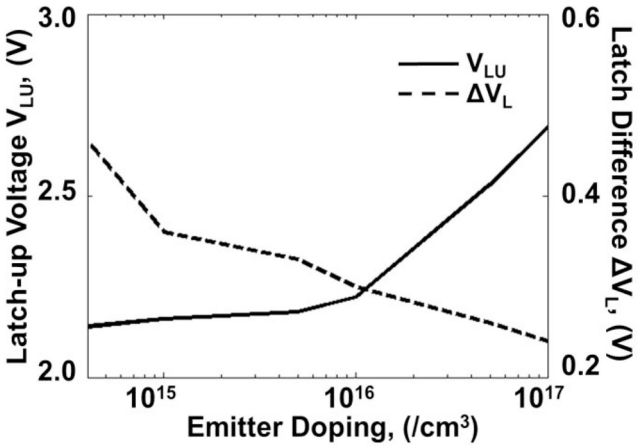

FIGURE 8. V_{LU} and ΔV_L versus emitter doping of the SALTran biristor.

Optimization of device parameters is performed as discussed below. Enhancement of current gain causes a decrement in V_{LU} and an increment in ΔV_L [6]. A reduction in base doping increases the current gain. However, when a base doping of less than 1×10^{17} /cm^3 is used, our simulation results indicate that breakdown occurs through punch-through mechanism [1] at a voltage (V_{CE}) less than 1.5 V. Therefore, an optimal base doping of 5×10^{17} /cm^3 is chosen.

A reduction in base length (W_B) also increases the current gain. However, at a base length of 100 nm and a base doping of 5×10^{17} /cm^3, the latch window ΔV_L is considerably low. This occurs as a result of enhancement in the multiplication factor M [6] with a reduction in base length. Hence, we used a base length of 150 nm in our optimized device.

The current gain of a SALTran device increases significantly with a reduction in emitter length. Hence, we can expect a reduction in V_{LU} as well as an increase in ΔV_L. A plot of V_{LU} and ΔV_L versus emitter length is shown in Fig. 6. From Fig. 6, we observe that, for an emitter length of 50 nm a low V_{LU} and high ΔV_L can be realized.

The other parameters that are capable of affecting the latch voltages include the work function of the metal electrode at the emitter contact and also the emitter doping. By decreasing the emitter electrode work function, a high current gain can be achieved [8] leading to a reduction in the latch voltages. This is corroborated by the simulation results shown in Fig. 7. Hence, we have used a work function of 3.9 eV for the emitter electrode. Also, a low emitter doping implies high current gain and hence low V_{LU} and high ΔV_L, as shown in Fig. 8. Hence, an emitter doping of 4×10^{14} /cm^3 [8] is used.

The parameters of the optimized SALTran biristor are therefore: N^- emitter doping $N_E = 4 \times 10^{14}$ /cm^3, P base doping $N_A = 5 \times 10^{17}$ /cm^3, emitter/collector length = 50 nm, base length = 150 nm and the emitter electrode work function = 3.9 eV.

Fig. 9 shows the I_C-V_{CE} characteristics of the optimized SALTran biristor compared with those of the un-optimized SALTran biristor of Fig. 5. For the optimized device, $V_{LU} = 2.14$ V, $V_{LD} = 1.68$ V and $\Delta V_L = 0.46$ V. This is a clear demonstration of reduction in the latch voltages as

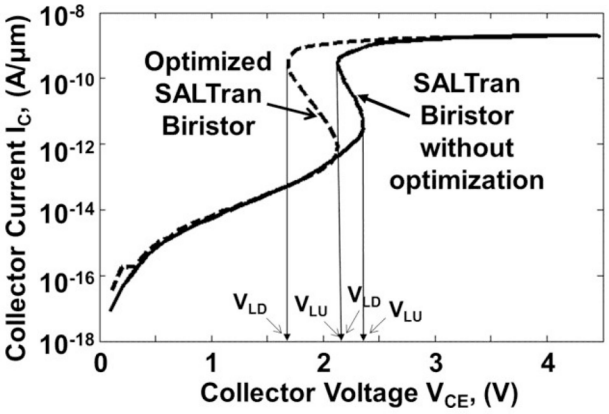

FIGURE 9. Comparison of I_C-V_{CE} characteristics of the optimized SALTran biristor with the SALTran biristor without optimization.

well as an improvement in the latch window in the optimized SALTran biristor.

The conventional biristors have identical emitter and collector dopings, which enables bi-directional operation and hence, results in sneak leakage paths among the neighboring cells in a crossbar array [3], [4]. However, in the proposed SALTran biristor, the emitter doping has to be necessarily lower than the collector doping to achieve a higher current gain and therefore, a higher impact ionization. Due to this asymmetrical nature of the SALTran biristor, the bidirectional operation is not possible and the sneak leakage currents could be avoided. Moreover, the size of the proposed optimized SALTran biristor is considerably less than previously reported biristors and hence, it acts as a high density memory device.

V. CONCLUSION

By increasing the current gain (β) of a silicon biristor using the SALTran effect, we have successfully demonstrated a silicon biristor with a low operating voltage for the first time. The proposed optimized silicon biristor exhibits a decrease of 2.14 V in the latch-up voltage and 1.68 V in the latch-down voltage. This amounts to a significant lowering of the operating voltage ($\sim$ 57%) compared to the silicon biristor reported in [2]. The optimized SALTran biristor has the added advantage of not allowing the sneak leakage current because of its asymmetrical emitter and collector doping. The proposed SALTran can be fabricated using a similar process as reported in [2] except that the emitter is lightly doped and the work function of the metal needs to be chosen to be less than that of the emitter region. Our results may provide the incentive for further experimental exploration of the proposed structure.

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