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Source-Pull and Load-Pull Characterization of Graphene FET

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ABSTRACT This paper presents the characterization of a GFET transistor using a source-pull/load-pull test set. The characterization shows that despite the good f_T and f_{MAX}, it is hard to achieve power gain using the GFET device within a circuit configuration. This is due to the very high impedance at the gate making impedance matching at the input extremely difficult. S-parameter characterization is performed and the associated small signal model is developed in order to further analyse and extrapolate the source-pull and load-pull measurement results. A good agreement is observed between small signal model simulation results and source-pull/load-pull measurements. Finally, the model is used to evaluate the optimum power gain of the transistor in a circuit configuration under matched conditions.

INDEX TERMS Graphene, FET, circuit design, impedance matching, source-pull, load-pull, small-signal model.

I. INTRODUCTION

Graphene research activities for circuit design have started recently and few analogue and RF circuits have been demonstrated [1]–[7] up to the GHz range. Despite the low maturity of the graphene material, first results show some interesting performances with a mixer working at 30 GHz having a conversion loss of 19 dB [2] and a ring oscillator [8], [9] working in the GHz range [9]. Most of the fabricated GFET devices are not able to amplify power in a 50Ω impedance environment and need input and output impedance matching elements. In [4], the impedance matching of GFET devices in mixer configuration has been evaluated by means of a compact model. In [5], the GFET transistor has been evaluated for LNA circuit design, high frequency noise performance, gain compression and the third order intermodulation product were characterised under 50Ω, that is to say without specific input-output impedance matching. Finally, reference [6] details a noise-pull characterisation of a GFET device, i.e. searching the optimum impedance matching to evaluate minimum noise figure. Unfortunately, impedance matching of first GFET generations is a weakness of this technology since the input port reflection coefficient S11 is very close to the open circuit. This is mainly due to a very small input capacitance combined with a moderate working frequency of the transistor. As analysed in [3] and [10]–[12] a large inductor is necessary for input circuit matching in the GHz range to avoid strong reflection. This large inductor is a very limiting factor for the realisation of completely integrated circuits. In this paper, we investigate the input and output impedance matching of the GFET. For the first time, up to our knowledge, we propose to match the GFET device using source-pull and load-pull tuners.

II. GFET CHARACTERISATION

The GFET devices under test have been fabricated by the IEMN laboratory [11] [see Fig. 1(a)]. The graphene was fabricated by thermal decomposition on the Si-face of a silicon carbide wafer. The transistor channel is composed of one to three graphene layers. The gate length is 150 nm. A top gate is used with an insulator thickness of 8 nm made of Al_2O_3. The width of the device is 2*24 μm. First, the device is characterised in DC and the output curves are presented in Fig. 2. Transconductance is plotted on Fig. 3 and shows an

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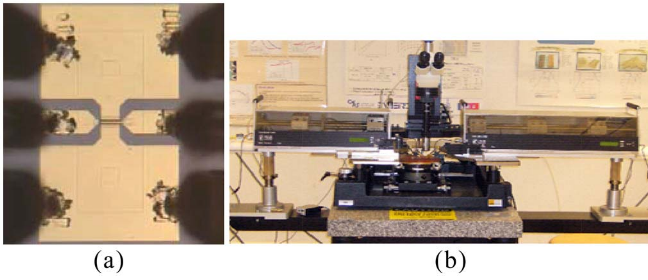

FIGURE 1. (a) GFET measured with GSG RF probes. (b) Load and source tuners associated with the probe station.

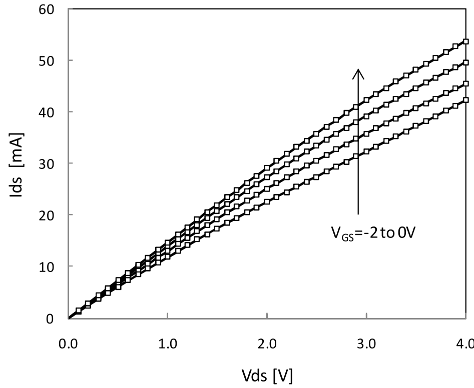

FIGURE 2. Output curves: I_{DS} versus V_{DS} and for different V_{GS}.

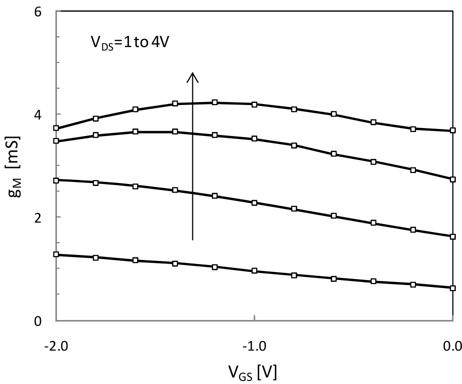

FIGURE 3. Transconductance versus V_{GS} for different V_{DS}.

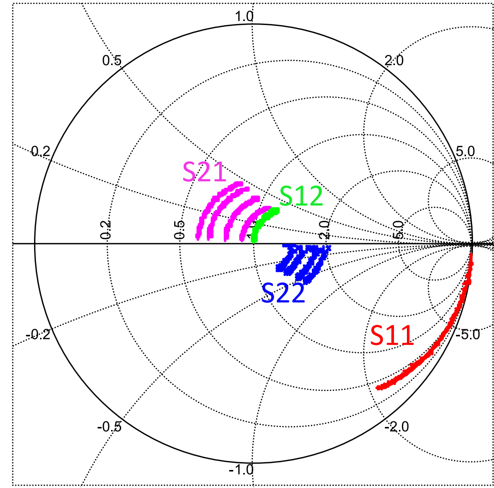

FIGURE 4. Smith chart (up to 20 GHz) at $V_{GS} = -1$V and for different V_{DS} (1, 2, 3, and 4 V). Measurement and simulation include pads. Measurement is in symbol and simulation is in solid line.

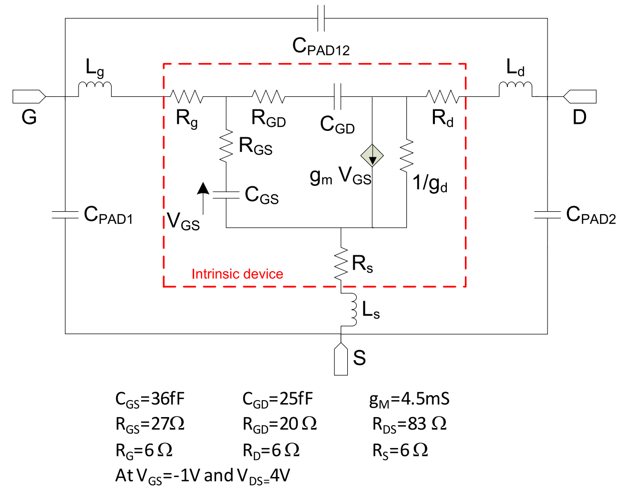

FIGURE 5. Small signal model used for S-parameter and source-pull/load-pull simulation. Each parameter value is bias condition dependent.

optimum bias point at V_{DS} = 4 V and $V_{GS} = -1$V. Second, S-parameter measurements are performed with a Rohde & Schwartz ZVA 67 GHz network analyser at different bias points (see Fig. 4). In order to build a consistent small signal model, a pad-open structure is used for de-embedding and a specific test structure is used to evaluate R_S and R_D. For each measured bias point, a small signal model is built (see Fig. 5) using the procedure described in [13]. Small signal model parameters are given for the optimum bias point, V_{DS} = 4 V and $V_{GS} = -1$V. S-parameter measurements and simulation results are presented on Fig. 4 and show a good agreement up to 20 GHz.

It can be noted that S21 is much lower than 0 dB meaning that the DUT does not amplify power in a 50 Ω environment. The device is characterised by an extrinsic cut-off frequency (including pads) of about 10 GHz and a maximum oscillation frequency of about 11 GHz (see Figs. 6 and 7). An input and output impedance matching is necessary to use the full operational capacity of this GFET device. A 0.8 GHz-18GHz load-pull/source-pull bench combined with an on-wafer probe station [Fig. 1(b)] is used to match the input and output port of the device. Hence, we can evaluate the device in a circuit configuration. The tuners are calibrated at two standards frequencies in RF electronics: 900 MHz and 2.4 GHz using a network analyser. The measurement set-up is presented on Fig. 8. A RF source, a splitter and two power-meters are used for transducer power gain measurement.

Using the S-parameter measurements and the small signal model, the optimum input matching at low power can

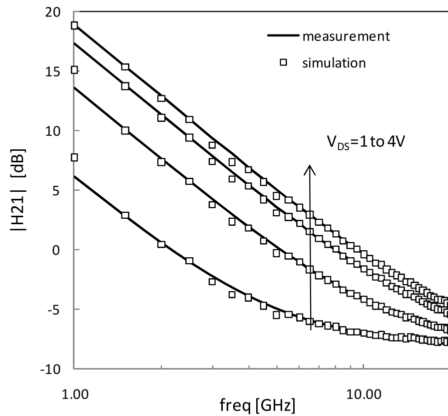

FIGURE 6. H21 versus frequency, measurement (symbols), and simulation (solid line) at $V_{GS} = -1V$ and for different V_{DS} (1, 2, 3, and 4 V). Measurement and simulation include pads.

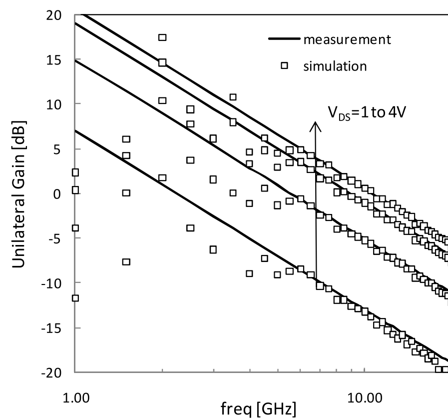

FIGURE 7. Unilateral gain versus frequency, measurement (symbols), and simulation (solid line) at $V_{GS} = -1V$ and for different V_{DS} (1, 2, 3, and 4 V). Measurement and simulation include pads.

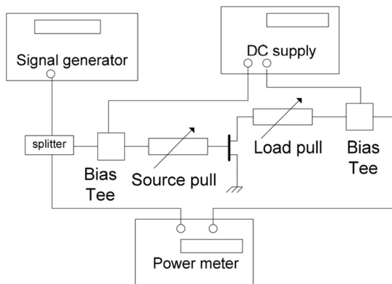

FIGURE 8. Measurement set-up for source-pull and load-pull measurement.

be evaluated using the conjugate of S11. Unfortunately, the optimum reflection coefficient Γ is higher than 0.99 at both frequencies: 900 MHz and 2.4 GHz. The corresponding impedance cannot be generated with our source-pull tuner which is limited to a reflection coefficient of about Γ = 0.95 due to the loss in the tuner and the test bench. Logically, we will not get the optimum performances of the device using the source-pull/load-pull bench.

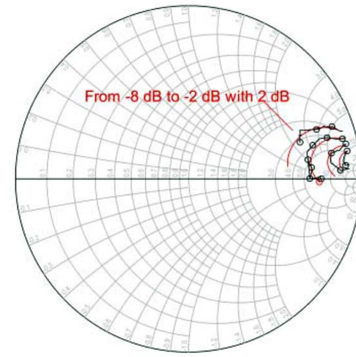

FIGURE 9. Constant transducer power gain circles (from −8 to −2 dB with 2 dB step), measurement black line with symbol, simulation in red solid line), input power = −25 dBm, f_0 = 2.4 GHz, and V_{GS} = −1 V, V_{DS} = 3 V.

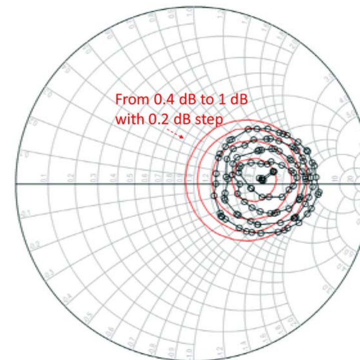

FIGURE 10. Constant transducer power gain circle from 0.4 to 1dB with 0.2 dB step, (measurement: black line with symbols, simulation: red solid lines), input power = −25 dBm, f_0 = 900 MHz, and V_{GS} = −1 V, V_{DS} = 4 V.

Hence, we tune the input tuner in the vicinity of Γ = 0.95 for best possible matched impedance in the test bench. At 2.4 GHz, the source tuning is performed with the optimum load impedance: 127 Ω + j 23 Ω. The power gain of the GFET is measured on a selected area of the Smith chart (see Fig. 9).

Unfortunately, the input matching is very selective with respect to frequency. The maximum gain (attenuation!) measured at 2.4 GHz and V_{DS} = 3V is about −2.dB.

At 900 MHz, the optimum source tuning results is Γ∼0.945. In order to search the optimum load, different load matching impedances are evaluated and presented on the Smith chart. The resulting measured constant power gain circles are plotted on the Smith chart. A gain of 0.9 dB is obtained pushing the bias condition to V_{DS} = 4 V for an optimum load of 142 Ω + j*42 Ω (see Fig. 10). Using the small signal model, we were able to validate the source-pull and load-pull constant-gain circle measurement (see Figs. 9 and 10). A good agreement is observed between measurement and simulation. The small discrepancies are due to a slight shift of electrical characteristics during measurements. The selectivity of the device in term of input matching is well modeled by our small signal model. The small constant gain circles are due to the small magnitude

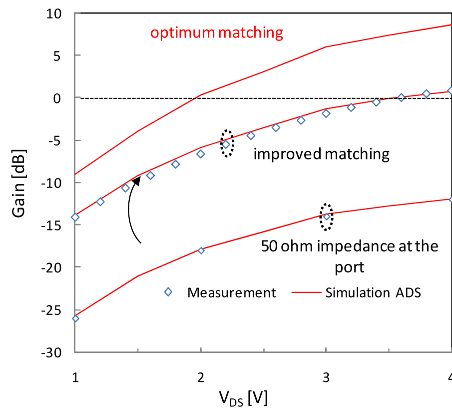

FIGURE 11. Transducer power gain, for different V_{DS} conditions under 50 Ω impedance at the ports, with improved impedance matching (in the limit of our input tuner), f_0 = 900 MHz, Pin = −25 dBm, and under theoretically optimised impedance matching conditions.

of the transistor S21 parameter. In fact not yet mature GFET technologies show in general low transconductance and in particularly high output conductance. Moreover, optimum load impedance is easily reached using the load-pull tuner.

Finally, Fig. 11 shows the impact on power gain of 3 different matching impedances as a function of bias. First, under 50Ω environment, the power gain varies from −25dB to −15dB when changing V_{DS} from 1 to 4V. Second, using the source-pull and load-pull tuners in order to optimize the matching within the tuner limitations, the gain changes from −15dB to 0.9 dB for the same V_{DS} range. Third, we have simulated the power gain under theoretically optimum matching conditions using the small signal model: this GFET is able to obtain a power gain of about 6 dB at 900 MHz and 5 dB at 2.4 GHz at V_{DS} = 3V (including pads).

III. DISCUSSION

In order to evaluate the graphene FET technology for RF circuit applications, different figures of merit can be analysed depending on the different circuit blocks, i.e. low noise amplifiers, power amplifiers, mixers. The most basic circuit function is the amplification: this characterisation work has shown that a reasonable power gain level can be obtained if impedance matching limitations can be circumvented by improving transistor performances such as g_M and g_{DS} and optimizing device size in order to increase C_{GS} capacitance. Increasing the graphene quality and the associated interfaces will directly increase mobility and as a consequence the I_{DS} current and the g_M parameter. Concerning power amplifier, the power added efficiency is one of most important figure of merit. This figure of merit directly involves the circuit amplifier gain and the associated DC power consumption. In order to improve this figure of merit, the amplifier gain needs improvement without increasing DC power, i.e. I_{DS} current. In this case, one needs to improve g_{DS}, i.e. the device saturation. The saturation of the transistor can be improved by working on different key points: i) the graphene mobility, ii) the contact resistance, iii) the electrostatic control of the channel. Finally, major improvements will come from improving the graphene quality and its associated interfaces, by choosing an optimum gate oxide such as the hexagonal boron nitride [14] and by preserving graphene quality using gold [15].

IV. CONCLUSION

A GFET transistor has been extensively characterised in order to evaluate its performances in RF circuit configuration. For the first time, a GFET device has been characterised using source-pull and load pull tuners to evaluate the power gain under matched conditions. The characterisation shows that despite a good extrinsic f_T and f_{MAX}, it is difficult to achieve power gain with the GFET device. This is due to the difficulties to match the input of this GFET device. Usually, mature FET devices are difficult to match in the low frequency range but have |S21| >1 under 50Ω environment. The input impedance matching of the GFET is very selective and a small dispersion on the input matching induces a large variation of the power gain of the complete circuit.

Nevertheless, a power gain of 0.9dB has been measured at 900 MHz. Also, a good agreement is observed between the small signal model and source-pull/load-pull and S-parameter measurements. Finally, the model is used to evaluate the optimum power gain of the transistor. Using an optimum impedance matching, this GFET is able to deliver a power gain of about 6 dB at 900 MHz and 5 dB at 2.4 GHz applying V_{DS} = 3V. The GFET's performances regarding circuit applications can be further improved by reinforcing the technology research on device saturation.

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