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4H-SiC N-Channel JFET for Operation in High-Temperature Environments

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ABSTRACT Lateral depletion-mode 4H-SiC n-channel junction field-effect transistors (JFETs) are demonstrated to operate with well-behaved electrical characteristics at temperatures up to 600 °C in air. Ti/Ni/TiW metal stacks are used to form ohmic contacts to n-type 4H-SiC with specific contact resistance of 1.14×10^{-3} Ω cm^{2}at 600 °C. The on/off drain saturation current ratio and intrinsic gain at 600 °C are 1.53×10^3 and 57.2, respectively. These results indicate that 4H-SiC JFETs can be used for extremely-high-temperature electronics applications.

INDEX TERMS High-temperature electronics, junction field effect transistor (JFET), silicon carbide (SiC).

I. INTRODUCTION

Sensors and electronic systems that can operate in the temperature range 300-600 °C are required for *in-situ* monitoring of fuel combustion and sub-surface reservoirs (deep well drilling), and for outer space exploration [1]–[3]. The use of semiconductor devices that can operate properly at such high temperatures would not only minimize the need for expensive and large cooling systems, but also provide for improved system reliability [4]. Silicon carbide (SiC) has become the preferred semiconductor material for harsh-environment sensing applications because of its wide bandgap energy (3.2 eV for 4H-SiC), excellent chemical and thermal stability, and high breakdown electric field strength (∼2.2 MV/cm) [5].

Operational amplifiers utilizing SiC metal-oxide-semiconductor (MOS) or junction (J) field-effect transistor (FET) devices as voltage-controlled current sources have been investigated in recent years [6], [7]. MOSFETs suffer from low field-effect mobility and poor gate-oxide reliability which limits their maximum operating temperature to 400 °C [6]. Transistors comprising only pn junctions such as the JFET and bipolar junction transistor (BJT) operate with better endurance at high temperature [4]. Although BJTs exhibit superior electrical properties, they consume more power and their performance degrades at temperatures above 350 °C; further studies of their long-term reliability are needed [8]. In contrast, 6H-SiC JFETs have been demonstrated for low-voltage analog signal amplification, with more than 10,000 hours of continuous operation at 500 °C in air [4]. There is growing interest in 4H-SiC, because of its larger bandgap energy and higher electron mobility (950 cm^2/Vs perpendicular to c-axis and 1150 cm^2/Vs parallel to c-axis) as compared with 6H-SiC, and its commercial availability in wafer sizes up to 6 inches in diameter. In this work, depletion-mode 4H-SiC n-channel JFETs designed for low-voltage operation are demonstrated to operate with well-behaved characteristics at temperatures ranging from room temperature up to 600 °C in air.

II. EXPERIMENT

Fig. 1(a) is a schematic cross-section of the lateral JFET structure investigated in this work, which is similar to the device described in [4] except that the semiconductor material is changed to 4H-SiC. The starting substrate is a p-type 4H-SiC wafer (from Cree Inc.) with resistivity of approximately 1 Ω-cm, on which three epitaxial layers were grown

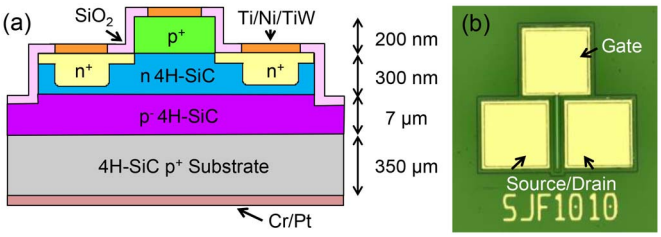

FIGURE 1. 4H-SiC lateral JFET. (a) Schematic cross section and (b) optical micrograph of a fabricated device with gate length $L = 10$ μm and gate width $W = 100$ μm.

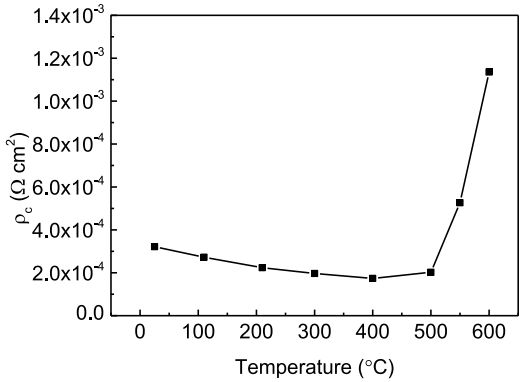

FIGURE 2. Temperature dependence of specific contact resistance (ρ_C) for a Ti/Ni/TiW metal stack on n^+ 4H-SiC.

(by Ascatron AB): firstly a 5 μm-thick lightly doped p-type (p^-) layer with dopant concentration 2×10^{15} cm^{-3}, followed by a 300 nm-thick n-type (n) layer with dopant concentration 1×10^{17} cm^{-3}, and finally a 200 nm-thick heavily doped p-type (p^+) layer with dopant concentration 2×10^{19} cm^{-3}. The p^+ layer is used to form the gate electrode, whereas the n layer comprises the channel region of the JFET. The thickness and dopant concentration of the n layer set the threshold voltage (V_T) of the transistor. A timed etch was used to pattern the p^+ gate electrode in a transformer coupled plasma (TCP) etcher with gas flows of 90 sccm Cl_2 and 10 sccm BCl_3 and radio-frequency (RF) power of 150 W. Then a 1 μm-thick SiO_2 masking layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) and patterned to expose the source and drain regions to nitrogen implantation at 600 °C to form heavily doped n-type (n^+) regions required for practically ohmic metallic contacts, with reduced crystalline damage [9]. A series of implants was performed with doses of 1.4×10^{15}, 7×10^{14} and 3.6×10^{14} at energies of 60, 40 and 20 keV, respectively, to achieve a box-like depth profile with nitrogen concentration greater than 10^{19} cm^{-3}, based on technology computer aided design (TCAD) process simulations [10]. After ion implantation, the SiO_2 layer was removed in a buffered oxide etch solution (hydrofluoric acid). A second series of shallower nitrogen implants was performed with doses of 3.2×10^{12}, 8×10^{11}, 1.2×10^{12} and 1×10^{12} at energies of 33, 24, 18, and 10 keV, respectively [11]. Afterwards a 2 μm-thick PECVD SiO_2 capping layer was deposited and the implanted dopants were electrically activated by thermal annealing at 1450 °C in Argon (Ar) atmosphere for 30 minutes. The capping layer was removed before a mesa etch was used to electrically isolate individual devices using the TCP etcher. A passivating layer of PECVD SiO_2 was then deposited and patterned to expose the metal contact regions. Subsequently a multi-layered stack of 50 nm titanium (Ti), 100 nm nickel (Ni) and 50 nm titanium-tungsten (TiW, 10% Ti, 90% W) was deposited and patterned via lift-off to form the metal contacts. The metal contacts were sintered by rapid thermal annealing (RTA) at 1000 °C for 2 minutes in Ar ambient. For integrated circuit fabrication (not shown in this paper), a 200 nm-thick layer of TiW was deposited and patterned to form the first level of metal interconnects. Finally, a second level of metal interconnects and backside contact was formed using 20 nm-thick chromium (Cr) and 180 nm-thick platinum (Pt) by lift-off process. Fig. 1(b) shows the optical image of a fabricated 4H-SiC lateral JFET with gate length $L = 10$ μm and gate width $W = 100$ μm. Considering that the distance between the metal contacts of source/drain and the gate region is 5 um, the active channel area is 2×10^{-5} cm^2. Note that the contact metal in the gate region is protected by PECVD SiO_2 for better device operating lifetime.

The fabricated devices were characterized using a high-temperature probe station (Signatone Inc.) at temperatures up to 600 °C. An Agilent B2912A precision source/measurement unit with tungsten probe tips was used to measure the current-*vs*.-voltage (*I-V*) characteristics of the devices.

III. RESULTS AND DISCUSSION

Contact between metal and n^+ 4H-SiC is rectifying (*i.e.* a Schottky contact) and becomes ohmic after RTA. The specific contact resistance (ρ_c) between a metal and semiconductor was extracted from electrical measurements using the transmission line method (TLM) [5]. Fig. 2 shows how ρ_c depends on temperature. It decreases slightly with increasing temperature in the range from 25 °C to 400 °C due to increasing average electron kinetic energy and hence current density [12]. However, it increases with increasing temperature in the range from 400 °C to 600 °C, to 1.14×10^{-3} Ω cm^2, due to thermal degradation of the metal contacts.

It should be noted that the metallic contact to p^+ 4H-SiC is still Schottky in nature after the RTA. However, since the gate current of a JFET is very small, this is acceptable [4].

Fig. 3(a) shows drain current (I_{DS}) versus drain-to-source voltage (V_{DS}) characteristics measured at room temperature, corresponding to various values of gate-to-source voltage (V_{GS}), for a JFET with $L = 10$ μm and $W = 100$ μm. Considering that the active channel area is 2×10^{-5} cm^2, the specific on-resistance ($R_{on,sp}$) is 59.3 mΩ cm^2. Note that the device is on at $V_{GS} = 0$ V and that a negative value of V_{GS} (less than -7 V) is necessary to turn it off. The channel-length modulation parameter (λ) has a very low value of 3.88×10^{-3}V^{-1}. The saturation current is 16.8 mA/mm

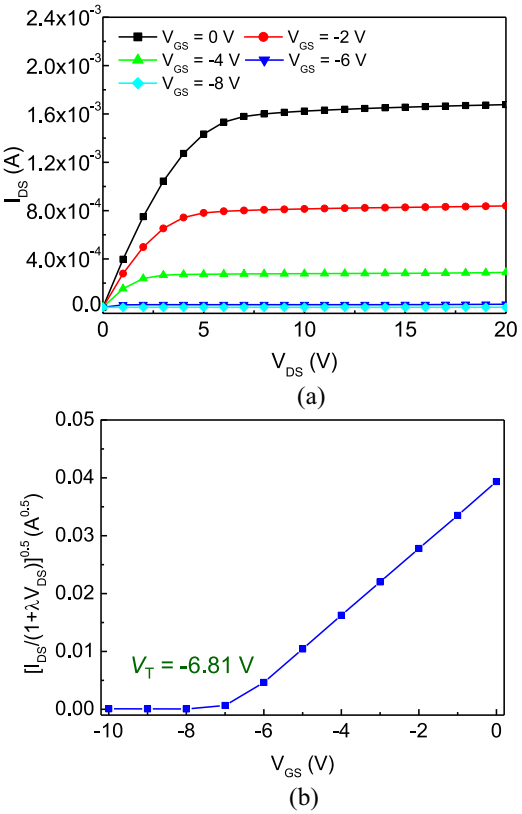

FIGURE 3. Measured electrical characteristics of 4H-SiC n-channel JFET with W/L = 100 μm/10 μm at 25 °C. (a) I_{DS}-V_{DS} for different values of V_{GS}. (b) $\sqrt{I_{DS}}$-V_{GS} for V_{DS} = 20 V.

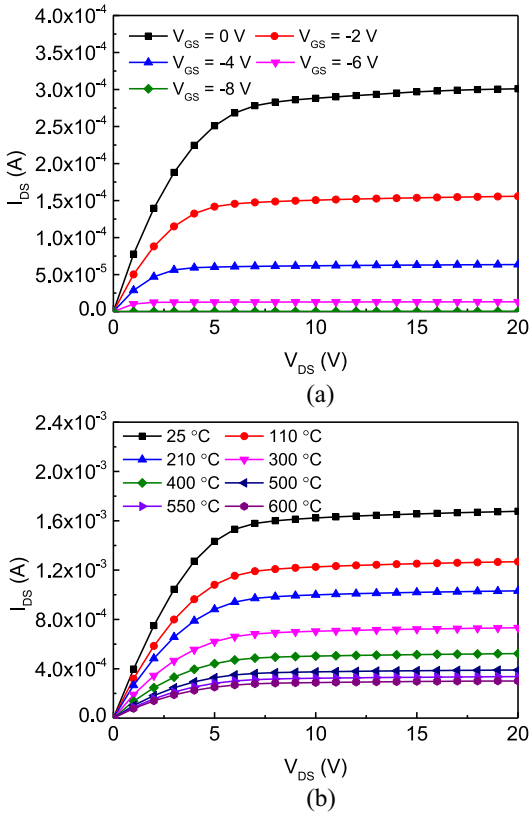

FIGURE 4. Measured I_{DS}-V_{DS} characteristics of 4H-SiC n-channel JFET with W/L = 100 μm/10 μm. (a) At 600 °C, for different values of V_{GS}. (b) At various temperatures, for V_{GS} = 0 V.

and by considering that the channel layer is 300 nm and the channel width is 100 um (for a cross-sectional area of $3\text{x}10^{-7}$ cm^2), the current density is 5600 A/cm^2 for V_{DS} = 20 V and V_{GS} = 0 V. Fig. 3(b) plots the square root of the saturation current as a function of V_{GS}, from which V_T is extrapolated (as the x-intercept) to be approximately -6.8 V at 25 °C.

Fig. 4(a) shows that the JFET has well-behaved characteristics at 600 °C. Fig. 4(b) shows how the I_{DS}-V_{DS} curve for V_{GS} = 0 V changes with temperature. Despite the built-in voltage decreases by approximately 0.5 V [13] and the effective width of the channel becomes wider from 25 °C to 600 °C. A monotonic decrease in drain saturation current (I_{Dsat}) with increasing temperature is observed. This can be attributed to the decrease of electron mobility at elevated temperatures, which follows a power law [14]. This decrease also causes $R_{on,sp}$ to increase to 280.2 mΩ cm^2 at 600 °C.

The off-state current (I_{off}) for V_{GS} = -9 V increases from 6.31×10^{-9} A to 1.97×10^{-7} A as the temperature increases from room temperature to 600 °C, due to increased intrinsic carrier concentration [14]. The increase in I_{off} is significantly larger than theoretically predicted, however, suggesting the presence of trap states (*e.g.* associated with crystalline defects caused by ion implantation). The saturation (V_{DS} = 20 V) on-current (V_{GS} = 0 V) to off-current (V_{GS} = -9 V) ratio, I_{Dsat}/I_{off}, is 2.66×10^5 at room temperature and decreases to 1.53×10^3 at 600 °C. This is in contrast to the 6H-SiC n-channel JFET with W/L = 200 μm/10 μm reported by NASA, which initially exhibited I_{Dsat}/I_{off} of only ~50 at 500 °C and after hundreds of hours of "burn-in" (to make the Ti/$TaSi_2$/Pt metal contacts ohmic) improved I_{Dsat}/I_{off} to be more than 10^3 [7].

The transconductance (g_m) can be extracted from the measured I-V characteristics using the square-law analytical model [4]. g_m for the 4H-SiC JFET in this work is 4.94 μS/μm (normalized to the channel width of 100 μm) at room temperature for V_{GS} = 0 V, which is approximately two times larger than g_m for the 6H-SiC JFET of a similar device configuration reported in [15]. The temperature dependences of g_m and intrinsic gain ($g_m r_o$) are shown in Fig. 5. The intrinsic gain has a relatively weak dependence on temperature because the output resistance (r_o) increases from 1.65×10^5 Ω to 7.25×10^5 Ω as the temperature increases from room temperature to 600 °C, compensating for the reduction in g_m with increasing temperature. These results indicate that the 4H-SiC JFET is promising for high-temperature amplifier applications. Measured performance parameters are summarized in Table 1, for V_{GS} = 0 V in the on state.

To evaluate the long-term reliability of the 4H-SiC JFET, the sample was periodically heated to 540 °C and 600 °C on a pre-heated hot-plate and a high temperature probe station in ambient air, respectively. The measured g_m changes

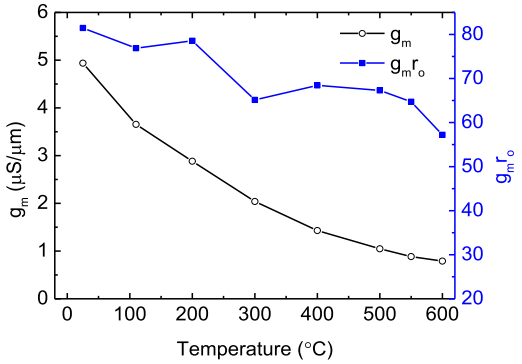

FIGURE 5. Temperature dependences of transconductance (g_m) and intrinsic gain ($g_m r_o$) of a 4H-SiC n-channel JFET with $W/L = 100\ \mu m/10\ \mu m$.

TABLE 1. Extracted 4H-SIC N-channel JFET performance parameters at various temperatures.

Temperature (°C)	V_T (V)	g_m ($\mu S/\mu m$)	$R_{on,sp}$ ($m\Omega\ cm^2$)	r_o (Ω)	$g_m r_o$	I_{Dsat}/I_{off}
25	-6.81	4.94	59.3	1.65×10^5	81.5	2.66×10^5
110	-6.95	3.65	72.0	2.10×10^5	76.9	9.88×10^4
210	-7.15	2.88	87.3	2.73×10^5	78.6	8.96×10^4
300	-7.19	2.04	123.21	3.20×10^5	65.1	4.24×10^4
400	-7.31	1.43	172.24	4.78×10^5	68.4	2.44×10^4
500	-7.45	1.05	214.00	6.42×10^5	67.3	1.15×10^4
550	-7.60	0.88	249.17	7.32×10^5	64.7	1.56×10^3
600	-7.63	0.79	280.23	7.25×10^5	57.2	1.53×10^3

approximately by 3 % over the 90 hour test at 540 °C, but it changes by 30 % for the 1 hour test at 600 °C. Further studies of the possible degradation mechanisms, such as contact degradation and charge trapping at the channel interfaces, are warranted.

IV. CONCLUSION

Lateral depletion-mode 4H-SiC n-channel JFETs are demonstrated to perform well at temperatures up to 600 °C. A relatively high transconductance of 4.94 μS/μm and low specific on-resistance of 59.3 mΩ cm^2 are achieved at room temperature. As the operating temperature increases, the threshold voltage shifts by -1.38 mV/ °C. Due to mobility degradation at elevated temperatures, the transconductance decreases to 0.79 μS/μm at 600 °C and the on/off drain saturation current ratio decreases to 1.53×10^3; however, the intrinsic gain remains higher than 50 at 600 °C. This work demonstrates that 4H-SiC JFETs are promising for use in extremely harsh environments.

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