Received 18 June 2014; revised 15 July 2014; accepted 19 July 2014. Date of publication 23 July 2014; date of current version 23 October 2014. The review of this paper was arranged by Editor T.-L. Ren.

Digital Object Identifier 10.1109/JEDS.2014.2342738

# A Combined Modulation of Set Current With Reset Voltage to Achieve 2-bit/cell Performance for Filament-Based RRAM

FANG YUAN (Student Member, IEEE), ZHIGANG ZHANG, LIYANG PAN, AND JUN XU

Institute of Microelectronics, Tsinghua University, Beijing 100084, China CORRESPONDING AUTHOR: F. YUAN (e-mail: yuanf09@mails.tsinghua.edu.cn) This work was supported in part by the State Key Development Program for Basic Research of China under Grant 2011CBA00602 and in part by the National Natural Science Foundation of China under Grant 20111300789.

**ABSTRACT** A combined operation scheme to realize multibit switching in filament-based bipolar RRAM device is proposed. By combining the modulations of the current compliance in set operations with the stop voltage in reset operations together, the size or the quantity of the filaments in the film bulk can be controlled. An RRAM device with the structure of  $Ag/HfO_x/Pt$  is fabricated and the 2-bit/cell memory function is achieved by the proposed modulation. Furthermore, the 2-bit/cell data reliability is satisfactory including the high-temperature retention, cycling endurance.

**INDEX TERMS** Multibit, conducting filament, current compliance (CC), reset voltage, combined modulation, resistive switching.

## I. INTRODUCTION

With the rocketing development in the consumer electronics industry, the urgent need for high-density and large-capacity nonvolatile memory never stops. Many solutions have been proposed to multiply the density of traditional flash memory, including multi-bit (multi-level) storage [1], [2], 3D stack [3], [4], etc. At the same time, some novel transistor-free memory devices come up, e.g., phase change memory (PCM) [5], magnetoresistive random access memory (MRAM) [6], resistive random access memory (RRAM) [7], [8], etc. Among these new memories, RRAM has drawn a great research interest because of its many advantages which can compete with flash memory, such as large data window, fast switching speed, low power consumption, excellent reliability, and superb potential in scaling down [7]–[9]. Moreover, multi-bit memory ability of RRAM has been proved feasible to effectively increase memory density [10]-[14]. For filament-based RRAM, 2 modulation methods can implement multi-bit switching: compliance current modulation [11], [12] and reset stop voltage modulation [13], [14], both of which are aiming at controlling the size or quantity of the filaments in the film to change the resistance states. And consequently, by using the current or

voltage modulation methods, to improve the multi-bit RRAM performance and reliability should be considered and studied.

In this work, an operation method combing the 2 modulations is proposed.  $HfO_x$  is chosen as the memory functional material for multi-bit switching validation due to its excellent CMOS process compatibility and outstanding performance in RRAM applications [9], [12]. A filament-based RRAM device with the structure of Ag/HfO<sub>x</sub>/Pt is fabricated. A 2-bit storage capacity of the Ag/HfO<sub>x</sub>/Pt device is realized by the proposed conjoined modulation of both current compliance in set operations and the stop voltage in reset operations. The 2-bit/cell RRAM device displays satisfactory performance in terms of memory window and switching reliability.

### **II. EXPERIMENT**

The Ag/HfO<sub>x</sub>/Pt MIM devices are fabricated on a p type Si wafer with a 300-nm-thick SiO<sub>2</sub> film as the isolation layer. A 2-nm-thick Ti film as an adhesion layer and a 100-nm-thick Pt film as the common bottom electrode (BE) were sequentially deposited by thermal evaporation. Next, an HfO<sub>x</sub> film with the thickness of 20nm was deposited by atomic layer deposition (ALD) at 220 °C. Finally, a

Personal use is also permitted, but republication/redistribution requires IEEE permission.

See http://www.ieee.org/publications\_standards/publications/rights/index.html for more information.



**FIGURE 1.** (a) *I-V* characteristics of Ag/HfO<sub>X</sub>/Pt device with different CC on a semi-logarithmic scale. (b) *I-V* curves with different CC in reset procedures on a linear scale. The schematic of the device structure is illustrated in the inset figure. (c) Maximum reset current and resistance in LRS as a function of CC. (d) Temperature dependence of LRS resistance set by CC of 10 and 100  $\mu$ A respectively. The values of  $\alpha$  indicate the element of conducting filaments is Ag.

100-nm-thick Ag film as top electrode (TE) was grown by thermal evaporation and followed by patterning with a circular shadow mask. The electrical characteristics of the fabricated RRAM devices were carried out by an Agilent B1500A semiconductor device analyzer at various temperatures. In all electrical measurements, the bias voltage was applied to the Ag TE and the Pt BE was grounded.

### **III. RESULTS AND DISCUSSION**

Fig. 1(a) shows the current - voltage (I-V) characteristics of the Ag/HfOx/Pt RRAM device with different compliance current (CC) in set operations. The device exhibits a bipolar switching behavior with positive bias to set and negative bias to reset. To clearly identify each reset switching, the *I-V* curves are redrawn on a linear scale in Fig. 2(b). As CC increases, the maximum current in reset procedures (Ireset, max) increases. Meanwhile, the slope of the I-V curves before current dropping increases, which indicates the resistance (the reciprocal of the slope) decreases accordingly. Fig. 1(c) shows the I<sub>reset,max</sub> and the resistance in low resistance state (LRS) as a function of the CC in set operations. The increase in  $I_{\text{reset},\text{max}}$  and decrease in LRS resistance strongly suggest a conducting-filament-based conduction in LRS. Many researches have verified that a larger current compliance permits a formation of wider or larger quantity conductive filaments within the thin film, leading to a lower resistance in LRS. On the other hand, the device in LRS with more filaments or wider filaments needs a larger current to break the filaments and reset the device





FIGURE 2. (a) *I-V* curves with different stop voltage in reset operations on a semi-logarithmic scale. (b) Set voltage and resistance in LRS as a function of the stop voltage in reset operations.

back to high resistance state (HRS) [11]. Furthermore, to find out the constituents of the conducting filaments, the temperature dependence of the LRS resistance is studied, using two devices set by the CC of 10 and 100  $\mu$ A, respectively. The thermal coefficients of resistivity  $\alpha$  are extracted, of which is shown in Fig. 1(d). The  $\alpha$  values for 10 and 100  $\mu$ A LRS devices are calculated to be  $3.953 \times 10^{-3}$  and  $3.932 \times 10^{-3}$  K<sup>-1</sup> respectively, which are quite close to the value of  $3.80 \times 10^{-3}$  K<sup>-1</sup> for high-purity silver at 293 K [15]. It indicates that Ag filaments form and govern the conducting in LRS of the devices. Considering a large enough resistance window and the tolerance of the reset current, the LRS resistances set with the CC of 10 and 100  $\mu$ A are chosen to realize 2 of the 4 memory states (about 10<sup>4</sup> and  $10^2\Omega$ , respectively).

The other way to achieve multi-level resistance states is to vary the stop voltage (V<sub>stop</sub>) in reset operations, owning to the gradual current fall in the reset procedures, as shown in Fig. 2(a). A later stop in the negative voltage sweep leads more conducting filaments to break or the conducting filaments to become narrower in LRS devices, in another word, the LRS device is reset to a more complete extent. As a result, a higher LRS resistance is obtained, and the set voltage (Vset) required to set the device to the former LRS resistance will increase due to the fewer or narrower conducting filaments existing within the film [13], [14]. Fig. 2(b) illustrates the V<sub>set</sub> and the LRS resistance as a function of the V<sub>stop</sub> in the reset operations. In Fig. 2(b), except for the  $V_{stop}$  of -0.5 V, which almost fails to reset the device, as the  $V_{stop}$  increases from -1.0 to -3.0 V, the  $V_{set}$  and the LRS resistance both increase. And when V<sub>stop</sub> the exceeds -3.0 V, both of the V<sub>set</sub> and the LRS resistance reach a relatively steady value, which means the device is fully reset back to original HRS. Similar to the CC modulation, for a sufficient memory window, the LRS resistances reset with the V<sub>stop</sub> of -1.0 V and -3.0 V are chosen and the difference of resistance values is over 3 orders. Therefore, the other 2 of the 4 memory states is achieved (about  $10^7$  and  $10^{10}\Omega$ , respectively), and the 2-bit/cell resistive switching is realized by the combination of controlling the CC and V<sub>stop</sub> simultaneously.



**FIGURE 3.** (a) Multi-bit resistance window comparison between three operation methods: only CC in set process, only  $V_{stop}$  in reset process, and combined modulation of CC and  $V_{stop}$ . (b) 2-bit resistance distribution realized by the proposed combined modulation of CC and  $V_{stop}$ .

In Fig. 3(a), a comparison of multi-bit resistance windows realized by the three types of operation is presented. The black squares shows the resistance value difference controlled by CC in the set process, which has an obviously non-uniform and narrow (smaller than one order) window between each resistance level. The blue circles are the resistance levels obtained by various Vstop during reset operations, which also shows the lack of sufficient resistance margin. However, by using the combined modulation and choosing proper CC (10 and 100  $\mu$ A) and V<sub>stop</sub>(-1.0 and -3.0 V), an enlarged memory window with 2-3 orders can be reached, which is shown as the green areas in Fig. 3(a). Fig. 3(b) shows the 2-bit/cell resistance distribution extracted from 30 random device samples. The large enough read-out windows between each level demonstrate the robust ability of the proposed modulation method by combing the CC with V<sub>stop</sub>.

Fig. 4 illustrates the proposed switching mechanism of 2-bit/cell Ag/HfOx/Pt RRAM device. The initial state of the device is in HRS as bit "11", and some Ag atoms (yellow circles) have already diffused into the  $HfO_x$  film during the fabrication process. In the set operations, when positive voltage is applied to Ag TE, the electrical field pushes Ag+ ions into the film bulk and drift towards Pt BE. As reaching Pt BE, the Ag+ ions are reduced to Ag atoms and establish one or more filaments penetrating the  $HfO_x$  film to form conducting channels (bright blue area). The set operations with CC of 100 and 10  $\mu$ A build more or wider conducting filaments and fewer or narrower ones respectively in the  $HfO_x$  film, resulting in transferring the data state to bit "00" and bit "01" accordingly. Oppositely, in the reset operations, negative voltage is applied to Ag TE and the electrical field oxidizes the Ag atoms from the conducting filaments to Ag+ ions. The Ag+ ions are attracted back to Ag TE so that the filaments shrink or even break down, which brings the film back to relatively higher resistance. Thus, the reset operations with different V<sub>stop</sub> of -1.0 and -3.0V drive the device to bit "10" with fewer or narrower filaments and bit "11" without any filaments, respectively. Physically, the 2-bit/cell switching is achieved by controlling the size or the quantity of the conducting filaments inside the  $HfO_x$  film bulk. And electrically, the 2-bit/cell memory function is realized



FIGURE 4. Proposed switching mechanism of the 2-bit/cell Ag/HfOx/Pt RRAM device.



FIGURE 5. (a) Cycling test sequence and (b) 2-bit/cell data endurance and read disturbance of the Ag/HfO<sub>x</sub>/Pt RRAM device.



**FIGURE 6.** 2-bit/cell data retention performance of the Ag/HfO<sub>x</sub>/Pt RRAM device.

by the combined modulation of the current compliance in set operations and the stop voltage in reset operations.

The endurance performance and the read disturbance of the 2-bit/cell switching is presented in Fig. 5. The switching cycling is operated in the sequence as: set bit "11" to bit "01" with the CC of 10  $\mu$ A, set bit "01" to bit "00" with the CC of 100  $\mu$ A, reset bit "00" to bit "10" with the V<sub>stop</sub> of -1.0 V, and reset bit "10" to bit "11" with the V<sub>stop</sub> of -3.0 V. At each bit level, the resistance is read with +0.1 V for 5 times to check the disturbance, which is demonstrated in Fig. 5(a). By using this cycling operation, the device exhibits satisfactory read disturbance of over 1000 cycles with negligible memory window degradation, as shown in Fig. 5(b).

Fig. 6 shows the retention performance of the Ag/HfO<sub>x</sub>/Pt RRAM device. The 4 states of resistance are operated by the combination of setting with CC of 100 and 10  $\mu$ A, resetting with V<sub>stop</sub> of -1.0 V and -3.0V, respectively, and the 4 states correspond to bit "00", "01", "10" and "11", respectively. All the 4 states of data can keep stable at 85 °C for at least 10<sup>4</sup> seconds. It appears satisfactory that there is a memory margin of 2-3 orders in resistance value between each level, which is competent for 2-bit/cell RRAM applications.

### **IV. CONCLUSION**

In summary, a combined operation scheme to realize multibit resistive switching is proposed. The operation method combines the modulations of both the current compliance in the set operations and the stop voltage in the reset operations. An RRAM device with the structure of  $Ag/HfO_x/Pt$ is fabricated and the 2-bit/cell memory function is verified by the proposed operation method. The data reliability is satisfactory for future multi-bit RRAM applications.

#### REFERENCES

- K. Yoshikawa, "Impact of cell threshold voltage distribution in the array of flash memories on scaled and multilevel flash cell design," in *Proc. VLSI Symp. Tech. Dig.*, 1996. pp. 240–241.
- [2] C. W. Oh *et al.*, "A 4-bit double SONOS memory (DSM) with 4 storage nodes per cell for ultimate multi-bit operation," in *Proc. VLSI Symp. Tech. Dig.*, 2006, pp. 40–41.
- [3] R. Katsumata *et al.*, "Pipe-shaped BiCS flash memory with 16 stacked layers and multi-level-cell operation for ultra high density storage devices," in *Proc. VLSI Symp. Tech. Dig.*, 2009, pp. 136–137.
- [4] J. Jang et al., "Vertical cell array using TCAT (terabit cell array transistor) technology for ultra high density NAND flash memory," in Proc. VLSI Symp. Tech. Dig., 2009, pp. 192–193.
- [5] H.-S. P. Wong *et al.*, "Phase change memory," *Proc. IEEE*, vol. 98, no. 12, pp. 2201–2227, Dec. 2010.
- [6] S. Tehrani *et al.*, "Magnetoresistive random access memory using magnetic tunnel junctions," *Proc. IEEE*, vol. 91, no. 5, pp. 703–714, May 2003.
- [7] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-based resistive switching memories- Nanoionic mechanisms, prospects, and challenges," *Adv. Mater.*, vol. 21, nos. 25–26, pp. 2632–2663, 2009.
- [8] H.-S. P. Wong *et al.*, "Metal–oxide RRAM," *Proc. IEEE*, vol. 100, no. 6, pp. 1951–1970, Jun. 2012.
- [9] Y. S. Chen et al., "Highly scalable hafnium oxide memory with improvements of resistive distribution and read disturb immunity," in Proc. Int. Electron Devices Meeting (IEDM) Tech. Dig., Baltimore, MD, USA, 2009, pp. 1–4.
- [10] J. Park *et al.*, "Multibit operation of TiO<sub>x</sub>-based ReRAM by schottky barrier height engineering," *IEEE Electron Device Lett.*, vol. 32, no. 4, pp. 476–478, Apr. 2011.
- [11] C. Rohde et al., "Identification of a determining parameter for resistive switching of TiO<sub>2</sub> thin films," Appl. Phys. Lett., vol. 86, no. 26, pp. 262907–262907-3, Jun. 2005.
- [12] Y. Wang *et al.*, "Investigation of resistive switching in Cu-doped HfO<sub>2</sub> thin film for multilevel non-volatile memory applications," *Nanotechnology*, vol. 21, no. 4, Jan. 2010, Art. ID 045202.
- [13] S. Yu, X. Guan, and H.-S. P. Wong, "On the switching parameter variation of metal oxide RRAM—Part II: Model corroboration and device design strategy," *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1183–1188, Apr. 2012.
- [14] J.-C. Wang et al., "High-performance multilevel resistive switching gadolinium oxide memristors with hydrogen plasma immersion ion implantation treatment," *IEEE Electron Device Lett.*, vol. 35, no. 4, pp. 452–454, Apr. 2014.
- [15] R. C. Weast, CRC Handbook of Chemistry and Physics, vol. 69. Boca Raton, FL, USA: CRC press, 1988.



FANG YUAN was born in Wuhu, China. She received the B.S. degree from the School of Microelectronics, Xidian University, Xi'an, China, in 2009, and is currently pursuing the Ph.D. degree from the Institute of Microelectronics, Tsinghua University, Beijing, China. Her current research interests include fabrication and characterization of RRAM materials, novel nonvolatile memory design, and 3-D memory structure and devices.



**ZHIGANG ZHANG** received the B.S. and the Ph.D. degrees in science from Nanjing University, Nanjing, China, in 1987 and 2000, respectively. From 2000 to 2002, he was a Research Associate with the University of Cambridge, Cambridge, U.K. In 2002, he joined IMIT, KTH, as a Senior Guest Researcher. Since 2004, he has been with the Institute of Microelectronics, Tsinghua University, Beijing, China. His current research interests include nonvolatile memories and quantum devices.



**LIYANG PAN** received the B.S., M.S., and the Ph.D. degrees in microelectronics from Hefei University of Technology, Hefei, China, Zhejiang University, Zhejiang, China, and Tsinghua University, Beijing, China, in 1996, 1999, and 2003, respectively. Since 2003, he has been with the Institute of Microelectronics, Tsinghua University. His current research interests include memory devices, circuits, and systems.



**JUN XU** was born in Hefei, China. He received the B.S. degree in electronic engineering from Tsinghua University, Beijing, China, in 1986, and the M.S. and Ph.D. degrees in electrical engineering from Shaanxi Institute of Microelectronics, Xi'an, China, in 1989 and 1994, respectively. He joined the Institute of Microelectronics, Tsinghua University, in 1994, as a Post-Doctoral Researcher, and then promoted as an Associate Professor, where he worked on deep submicron CMOS VLSI devices and process development. From

1997 to 1999, he was with the Solid-State Device Simulation Group, University of New Orleans, LA, USA, working on the numerical simulation and design optimization of deep submicron MOSFET's operating at low temperature and low voltage. He is currently a Full Professor with the Institute of Microelectronics, Tsinghua University. His current research interests include nano-scale high performance CMOS devices and technology.