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Controlling Ambipolar Current in Tunneling FETs Using Overlapping Gate-on-Drain

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ABSTRACT In this paper, we have demonstrated that overlapping the gate on the drain can suppress the ambipolar conduction, which is an inherent property of a tunnel field effect transistor (TFET). Unlike in the conventional TFET where the gate controls the tunneling barrier width at both source-channel and channel-drain interfaces for different polarity of gate voltage, overlapping the gate on the drain limits the gate to control only the tunneling barrier width at the source-channel interface irrespective of the polarity of the gate voltage. As a result, the proposed overlapping gate-on-drain TFET exhibits suppressed ambipolar conduction even when the drain doping is as high as 1×10^{19} cm^{-3}.

INDEX TERMS Ambipolarity, overlapping gate-on-drain, TFET, tunneling barrier width, overlap length.

I. INTRODUCTION

Tunnel field effect transistor, as a promising future low power device, comes with advantages like lower leakage current, less than 60 mV/decade subthreshold swing (SS) at room temperature and less susceptibility of short channel effects [1]–[7]. But it also comes along with its unique property of ambipolarity, which is conduction of current for both high negative and high positive gate voltages. Ambipolar conduction makes the TFET less effective in complementary circuit applications restricting its utility in digital circuit design [2], [8].

Several methods have been attempted to control the ambipolar conduction in TFETs [2], [8]–[11]: (i) Reduce the electric field on the drain side by increasing the gate-drain distance or by using heterogeneous gate dielectrics, (ii) increase the depletion region width on the drain side by decreasing the drain doping, (iii) use large bandgap heterostructures on the drain side to increase the tunneling width. Although the above methods reduce the ambipolar conduction, they can lead to (a) reduction in ON-state current, (b) increase in the drain series resistance and (c) added process complexity.

If the ambipolar conduction can be controlled without the above limitations, the TFETs would become attractive candidates for complimentary digital circuit design. In this paper, we demonstrate that using an overlapping gate-on-drain, the ambipolar conduction can be efficiently controlled for drain dopings up to $N_D = 1 \times 10^{19}$ cm^{-3}. In all the structures (e.g. underlapped, lower drain doping and high bandgap drain) reported earlier [2], [8]–[11], the gate is present only over the intrinsic channel region. In our paper, we have suggested overlapping the gate on the heavily doped drain and provided a clear explanation for the reduced ambipolar conduction. We have compared our proposed approach with the conventional TFET using calibrated TCAD simulations to show the efficacy of overlapping gate-on-drain side in reducing the ambipolarity.

II. DEVICE STRUCTURE AND OPERATION

The schematic view of (a) the conventional TFET and (b) the overlapping gate-on-drain TFET are shown in Fig. 1. For both the devices, the parameters used in our simulation are: silicon film thickness t_{si} = 10 nm, gate oxide thickness (SiO_2) t_{ox} = 3 nm, channel length (L) = 50 nm, gate work function = 4.5 eV, source doping $N_A = 1 \times 10^{20}$cm^{-3} and channel doping $N_D = 1 \times 10^{17}$cm^{-3} and drain doping $N_D = 1 \times 10^{19}$ cm^{-3}.

In the conventional TFET, the gate controls only the channel region, i.e., it changes the tunneling barrier width either at source-channel interface or at the channel-drain interface depending on the polarity of the gate voltage for the conduction of current. A high positive gate voltage makes the

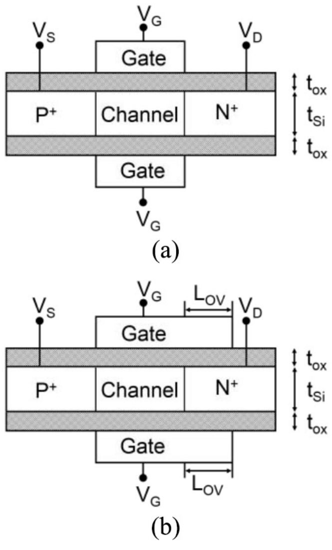

FIGURE 1. Schematic view of (a) conventional TFET and (b) overlapping gate-on-drain TFET.

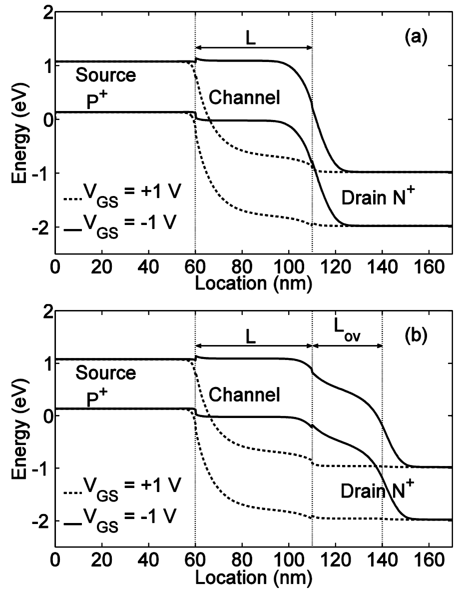

FIGURE 2. Energy-band profiles of (a) conventional TFET and (b) overlapping gate-on-drain TFET for $V_{GS} = -1.0$ V, $V_{GS} = +1.0$ V, $V_{DS} = 1.0$ V, and $L_{ov} = 30$ nm.

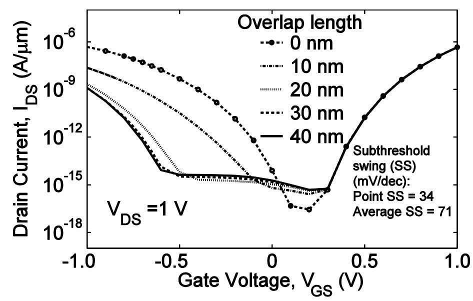

FIGURE 3. Transfer characteristics of the overlapping gate-on-drain TFET for different overlapped gate length L_{ov} where $L_{ov} = 0$ nm corresponds to the conventional TFET [Fig. 1(a)]. The drain doping is $N_D = 1 \times 10^{19}$ cm^{-3} and channel lengh $L = 50$ nm.

tunneling barrier width narrower at the p^+ source – channel interface leading to a drain current and a high negative gate voltage narrows the tunneling barrier width at the n^+ drain – channel interface again resulting in a drain current. This ambipolar conduction makes the TFET unsuitable for complementary digital circuits.

To minimize the ambipolar conduction, the OFF-state tunneling barrier width at the n^+ drain – channel interface should not be narrowed when the gate voltage polarity is changed. This can be achieved if the gate is overlapped over the drain as shown in Fig. 1(b).

Fig. 2 shows the band diagram for both the conventional TFET and the overlapping gate-on-drain TFET at a gate voltage $V_{GS} = -1.0$ V, $V_{GS} = +1.0$ V and a drain voltage $V_{DS} = 1.0$ V. As shown in Fig. 2(a), for the conventional TFET, (i) for a positive gate voltage, the tunneling barrier width at the p^+ source – channel interface becomes narrow and (ii) for a negative gate voltage, the tunneling barrier width at the n^+ drain – channel interface becomes narrow resulting in ambipolar conduction. However, with the overlapping gate-on-drain TFET shown in Fig. 2(b), for a positive gate voltage, the tunneling barrier width at the p^+ source – channel interface becomes narrow as in the case of the conventional TFET. But, since the effect of the gate voltage over both the channel and the overlapped region of the drain is the same for the overlapping gate-on-drain TFET, there is no narrowing of the tunneling barrier width at the n^+ drain – channel interface when the gate voltage is negative reducing the possibility of ambipolar conduction.

III. RESULTS AND DISCUSSIONS

All the simulations were done in Silvaco Atlas, Version 5.18.3.R [12]. We use a nonlocal band-to-band tunneling (BTBT) model to take into account the tunneling along the lateral direction. To include the mobility effect, concentration dependent model is used in our simulation. Band-gap narrowing (BGN) model is also enabled for high doping concentration in the source and drain regions. We have used the Fermi Dirac statistics and the Shockley-Read-Hall (SRH) recombination model. We have calibrated our simulation models by reproducing the results reported in [4].

The effect of changing the gate-on-drain overlap length L_{ov} on the ambipolar conduction is shown in Fig. 3. Since, the overlap length determines the tunnelling barrier width in the drain region, it is seen that as the overlap length increases, the ambipolar current is effectively controlled.

The ambipolarity is significantly suppressed in the overlapping gate-on-drain TFET for gate voltages as large as -0.5 V and overlap length $L_{ov} \geq 20$ nm. The overlap length can be chosen depending on the choice of tolerable ambipolar current for a given application. Therefore, by using a suitable value for L_{ov}, not only can the ambipolar conduction be controlled but also the gate-on-drain overlap capacitance can be kept to its minimum value. However,

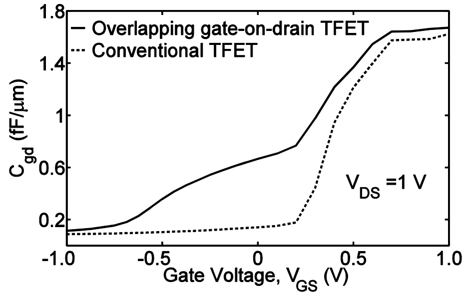

FIGURE 4. Simulated gate-drain capacitance (C_{gd}) of the overlapping gate-on-drain TFET (gate length $L_g = L + L_{ov} = 50 + 30$ nm) and the conventional TFET (gate length $L_g = L + L_{ov} = 80 + 0$ nm). The drain doping concentration of both the TFETs is $N_D = 1 \times 10^{19}$ cm^{-3}.

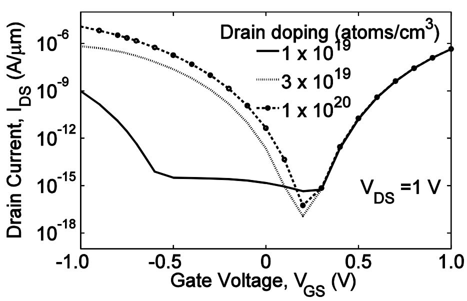

FIGURE 5. Transfer characteristics of the overlapping gate-on-drain TFET for different levels of drain doping. The overlapped gate length L_{ov} is 30 nm.

when the gate voltage polarity is changed, the conventional TFET ($L_{ov} = 0$ nm) exhibits a strong ambipolar conduction due to the narrowing of tunneling barrier width at both the source-channel and the drain-channel interfaces as shown in Fig. 2(a).

Since the gate is overlapped on the drain in the proposed structure to reduce the ambiplolar conduction, we need to examine if the drain overlap capacitance will affect the total gate-drain capacitance $C_{gd} = C_{of} + C_{dif} + C_{sif} + C_{dov} + C_{gd,inv}$ where C_{of} is the outer fringing capacitance, C_{dov} is the drain overlap capacitance and C_{dif} and C_{sif} are the inner fringing capacitances at the drain and source sides, respectively [13]. For identical gate lengths, the simulated gate-drain capacitance (C_{gd}) of the overlapping gate-on-drain TFET (gate length $L_g = L + L_{ov} = 50$ nm + 30 nm) and the conventional TFET (gate length $L_g = L + L_{ov} = 80$ nm + 0 nm) is shown in Fig. 4. We observe that in the ON-state, the total gate-drain capacitance C_{gd} is approximately identical for both the devices indicating that the AC performance will not be negatively impacted if the gate length is kept constant, as also demonstrated in [13].

The effect of drain doping on the ambipolar conduction for the overlapping gate-on-drain TFET is shown in Fig. 5. We observe that the ambipolar current increases significantly as the drain doping is increased above 1×10^{19} cm^{-3}. To understand this increase in the ambipolar current, the energy band profile of the overlapping gate-on-drain TFET with different drain doping levels is shown in Fig. 6. Up

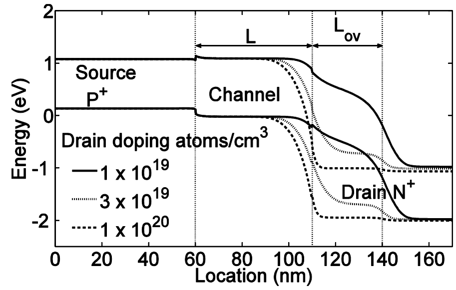

FIGURE 6. Energy-band profiles of the overlapping gate-on-drain TFET for $V_{GS} = -1.0$ V, $V_{DS} = 1.0$ V, and $L_{ov} = 30$ nm for high levels of drain doping.

to 1×10^{19} cm^{-3}, the tunnel barrier width is larger due to the overlapped gate-on-drain resulting in a suppressed ambipolar conduction as shown in Fig. 5. However, as the drain doping is increased above 1×10^{19} cm^{-3}, the gate potential in the overlapped gate-on-drain region becomes ineffective in modulating the band bending. Therefore, it results in a narrower tunnel barrier width increasing the ambipolar conduction.

IV. CONCLUSION

In this paper, using 2D simulations, we have studied the impact of overlapping the gate on the drain region as an effective means to control the ambipolar conduction in a TFET. We demonstrate that by overlapping the gate over the drain region, the ambipolar conduction can be suppressed in a TFET. For drain dopings up to $N_D = 1 \times 10^{19}$ cm^{-3}, the proposed approach effectively suppresses the ambipolar conduction in a TFET. Our results need to be confirmed by measurements.

REFERENCES

[1] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.
[2] T. Krishnamohan, D. Kim, S. Raghunathan, and K. C. Saraswat, "Double-gate strained-Ge heterostructure tunneling FET (TFET) with record high drive currents and <60 mV/dec subthreshold slope," in *Proc. IEDM Tech. Dig.*, San Francisco, CA, USA, 2008, pp. 947–949.
[3] P. F. Wang *et al.*, "Complementary tunneling transistor for low power application," *Solid-State Electron.*, vol. 48, no. 12, pp. 2281–2286, Dec. 2004.
[4] K. Boucart and A. M. Ionescu, "Double gate tunnel FET with high-k gate dielectric," *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1725–1733, Jul. 2007.
[5] M. J. Kumar and S. Janardhanan, "Doping-less tunnel field effect transistor: Design and investigation," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3285–3290, Oct. 2013.
[6] S. Saurabh and M. J. Kumar, "Estimation and compensation of process induced variations in nanoscale tunnel field effect transistors (TFETs) for improved reliability," *IEEE Trans. Device Mater. Rel.*, vol. 10, no. 3, pp. 390–395, Sep. 2010.
[7] S. Saurabh and M. J. Kumar, "Impact of strain on drain current and threshold voltage of nanoscale double gate tunnel field effect transistor (TFET): Theoretical investigation and analysis," *Jpn. J. Appl. Phys.*, vol. 48, Article ID 064503, Jun. 2009.
[8] A. Hraziia, C. Andrei, A. Vladimirescu, A. Amara, and C. Anghel, "An analysis on the ambipolar current in Si double-gate tunnel FETs," *Solid-State Electron.*, vol. 70, pp. 67–72, Apr. 2012.
[9] W. Y. Choi and W. Lee, "Hetero-gate-dielectric tunnelling field effect transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2317–2319, Sep. 2010.

[10] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, "Tunnel field-effect transistor without gate–drain overlap," *Appl. Phys. Lett.*, vol. 91, no. 5, pp. 053102–053103, Jul. 2007.
[11] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "SOI TFETs: Suppression of ambipolar leakage and low-frequency noise behavior," in *Proc. ESSDERC*, Sevilla, Spain, 2010, pp. 341–344.
[12] *ATLAS Device Simulation Software*, Silvaco Int., Santa Clara, CA, USA, 2014.
[13] Y. Yang *et al.*, "Tunneling field-effect transistor: Capacitance components and modelling," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 753–754, Jul. 2010.

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