CMOS Compatible Fabrication Processes for the Digital Micromirror Device

Cuiling Gong, *Member, IEEE,* and Tim Hogan

***Abstract*—DLP® technology has been widely used in the display products since it was first introduced to the world in 1996 by Texas Instruments. Projectors powered by DLP® technology range from cinema projectors that light up large movie theater screens to palm-sized "Pico" projectors. The heart of the technology is the digital micromirror device (DMD) that features an addressable array of up to 8 million microscopic mirrors. DMDs are fabricated using standard semiconductor processing equipment. However due to the unique nature of MOEMS application and digital operation of the DMDs, special CMOS-compatible fabrication processes have been developed to produce highly reflective digital micromirrors with robust operation margin and long term reliability. This paper will present an overview of the fabrication processes of the DMDs.**

***Index Terms*—Microelectromechanical devices, spatial light modulators, fabrication, DMD, DLP.**

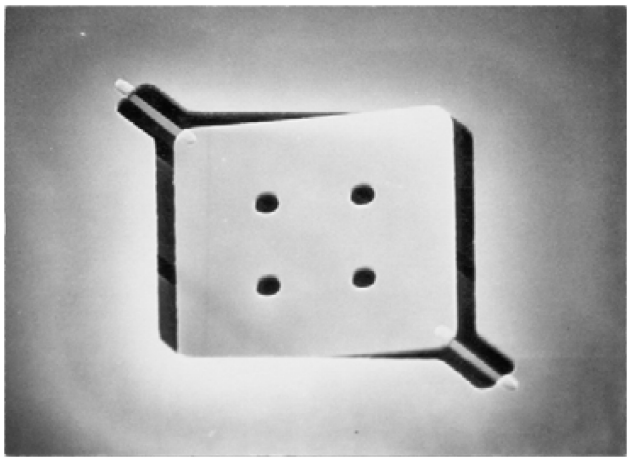

Fig. 1. The early digital micromirror device.

I. Introduction

THE DIGITAL Micro-mirror Device (DMD) evolved from an earlier membrane based analog design called the "deformable mirror device", first conceived in 1977 [1]–[3]. In 1987 Dr. Larry Hornbeck invented the digital micromirror, called DMD as shown in Fig. 1 [4]. The digital micromirror had a mirror plate supported by two exposed flexible hinges and was controlled by electrostatic forces. After nine years of intensive research and development, Texas Instruments introduced the first digital projectors based on DLP technology to the world in 1996. Today, DMD enabled products range from the tiny "Pico"- projectors that can fit into a smart phone to digital cinema projectors that can illuminate 33 meter cinema screens [5]–[12]. In addition, the DMD is used in many other display-oriented applications including medical imaging, mask-less lithography, structured lighting, rapid prototyping and more.

DMDs are fabricated using the standard semiconductor processing equipment. In order to meet image quality requirements for display applications, DMDs must have highly reflectivity and planar mirror surfaces. Consequently, film coating and deposition processes must be tightly controlled during the entire fabrication processes. An additional challenge for the fabrication of DMD arises from the requirement of monolithic integration of the micromirror structure atop the driving and signal processing electronics. Since the micromirrors are built directly over the CMOS wafer, the fabrication processes must be CMOS-compatible [13]–[16].

To help illustrate DMD fabrication processing, the micromirror architecture and the basic operation principles of the DMD will be presented in Section II. The details of a typical process flow and the corresponding fabrication steps to build the DMD are provided in Section III. Due to the nature of the mechanical motion of the micromirror and the sheer number of mirrors per chip, particle control plays a critical role for yield and reliability of DMD devices. Section IV will cover the practice and the impact of particle control followed by a summary in Section V.

II. Micromirror Architecture and Operation

A. Micromirror Architecture

An exploded view of the DMD micromirror is shown in Fig. 2 [17]–[19]. The micromirror has three metal layers which include M3 (CMOS level), hinge, and mirror layers. The M3 layer is built directly atop the CMOS SRAM cell and creates the voltages used by the address electrodes in the M3 layer. In addition to the address electrodes, the M3 layer has routings to conduct the bias (reset) voltages. The middle layer of metal

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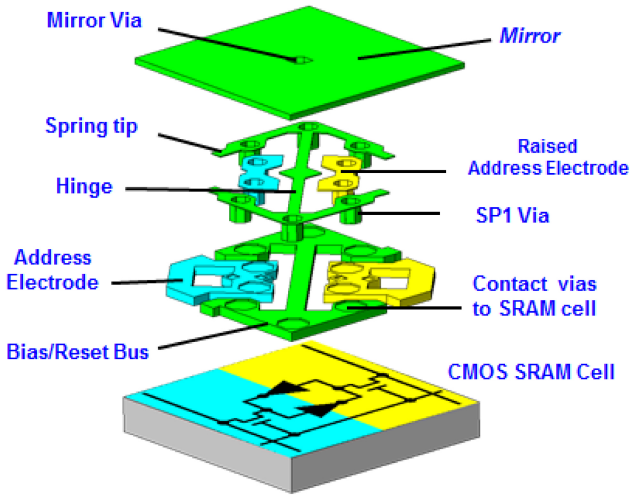

Fig. 2. The exploded view of a micromirror architecture with three metal layers on top of the CMOS SRAM cell. The bottom layer is called M3 layer includes address electrode and bias (or reset) bus. The middle layer is called the hinge layer and includes the hinge, spring tips, and raised address electrodes. The top layer is the mirror layer.

is called the hinge layer and incorporates a mirror-supporting hinge, raised address electrodes, and spring tips on which the mirror lands. The spring tips control the mirror's tilt angle and help the mirror to make dynamic transitions. The top layer is the free-standing reflective mirror.

Both the hinge and mirror metal layers sit atop sacrificial layers of photoresist, referred to as, "spacer-1" and "spacer-2". The metal layers are connected by vias in the spacer-1 and spacer-2 layers. The hinge level connects to the M3 level through spacer-1 for conduction of bias and address voltages. The mirror via connects through spacer-2 to couple the hinge and the mirror metal levels, allowing bias voltage connection to the mirror. Aluminum alloys used in the metal layers have been chosen based upon their ability to meet reflectivity, manufacturability, mechanical, and reliability requirements for the micromirror structure.

B. Micromirror Operation

DMD operation is driven by the electrostatic force. As previously described, the mirror is connected to the bias (or reset) signal through mirror and spacer-1 vias. The address electrodes in the M3 layer and the raised address electrodes in the hinge layer receive the complementary address voltages from the SRAM cell. When a digital video or graphic signal enters a DLP system, it activates the address electrodes. Electrostatic attraction created by the voltage difference between the mirrors and address electrodes drives the mirror to the desired landing state, as shown in Fig. 3.

When the mirror tilts toward the light source, it reflects light to the projection lens and it is in the "ON" state. The pixel appears bright in the projected image. When the mirror tilts away from the light source, it reflects light to a light absorber and it is in the "OFF state", and the corresponding pixel appears dark in the image. The shades of gray are created by controlling the time the pixel spends in the "ON" or "OFF" states during a frame time. For example, when a pixel is in

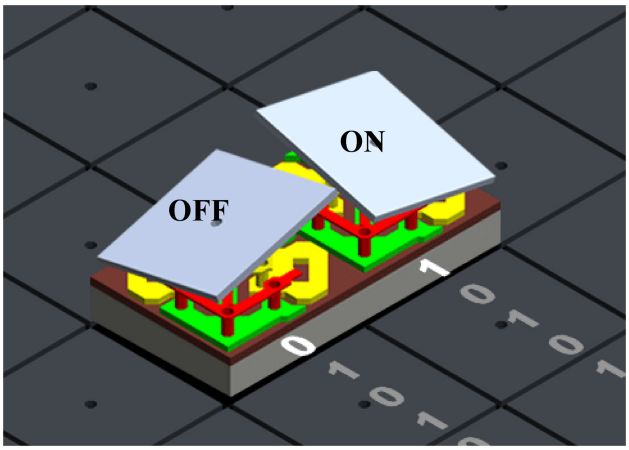

Fig. 3. The "ON" and "OFF" positions of micromirrors during operation. The mirror at the "ON" state reflects light to the project lens and the corresponding pixel is bright in the projected image. The mirror at the "OFF" state reflects light to the light dump and the pixel appears dark.

the "ON" or "OFF" state during the entire frame time it will be pure bright or dark. When the pixel spends half time in "ON" state and half time in "OFF" state, it will appear as a gray pixel. In single-chip DMD systems, color is created in the projected image by a synchronized color wheel in the illumination path. Larger systems use three DMD chips with each DMD reflecting one primary color.

Over the last twenty years, the unprecedented performance and reliability of the DMDs have been demonstrated. All micromirrors in the DMD chip must operate reliably throughout the lifetime of the device and this requires thorough engineering solutions for all aspects of the product [20], [21]. Among these factors, a robust manufacturing process is one of the most critical items. In the following section a typical DMD fabrication flow and the corresponding process steps are described.

III. DMD Fabrication Processes

The DMD architecture is built up using surface micromachining manufacturing processes. Since the micromirrors are built directly on top of the CMOS wafer, low temperature fabrication processes have to be used to build the micromirrors. Semiconductor photoresist was chosen for the sacrificial layer material, which is removed in the final processing steps using dry plasma ash processes. Photoresist also has the advantage of being a commonly used and widely available semiconductor processing material. A DMD process overview is shown below:

A. List of Fabrication Steps

1) Open contact vias to the SRAM cells.
2) Create first sacrificial layer, "spacer-1."
3) Deposit torsion hinge metal film.
4) Pattern and etch hinge metal.
5) Create second sacrificial layer "spacer-2."
6) Deposit mirror metal film.
7) Pattern and etch mirror metal.
8) Coat protective layer.
9) Package and remove sacrificial layers.

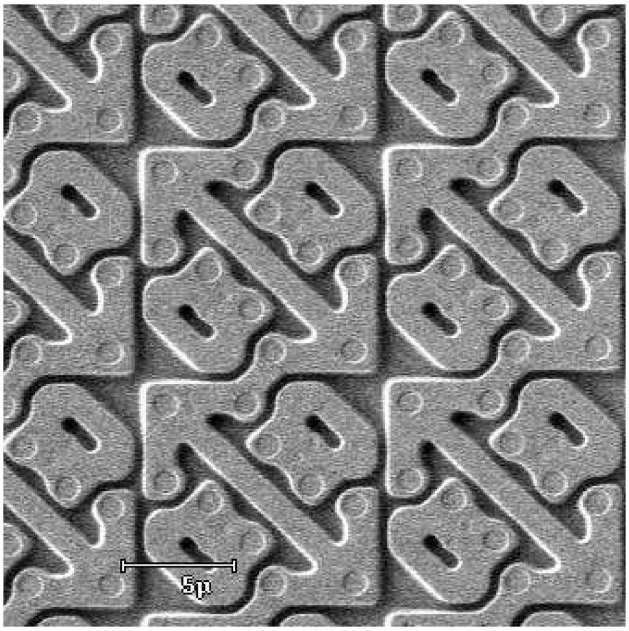

Fig. 4. Image of the M3 layer with vias opened to SRAM memory cell contacts after post M3 etch.

B. Description of Fabrication Steps

1) *Open Contact Vias to the SRAM Cells:* The CMOS wafers have been electrically tested to identify passing chips (also called "die") at the test facility before being shipped to the MEMS fabrication line. The wafers are coated with photoresist, exposed and developed to reveal regions where the vias will be etched. The vias allow an electrical connection to be made between the SRAM memory cell and the address structures of the DMD micromirror (or pixel). Vias are opened up for every pixel during the etch process, which is done with a dry plasma oxide-etch process. Upon completion of the etch process, the pattern resist is then removed to ready the wafer for building the micromirror stack. An image of the M3 layer with vias opened to SRAM memory cell contacts after post M3 etch is shown in Fig. 4.

2) *Create First Sacrificial Layer, "Spacer-1":* The first sacrificial layer, coined "spacer-1," involves coating the wafer with photoresist, exposing in the patterning stepper, and developing open the vias, as described in the contact-via process. The spacer films function both as a pattern mask and a sacrificial layer and are not removed until final assembly packaging. The vias opened up in the spacer -1 patterning process allow the subsequently deposited hinge metal film to contact the CMOS level via contacts.

Spacer thickness is chosen to achieve the desired pixel performance and the planarity required for the subsequent deposition step. A variety of measurement schemes can be employed to measure the spacer thickness. Standard semiconductor interferometry film thickness measurement schemes are the most common means of measuring resist film thicknesses.

3) *Deposition of Hinge Metal Film:* The next operations deposit the metal film that will make contact with the SRAM memory cell (through the address vias). This metal film also forms the torsion hinges and the spring tips. The hinges support the mirror and provide the torsional restoration force when the mirror is launched. The spring tips help the dynamic launch of the mirror and also serve as the rotating "stops" to control the tilt angle. The hinge metal is comprised of an aluminum alloy and is deposited by physical vapor deposition (PVD).

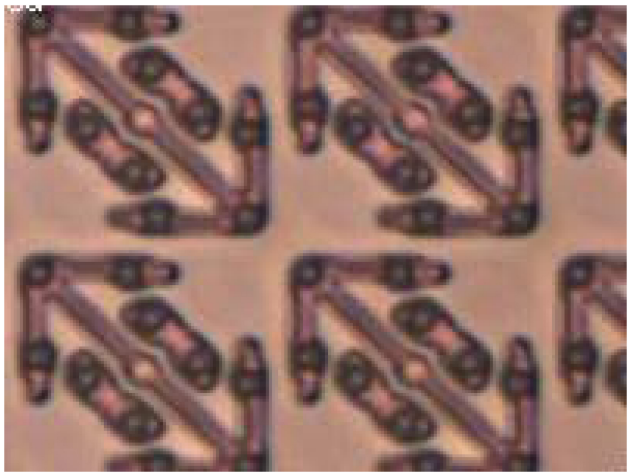

Fig. 5. An optical image of the top of the hinge pattern.

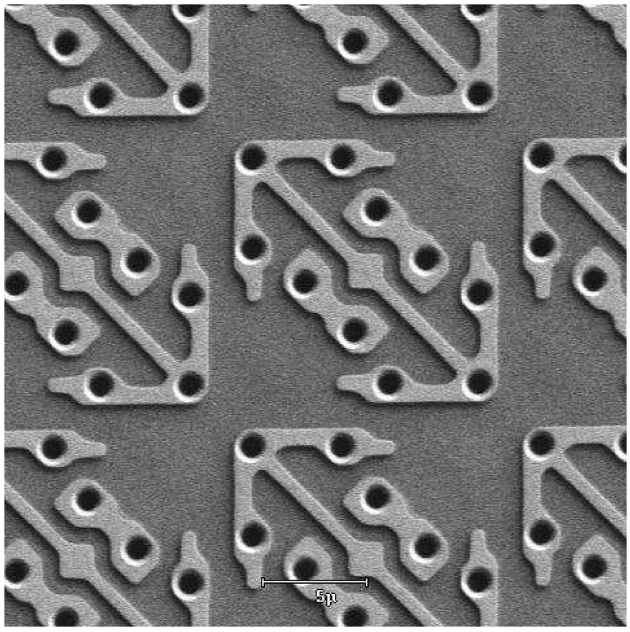

Fig. 6. Top view of the wafer after hinge level post-etch.

4) *Hinge Pattern and Etch:* The next process loop forms the hinge and raised address electrode structures. The wafer is now coated with photoresist, exposed and developed as in previous patterning steps. The torsion hinge properties are largely determined by the length and cross-sectional area of the hinge. An optical image of the hinge-patterned film is shown in Fig. 5.

After patterning, the hinge metal is plasma etched in a process tuned to etch the aluminum hinge metal film. Hinge pattern resist is then removed and the hinge dimensions are verified. Fig. 6 shows a typical view of the completed hinge level.

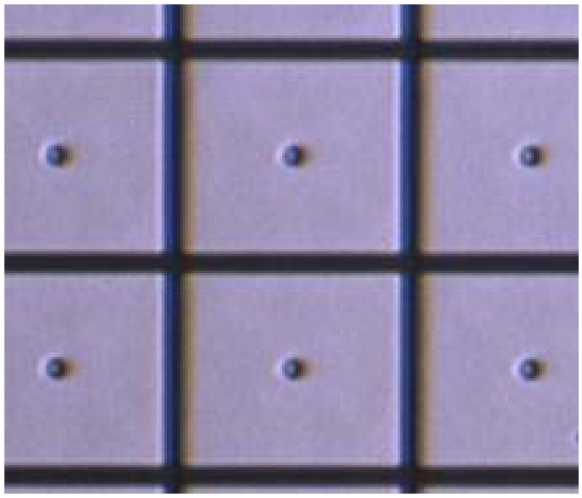

Fig. 7. Top view of the wafer after mirror metal etch.

5) *Coat and Pattern "Spacer-2":* Similar to spacer-1 processing, the second sacrificial layer "spacer-2," forming the region between hinge and mirror layers, is now coated atop the hinge level. Photoresist is coated and patterned (exposed and developed). The patterning step opens vias once again to form the connection between the mirror and hinge strap. This spacer plays a critical role in the uniformity of the mirror tilt angle. Therefore the process variation has to be tightly controlled across the wafer to ensure the tilt angle variation is within +/− 1degrees from the target tilt angle.

6) *Mirror Metal Deposition:* Aluminum-alloy mirror metal is now deposited on top of spacer-2, similar to the hinge metal deposition process. The thickness of the mirror is greater than the hinge and is determined by the dynamic performance requirements. A thicker mirror tends to stay "flatter" than a thinner mirror, yet will also result in a slower response time. Consequently, mirror thickness is chosen to balance the pixel switching speed performance with manufacturability and optical characteristics requirements.

7) *Mirror Pattern and Etch:* The mirror pattern and etch sequence separates each pixel so that they may act as an independent unit, although for now, they are still locked in place by the sacrificial spacer resist layers. The mirror etch process is similar to previously described pattern and etch process steps, differing by the pattern required to achieve the size, orientation and gap spacing between mirrors. An image of the micromirror array segments after mirror metal-etch is shown in Fig. 7.

8) *Protective Overcoat:* The final processing step is to add an overcoat of photoresist to the wafer surface to protect the mirrors from particles, moisture, etc. until assembly processing. The micromirror stack (also called "superstructure") processing is now complete and the wafers are ready for packaging and testing.

9) *Packaging and Sacrificial Layer Removal (Undercut):* Removal of the protective overcoat and sacrificial layers are packaging/assembly operations, yet a short description is included as the process is accomplished by plasma ashing, which was adapted from standard semiconductor processing methods.

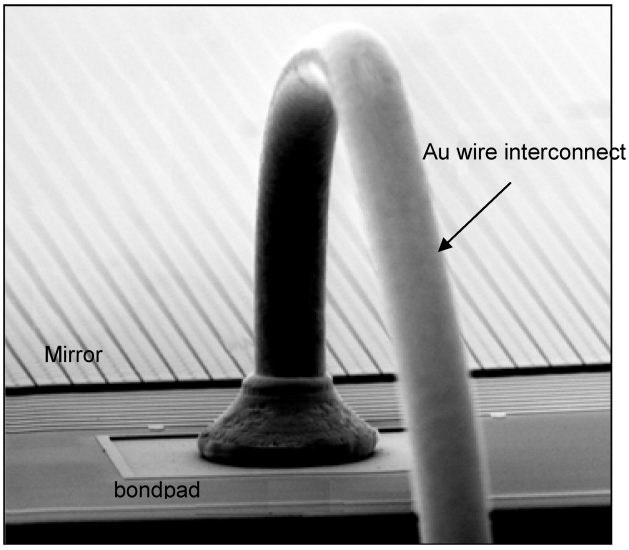

Fig. 8. DMD device with mirror undercut and wire bond interconnect processes complete.

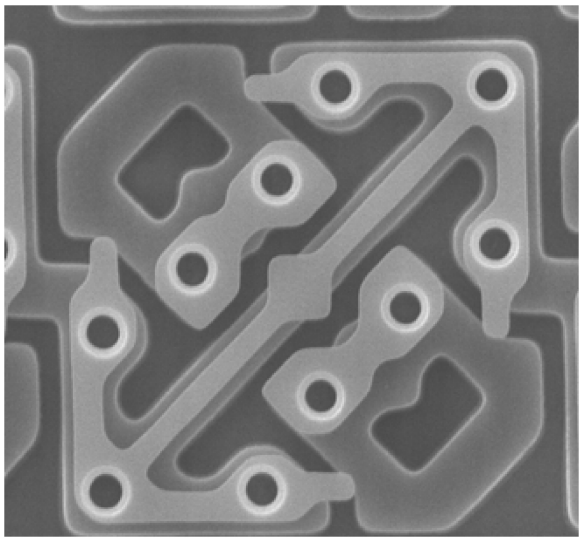

Fig. 9. Top view of a DMD micromirror after completing all fabrication processes (mirror was removed).

After the DMD chips are singulated, they are attached to a carrier package with an epoxy adhesive. The protective topcoat and spacer resist are removed by an oxygen-plasma ashing process, tuned to remove organic films. The process has been coined "undercutting" of the micromirror array. The sacrificial layers are ashed (combusted) through the mirror gaps of the array until the spacer material is removed and the mirror structure is free to rotate about the hinge axis.

The DMD chip is then wire-bonded to make electrical connection between the chip and package, and finally encapsulated with a clear window attached to top of the package. To help put the micromirror size in perspective, Fig. 8 shows an image that includes a wire interconnect on the edge of the DMD chip.

An image of the micromirror after going through all the fabrication processes is shown in Fig. 9. The uniformity of the spacer 1 via formation and the hinge geometry can be seen

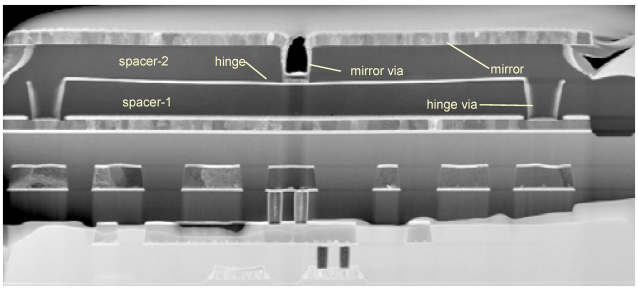

Fig. 10. Cross section view of the micromirror atop the underlying CMOS structure.

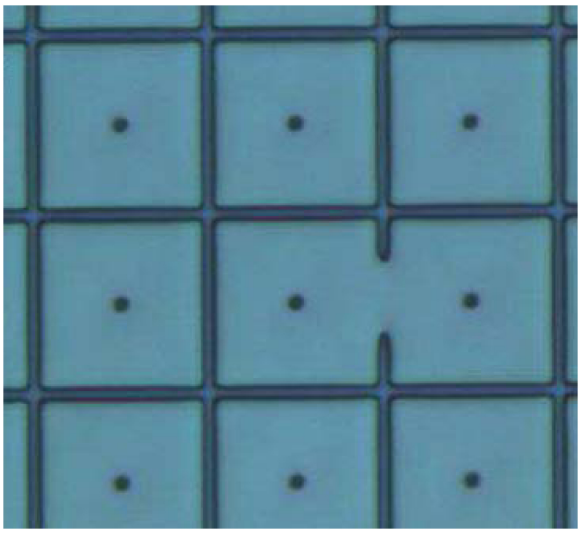

Fig. 11. An example of particle caused blocked mirror pattern.

clearly. The cross-sectional view of the DMD/CMOS stack atop the underlying CMOS structure is shown in Fig. 10. It clearly reveals the interconnections between the M3 layer and the hinge layer through hinge vias and the interconnection between the hinge layer and the mirror through the mirror via. The flatness of the mirrors and the uniformity of the hinge thickness are critical for image quality and dynamic operation of the micromirror.

IV. Particle Control

Key to achieving high-yield in semiconductor manufacturing is the control of particle contamination. MEMS fabrication, such as the DMD, also has stringent requirements for particle control, with added requirements of no loose particles since it is a device operating in free space, unlike a semiconductor chips which have no moving parts. Excellent particle control in all stages of wafer patterning, etch, metal deposition and handling operations are necessary to achieve high device yields and long term performance and reliability.

An example of a particle-induced defect that caused a DMD device to become operationally unacceptable is shown in Fig. 11. In this instance, a stray particle fell upon the coated wafer prior to pattern exposure. The particle blocked the exposure beam from the photoresist which subsequently blocked the etch-line from being formed. The resulting device has two inoperable mirrors, fused together instead of separated during the mirror-etch process.

Periodic tool particle level checks on process and handling tools as well as a robust preventative maintenance (PM) program are the backbone of effective particle control. Inline inspection schemes (i.e. optical, electron microscopy (SEM), laser-based detection) allow intervention for unexpected issues such as equipment component failures.

V. Summary

DMD manufacturing processes are developed to meet the unique requirements of the DMD operation and MOEMS applications. Low temperature MEMS fabrication processes using photoresist as the sacrificial material enables monolithic integration of the CMOS and MEMS manufacturing for the DMDs. Rigorous control methodologies ensure that the precision and stability of the critical dimensions of the micromirrors are achieved and maintained. Finally the integration of design, manufacturing and test capabilities makes the difference between proving a viable concept and building a successful product line.

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She joined DLP Products at Texas Instruments (TI), Dallas, TX, USA, in 2000 as a Mechanical Design Engineer. She was responsible for the design of the micromirrors used in the DMDs for eight years. She was later selected to join the first group of innovators to work on TI's future research and development projects at the Kilby Innovation Labs with a focus on microscale piezoelectric energy harvesting technology in 2008. She joined the faculty of the College of Science and Engineering at Texas Christian University, Fort Worth, TX, USA, in 2011.

Dr. Gong was elected to the Member of Group Technical Staff at TI in 2004. She received the Innovator in Action Award from TI in 2004 and the Texas Instruments Innovator Award in 2009. She has received six US Patents.

Tim Hogan joined Texas Instruments in 1984 with a degree in Mechanical Engineering from Iowa State University. He began work with Texas Instruments performing assembly/test/process-control process operations of Mil-Spec integrated circuits before joining the DMD Development Group in 1993. He is a Senior Member of the Texas Instruments technical staff where his research interests include wafer-level yield enhancement, process integration and SPC roles. He has received 5 US Patents and Co-Patents.