A Flexible 0.18 μm BiCMOS Technology Suitable for Various Applications

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***Abstract*—Hitachi's SiGe BiCMOS technology, which integrates 0.18 μm CMOS and a SiGe heterojunction bipolar transistor (HBT), does not degrade MOS or bipolar performance. The BiCMOS process is divided into blocks, and the ordering of their processing is optimized so that they do not interfere with each other. Low-thermal-budget SiGe HBT formation is achieved using a minimal-moisture-desorption oxide layer, thereby avoiding disturbing the CMOS process. This technology, which can also be applied to the 0.13 μm generation, has been used for applications ranging from high-speed ones like automotive radar and 40 Gbps optical communication to consumer ones like wireless.**

***Index Terms*—Bipolar transistor, BiCMOS, hydrogen termination, SiGe heterojunction bipolar transistor (HBT).**

I. Introduction

BICMOS TECHNOLOGIES have a long history of being used for various applications because they enable a high-speed and low-noise bipolar circuit to be flexibly combined with a low-dissipation CMOS circuit on the same chip. Initially, the formation of a bipolar junction transistor (BJT) in a BiCMOS process was very simple, so the BJT formation did not affect the MOS process or MOS device characteristics. Only a few additional processing steps were needed for forming the vertical junction structure of the BJT for the 1.3 μm and 2.0 μm generations [1]–[6]. Since the base region should be as thin as possible in the BJT formation process, the MOS-first process scheme was a natural choice for suppressing undesirable diffusion of the narrow and high-impurity-concentration emitter and base layers during MOS gate formation.

A double-polysilicon self-aligned BJT structure became possible with the 0.8 μm generation, and a complex bipolar /BiCMOS process was added [7]–[12]. The self-aligned BJT structure and deep trench isolation structure boosted transistor performance by reducing the parasitic resistance and capacitance. The next wave of BiCMOS technologies included new circuit technologies combining the same BJT high-performance as the base bipolar process with CMOS devices. The BiCMOS process enabled the fabrication of a composite circuit containing a CMOS logic gate and a current amplification circuit consisting of BJTs. A composite BiCMOS circuit that balanced circuit speed and power dissipation was developed in the 1980s [7]. Since CMOS performance had become good enough to handle the complex signal processing requirements of the 0.25 μm generation, circuits combining high-speed emitter-coupled logic (ECL) and high-density CMOS received attention as an alternative to BiCMOS gate technology [10].

The CMOS technology that came with the 0.25 μm generation was a driver of new technologies such as shallow trench isolation and silicide formation, which reduced the parasitic resistance and capacitance of bipolar transistors [13]. The cutoff frequency (f_T) improved from 4 GHz to 40 GHz, and the parasitic collector-base capacitance (Cjc) decreased from 33 fF to 1 fF, as illustrated in Fig. 1. The emitter size was reduced from $2\,\mu m \times 5\,\mu m$ to $0.2\,\mu m \times 1\,\mu m$ with increased collector current density, and the ECL gate delay time was reduced from 250 ps/gate to 25 ps/gate [11]. An accompanying technology was the application of a thick bonded SOI substrate in the BiCMOS process combined with deep trench isolation, enabling fabrication of a completely latch-up-free CMOS circuit and reduction of RF leakage current through the substrate [8]–[10], [12]–[14].

In the 2000s, SiGe technology has played the leading role in the formation of shallow base regions and thereby dramatically boosting bipolar performance [15]–[30]. Fig. 2 shows the tradeoff between f_T and the collector-emitter breakdown voltage (BVceo) of Si BJTs and SiGe heterojunction bipolar transistor (HBTs). The f_T with SiGe technology is two and half times that with Si BJT technology at the same BVceo. An f_T of over 240 GHz and an ECL gate delay time of less than 3 ps/gate were recently achieved with SiGe technology [23].

The enhancement of the CMOS technology used in the BiCMOS process in the 0.18 μm and 0.13 μm generations led to the quick development of various processes for combining different SiGe HBTs and different CMOS devices to meet various demands in different marketplaces. Device

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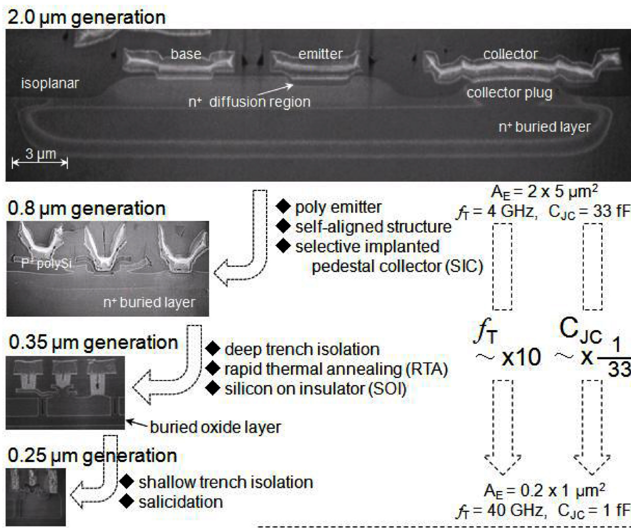

Fig. 1. SEM cross-sections of Si BJTs from 2.0 μm to 0.25 μm generation [13]; description of main technology innovation of each generation. Samples were slightly wet-etched using diluted fluonitric acid to emphasize highly doped areas.

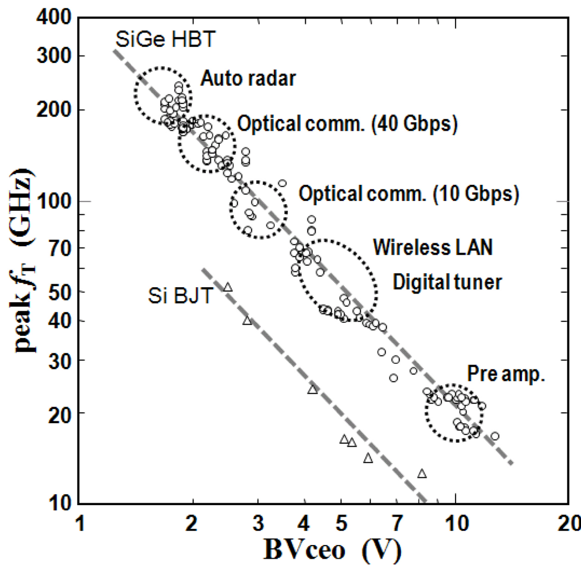

Fig. 2. Tradeoff between f_T and BVceo of SiGe HBTs and Si BJTs; both types were fabricated on Hitachi's 8 inch line. SiGe HBT performance is for 0.13 μm/0.18 μm/0.25 μm generations; Si BJT performance is for 0.35 μm/0.25 μm generations.

characteristics have tended to be optimized for specific market applications because each application has a different priority for the tradeoff between the f_T and BVceo of the SiGe HBTs. Moreover, the MOSFET supply voltage depends on the application. The combination of different kinds of MOSFETs and BJTs thus resulted in a great number of different BiCMOS technologies. Each one incurs its own development costs, including those for tuning the process conditions to match the device parameters, for confirming the reliability of new devices, and for preparing new design kits. A design kit consists of a set of compact models for both active and passive devices as well as interconnects, design checking rules that support circuit simulation and layout design, and intellectual property like a CMOS standard logic cell library.

This paper presents Hitachi's SiGe BiCMOS technology, which integrates 0.18 μm CMOS and 200 GHz SiGe HBTs, and explains why the changes in CMOS characteristics and layout rules must be minimized when implementing the original CMOS technology into the BiCMOS process. Section II explains the concept of constructing a flexible 0.18 μm BiCMOS technology suitable for various applications. Compatibility with a standard logic library was emphasized in previous papers [18], [23], [30], but a detailed description was not provided. A low thermal budget process, which does not affect MOS characteristics, may affect transistor yield. Section III describes the low thermal budget process used for forming SiGe HBTs so that changes in the CMOS characteristics are minimized and side effects are avoided. Section IV concludes with a summary of the key points.

II. Basic Concept of Constructing BICMOS Process

The basic concept of constructing Hitachi's BiCMOS process is to avoid disturbing the MOS process and to avoid degrading MOS and bipolar performance. Hitachi developed a 40 Gbps optical communication integrated circuit using a 0.25 μm SiGe bipolar process [31]. The same device performance as for a SiGe HBT made using the 0.25 μm process was achieved using 0.18 μm SiGe BiCMOS technology, which features CMOS circuits that handle signal speeds of up to 2.7 Gbps and ECL circuits on the same chip that handle 43 Gbps signals for use in optical communication systems. The drain currents of the NMOS and PMOS were 660 and 295 μA/μm, respectively. The high drain currents were achieved by inserting the P gate doping step before low thermal budget process of SiGe HBT formation. This process differs from other BiCMOS processes [15], [17], [18], [23]–[30], [35] as described in detail in Section III. A reported SiGe HBT has an f_T of 140 GHz, a maximum oscillation frequency (f_{MAX}) of 183 GHz, and a BVceo of 1.9 V [19], [21]. The application of carbon doping of 0.1 % in the intrinsic base region increased the f_T of the SiGe HBT to 211 GHz and the f_{MAX} to 204 GHz with 1.5 V BVceo, making it suitable to applications requiring even higher speed. The parasitic collector-base capacitance was 2.0 fF for an emitter size of 0.2 μm $\times$ 1.0 μm.

The three keys to implementing this concept are to optimize the order of the processing steps from the viewpoint of the thermal budget, to perform global planarization, and to avoid disturbing the optimized process module to reduce the length of the process.

A. Optimize Order of Thermal Processing Steps

In the 0.18 μm SiGe BiCMOS process sequence (Fig. 3), the bipolar fabrication blocks were added to the most appropriate places in the base CMOS process [19]. The heavy thermal processing steps for fabricating an n$^+$ buried layer (NBL), a collector Si epitaxial growth layer, a collector plug to n$^+$ buried

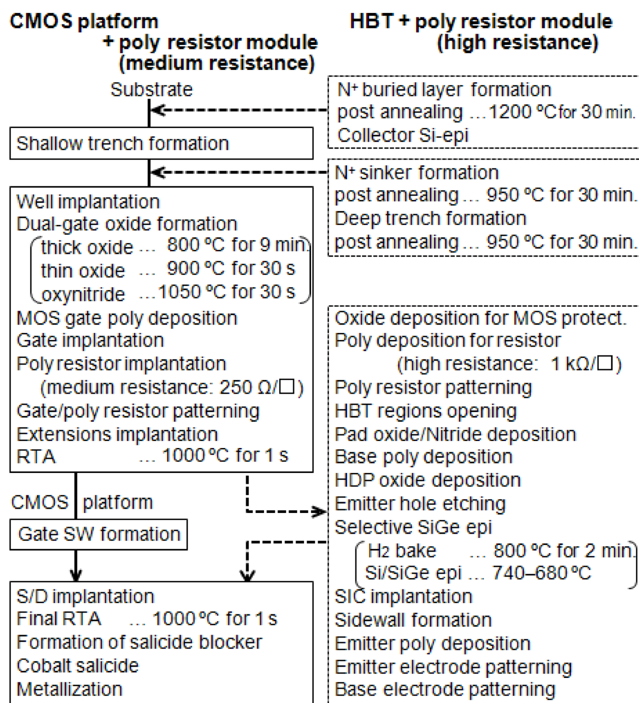

Fig. 3. Sequence of 0.18 μm SiGe BiCMOS process. Formation of passive components of sinker/metal-insulator-metal capacitors and Schottky barrier/varactor diodes explanation is omitted.

collector, and a deep trench are performed prior to the MOS process block.

A 30 nm thick pad oxide is formed at 1000 °C before deposition of high-density plasma (HDP) oxide for the shallow trenches, and a 4 nm thick pad oxide is formed at 750 °C before filling the deep trenches with high-temperature low-pressure oxide (HTO) at 800 °C. Both deposited oxide layers are densified at 950 °C for 30 minutes. Another 950 °C annealing immediately after implantation of phosphorus (5×10^{15} cm^{-2}) at an acceleration energy of 80 keV into the n$^+$ sinker region of the HBT is needed to recrystallize the damaged region because small defects due to the implantation might magnify the problem during a subsequent lower temperature deposition process step. A low-temperature process instead of the heavy thermal process cannot prevent the n$^+$ sinker layer and deep trench from possibly inducing crystal defects. The kind of material placed in the deep trench could also increase the possibility of defect occurrence. If polysilicon is used as the trench filling material [32], stress due to cap oxidation can cause crystal defects and/or changes in the BJT characteristics [9], [33]. The combination of low-stress oxide deposition and post annealing prevents this problem.

Dual gate oxide layers with thicknesses of 3.5 nm and 6.5 nm are fabricated for 1.8 V MOSFETs and 3.3 V MOSFETs, respectively. The oxynitride processing step (1050 °C for 30 s) is the step in the MOS formation block with the highest thermal budget. Deposition of a non-doped polysilicon layer is followed by N/P impurity MOS gate implantation, medium- resistance polysilicon resistor implantation, and dry etch patterning. A processing step using rapid thermal annealing (RTA) at over 1000 °C is carried out immediately

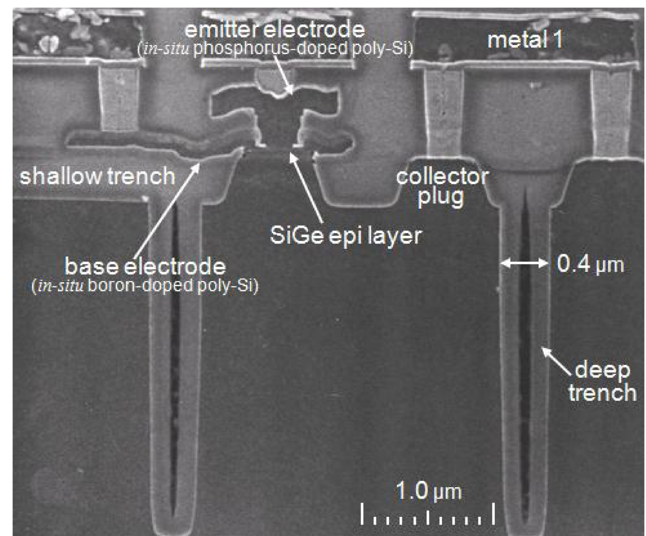

Fig. 4. SEM cross-sectional view of 0.18 μm based SiGe HBT. Cross-section of sample was slightly wet-etched using diluted HF.

after extension implantation to reduce the transient enhanced diffusion (TED) of impurities implanted in the extension and halo regions. The TED effect is usually observed in relatively low-temperature furnace annealing processes, and immediate RTA after implantation has been used to suppress the short channel effects in CMOS devices from the 0.18 μm generation [34]. The gate sidewall (SW) formation processing step includes thermal deposition of an oxide layer at a relatively low temperature.

Several SiGe HBTs have been developed using a combination of blanket SiGe epitaxial growth to form the intrinsic base region and selective boron-doped Si epitaxial growth to form the elevated extrinsic base layer [23], [30], [35]. The intrinsic base region of Hitachi's SiGe HBT is formed using selective SiGe epitaxial growth inside an emitter hole (Fig. 4, [20]). This process, which forms an emitter-base spacer as a self-aligned structure [29], enables formation of a fine emitter region that is beyond the ability of lithography technology. The processing steps start after deposition of an oxide layer on the MOS gates and a medium-resistance resistor. They include depositing *in-situ* boron-doped polysilicon and oxide layers, opening a bipolar hole where the SiGe epitaxial base will be grown, selectively growing the SiGe epitaxial base, depositing a series of dielectric and *in-situ* phosphorus-doped polysilicon layers, etching back the doped polysilicon to form a SW to separate the emitter and base electrodes, depositing an n$^+$ emitter polysilicon layer, and patterning emitter and base polysilicon electrodes. Final high-temperature (1000 °C) spike annealing is used to activate the impurities and form emitter regions in the HBT by diffusing phosphorus from the *in-situ* doped polysilicon into the Si layer selectively grown on the SiGe epitaxial base. Because the low thermal budgets throughout the HBT formation process are not sufficient to drive the boron impurities in non-doped polysilicon, the previous combination of non-doped polysilicon deposition and boron implantation was replaced by boron *in-situ* polysilicon deposition for the base electrode.

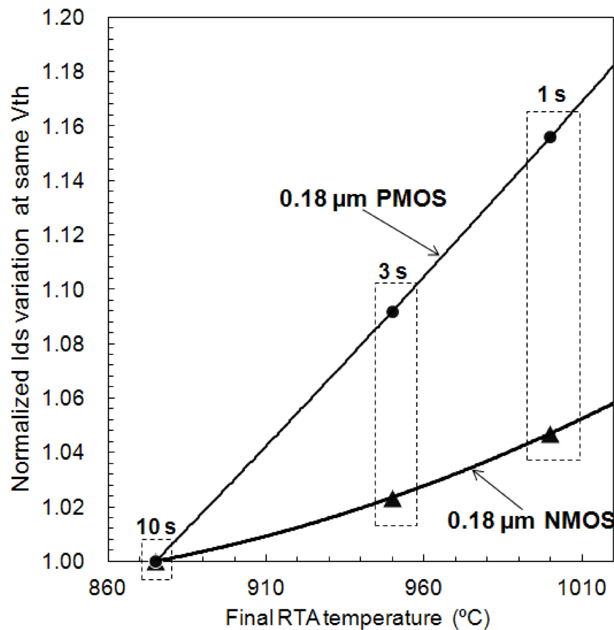

Fig. 5. Dependence of 0.18 μm MOSFET Ids on final RTA temperature. Increase in Ids is plotted from value at 875 °C. Annealing time was adjusted so that thermal budget was the same for each condition. Ids values were normalized to that at same Vth for different annealing temperatures.

The source/drain current (Ids) of MOSFETs fabricated with different final RTA temperatures normalized to that at the same Vth are plotted in Fig. 5. High-temperature annealing reduced the parasitic resistance and improved the current drivability of the MOSFETs. However, the final RTA needs to be performed quickly at high temperature to prevent excess phosphorus diffusion from the highly doped emitter poly-Si electrode. The cobalt self-aligned silicidation and metallization process steps are carried out, and the electrodes of a SiGe HBT with a high f_T of 200 GHz are connected by metallization [22].

B. Perform Global Planarization

Both the shallow and deep trenches should be planarized to enable fine MOS gates to be patterned on them even though the deep trenches are not used for separating MOSFETs. Because filling a deep trench is more difficult than filling a shallow one, the shallow and 0.4 μm wide deep trenches are formed separately in our SiGe BiCMOS process, as shown in Fig. 3.

Undoped silicate glass (USG) and HDP chemical vapor deposition (CVD) oxide have been widely used for filling shallow (0.35 μm deep) trenches. The USG process, which uses low-temperature and sub-atmospheric (600 Torr) conditions for mixing organic raw materials and ozone, results in good coverage for shallow high-aspect trenches but cannot fill a deep (2.5 μm) trench due to a short mean free path in the gas phase. The HDP CVD oxide process, which achieves good coverage by preventing clogging during Ar sputtering, creates reactive molecules with a short mean free path in the gas phase under low-temperature and relatively high-pressure (5 Torr) conditions, so it also cannot fill a deep trench. An HTO CVD process can fill a deep trench due to the long mean free path of the molecules in the gas phase, but its low coverage performance due to the short mean free path at the surface produces a weak adherence of the HTO layer at joints. This problem is overcome by depositing the HTO into the deep trenches twice by etching after the first deposition, resulting in joints that are not exposed on the device surface [12]. Fig. 4 shows a well-planarized deep trench structure underneath a base polysilicon electrode.

The use of a 1.0 μm wide trench with an air gap was reported to result in a record peripheral substrate capacitance of 0.02 fF/μm [35]. While a wider trench can suppress parasitic substrate capacitance, thicker oxide deposition is needed to fill a wider deep trench. A total deposition thickness of 1.0 μm was used to achieve a well-planarized surface on the 0.4 μm wide deep trenches (Fig. 4). Even though chemical mechanical polishing (CMP) was used to planarize the deep trenches, thickness fluctuation of the HTO layer on a wafer affects the planarization. We thus limited the deep trench width to 0.4 μm.

The height of Hitachi's first SiGe HBT was 0.8 μm [31]. It was subsequently reduced to 0.6 μm to enable integration of the 0.25 μm SiGe BiCMOS process without causing problems during inter-metal dielectric layer (IML) formation because the IML thickness is determined by the CMOS process technology. The height of the 0.18 μm based SiGe HBT was reduced to 0.48 μm to enable application to both 0.18 μm and 0.15 μm CMOS [19], [20].

Fig. 6 compares the height of the 0.18 μm based SiGe HBT and the IML thickness of 0.18 μm to 0.13 μm MOSFETs. The IML thickness is usually determined by the contact hole size, i.e., the need to keep the aspect ratio of the hole to around three. Although a self-aligned HBT using double poly-Si layers tends to be taller than the MOS gate, the height of the SiGe HBT must be reduced in accordance with the thickness of the IML. The height of the SiGe HBT can be reduced without degrading its performance when it is applied to 0.13 μm CMOS by using a thinner emitter and thinner base polysilicon layers [29]. An advanced BiCMOS could be integrated without reducing the IML thickness and contact hole size by reducing the gate length and optimizing the impurity profile of the MOSFET, but this would require much effort to redesign the standard CMOS circuit.

C. Keep Scheme of Optimized Process Module

Combining the CMOS process and bipolar process increases the number of processing steps, so techniques for reducing the number have been proposed. For instance, the N-well of the PMOS could use the NBL of the BJTs. Since the sheet resistance of the NBL in which Sb ions (2×10^{15} cm^{-3}) are implanted is 38 $\Omega/\square$, which is one-tenth that of the N-well in conventional PMOS, the PMOS N-well could be formed in the same layer as the NBL. However, this would reduce the flexibility needed to support a wide variety of applications.

Device characteristics are optimized by changing the Si epitaxial thickness and selective collector implantation (SIC) doping level in accordance with the tradeoff between f_T and BVceo (Fig. 2). If the PMOS N-well uses the NBL of the BJTs, the Si epitaxial thickness depends on the PMOS characteristics, and the flexibility of the BJT process is limited. The thickness of the Si epitaxial layer used for high-frequency

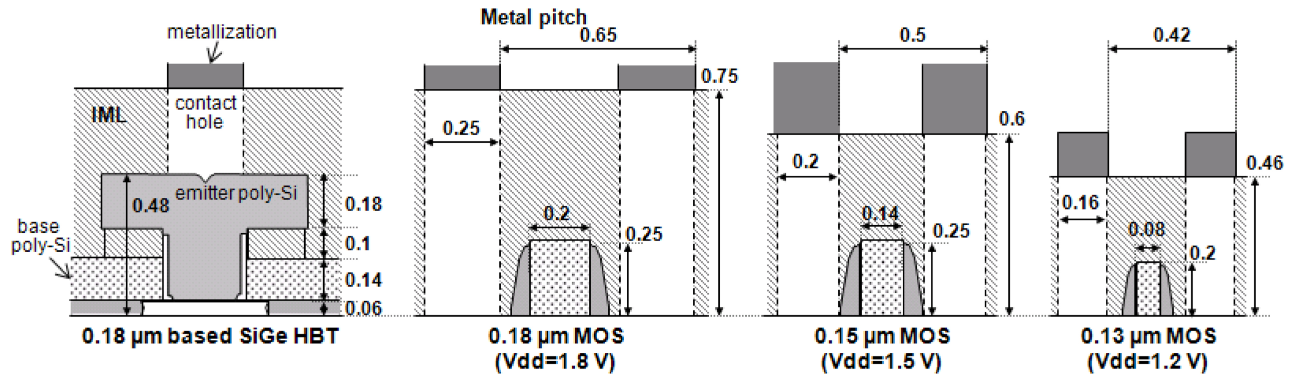

Fig. 6. Schematic cross-section and standard values for 0.18 μm SiGe HBT and 0.18 μm to 0.13 μm MOSFETs (all measurements in μm).

applications is less than 0.3 μm, and that for high-voltage applications could be more than 1.5 μm. SIC doping does not cover all areas from high frequency like 200 GHz to high voltage.

Another approach is to use the same polysilicon layer for a poly resistor and a MOS gate. However, doped NMOS and PMOS gates are not suitable as precise poly resistors for analog applications. The sheet resistance should have a small temperature coefficient of resistance (TCR), and the process conditions for the N and P gates should be independent of the TCR. A small TCR can be obtained during the formation of a polysilicon resistor through layer-by-layer polysilicon formation [16]. The polysilicon initially has small grains following deposition, and impurity implantation results in the formation of an amorphous layer on the upper layer of the polysilicon. This layer turns into large-grain polysilicon due to recrystallization after annealing.

The TCR for large-grain polysilicon is positive while that for small-grain polysilicon is negative due to the electrical characteristics of the grain boundary. The positive TCR reflects resistivity inside the grains, and the negative TCR reflects the barrier resistance of the grain boundary [36]. These opposite characteristics cancel out the temperature dependency of the resistivity. Implantation of BF_2 or Ge is used to form an exact layer-to-layer structure. Low-temperature implantation using fluorinate at -40 °C as a refrigerant can be used to suppress the formation of microcrystallines in the implanted amorphous layer.

The acceleration energy of the Ge implantation can change the TCR, as shown in Fig. 7. The TCR fluctuation was of the order of 100 ppm/°C, and a slightly negative TCR helps prevent thermal runaway of the circuit function. However, the process conditions for achieving a small-TCR 1 kΩ/□ resistor are not suitable for achieving 250 nm thick poly-Si. It is difficult to achieve a small TCR from low resistance to high resistance with the same polysilicon thickness. A higher Ge acceleration energy can be used to increase the relative amount of bigger grain sizes inside a polysilicon resistor. The thickness of the MOS gate with the 0.18 μm SiGe BiCMOS process is 0.25 μm, which is suitable for achieving 250 Ω/□. In this case, 0.25 μm is too thick to achieve 1 kΩ/□ with a small TCR. Thinner poly-Si is needed to achieve a small TCR and high-resistance resistor.

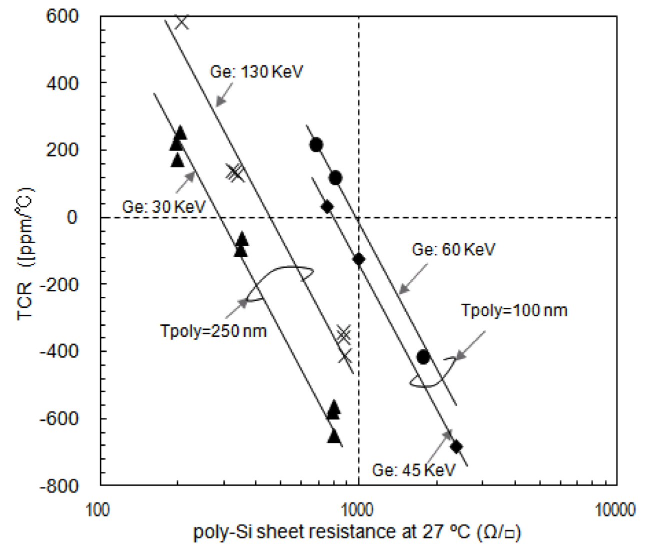

Fig. 7. Relationship between TCR and sheet resistance of high-resistance poly-Si resistor with implanted Ge (5×10^{14} cm^{-2}).

Commonization is used to disturb the optimized process module and change the characteristics. The divide-into-dependent-blocks process flow must therefore be retained to realize maximum device performance.

III. Low Thermal Budget Process for Forming HBTs

The BJT formation process is inserted into the CMOS process as a module, and there are various ways to insert the BJT module. Impurity diffusion from heavily doped source/drain (S/D) regions during BJT block processing was adjustable until the 0.25 μm generation. Expanding the MOSFET SW length and adjusting the impurity profile of the halo regions suppress the short channel effects, so the SiGe HBT module can be integrated into the base CMOS process after MOS formation [9], [12], [16]. However, things became more difficult from the 0.18 μm generation. First, the tight metal pitch does not allow expansion of the SW length, as shown in Fig. 6. Second, boron diffusion from the heavily boron-doped area of the PMOS is especially problematic compared to the arsenic or phosphorus diffusion from an NMOSFET, and the heavily

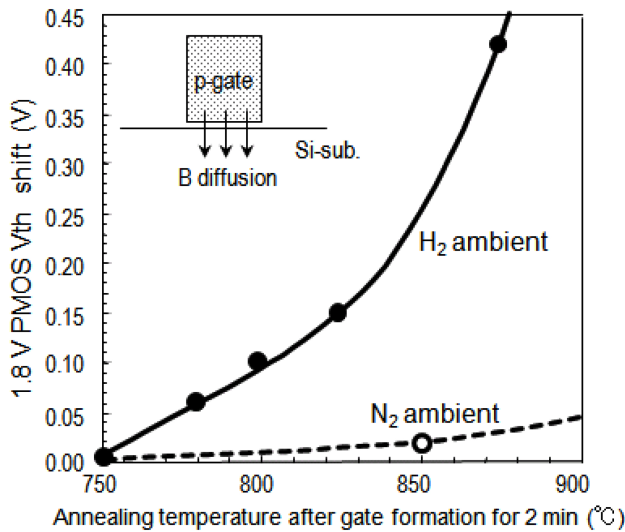

Fig. 8. PMOS Vth shift due to H_2 bake prior to SiGe epitaxial growth. Gate oxide thickness was 3.5 nm for 0.18 μm CMOS. Gate length of PMOS was set to 2 μm to evaluate degree of boron penetration.

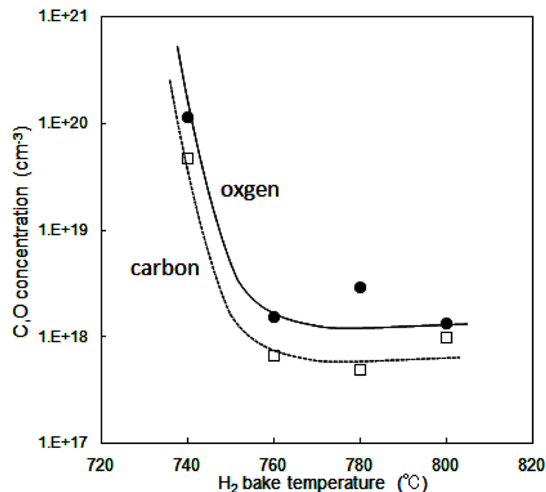

Fig. 9. SIMS-measured C and O concentrations on surface between SiGe epitaxial growth layer and Si substrate.

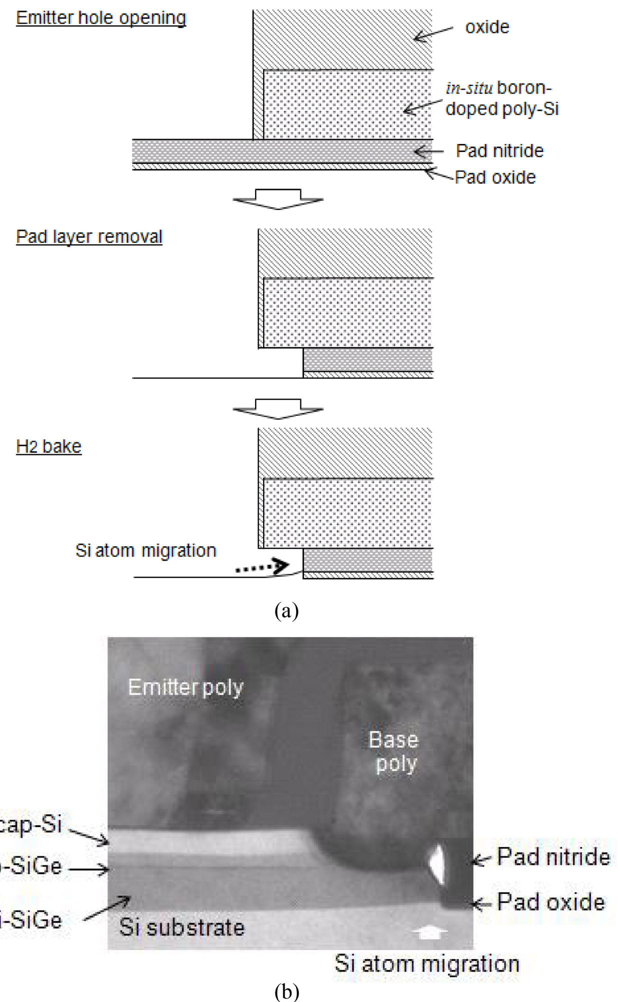

Fig. 10. Si/SiGe epitaxial growth in base contact cavity. (a) Cross-section of epitaxial growth layers; (b) TEM cross-sectional view of base region of SiGe HBT. H_2 bake temperature prior to epitaxial growth was 875 °C.

doped p-type S/D regions extended by the thermal budget of the bipolar process increase the short channel effect. The doping levels for the extensions and halo regions are lower than that for the S/D regions, so the effect of the SiGe HBT module on the extension regions is small. To avoid this second problem, the SiGe HBT formation module was inserted after patterning of the MOS gate and before S/D implantation, starting with the 0.18 μm generation, as shown in Fig. 3 [19], [20], [22].

The thermal budget for SiGe HBT formation is mainly used for H_2 bake prior to SiGe epitaxial growth. From the viewpoint of MOS device characteristics, the H_2 bake temperature must be below 800 °C to suppress threshold voltage (V_{TH}) shift due to the H_2 bake. Hydrogen atoms during annealing promote boron diffusion throughout the gate oxide layer and enhance the V_{TH} shifting of the P-gate PMOS much more than N_2 annealing, as shown in Fig. 8. The N-gate PMOS, commonly used until the 0.25 μm generation, is not affected by this problem. In contrast, the P-gate PMOS, commonly used from the 0.18 μm generation, is affected by boron penetration through the gate oxide during the H_2 bake. This problem can be avoided by placing the BJT fabrication process after source/drain/gate (S/D/G) NMOS implantation and before S/D/G PMOS implantation [15]. Because impurities are spontaneously implanted into the MOS gate and S/D regions, there is no boron inside the P-gate during the H_2 bake. However, a final spike annealing at 1000 °C alone could be insufficient to make the boron diffuse in the P-gate poly-Si in the case of spontaneous S/D/G implantation. This would induce the formation of a thick depletion layer in the P-gate and thereby degrade PMOS performance.

An intrinsic base region is selectively formed at an open emitter hole using a conventional single-wafer LP-CVD technique [19], [20], [22]. An H2 bake is used to eliminate surface contamination (C, O, etc.) prior to SiGe epitaxial growth. For conventional blanket Si epitaxial growth for a collector region, a 10-minute H2 bake at 1040 °C is used for surface cleaning. This condition is not appropriate for intrinsic base regions. An 800 °C H_2 bake is sufficient to

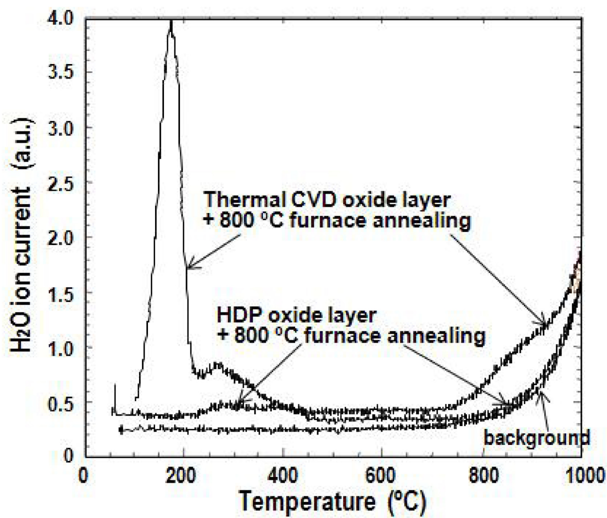

Fig. 11. Thermal desorption spectrum of thermally stimulated moisture from oxide layers.

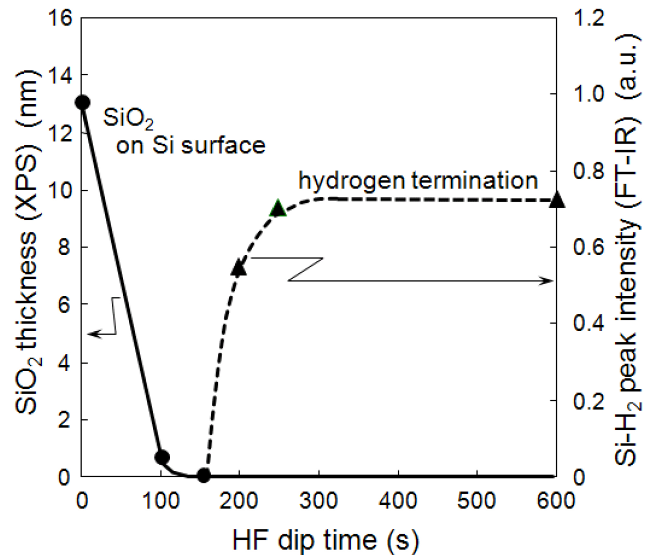

Fig. 12. Oxide layer thickness and H termination dependencies on HF dip time. Thickness of thin oxide layer was measured by x-ray photoelectron spectroscopy (XPS); amount of H termination was measured by Fourier transform infrared spectroscopy (FT-IR). Si-H_2 intensity was measured because two dangling bonds are on Si(100) surface.

remove the natural oxide layer. Fig. 9 shows the measured C and O concentrations after the H_2 bake and Si/SiGe epitaxial growth. The concentrations were measured on a bare Si wafer by secondary ion mass spectrometry (SIMS). A 760 °C H_2 bake was sufficient to remove the C and O from the Si surface. Hydrogen termination, which forms during wet etching in HF dip, prevents natural oxide growth on a Si surface [37].

After an emitter hole is opened on the pad SiN layer, the SiN layer and pad SiO_2 layer are removed by wet etching, as shown in Fig. 10(a). A TEM cross-sectional view of the base region (Fig. 10(b)) shows that the Si migrated during H_2 bake at 875 °C. This indicates that the thin natural oxide is removed by baking at 875 °C. Even at 800 °C, slight Si migration was observed, and a clean Si surface was obtained.

Two things must be done in order to finish epitaxial growth with a low-temperature H_2 bake. One is suppressing the effect of the wafer. Fig. 11 shows the measured moisture emission from the oxide layers. A thermal CVD oxide layer, which was deposited at 680 °C, tended to absorb moisture in the atmospheric environment and to desorb a great deal at 170 °C, resulting in the formation of a thin thermal oxide layer. An 800 °C H_2 bake was not sufficient to remove this layer. Since the quality of HDP oxide is close to that of thermal oxide, a slight amount of moisture emission from the HDP layer was observed, as shown in Fig. 11.

The second thing that needs to be done is optimizing the HF dip time. Formation of hydrogen termination on a silicon surface takes time after removal of the surface pad oxide, as shown in Fig. 12. A 300 s HF dipping process creates hydrogen termination with Si bonds on the Si surface, which prevents the formation of natural oxide. In addition, a pad oxide layer is formed by USG oxide under low-pressure conditions, resulting in quality close to that of thermal oxide. Low thermal budget BJT fabrication using these techniques achieves a high bipolar transistor yield (99.99993 %) and maintains 0.13 μm and 0.18 μm CMOS performance with little process condition tuning [19], [20], [22].

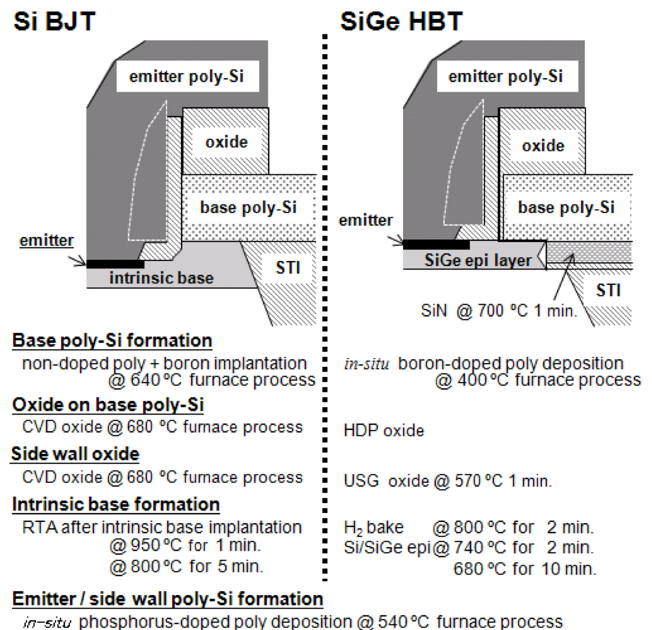

Fig. 13. Comparison of thermal budgets needed to form Si BJT described elsewhere [13] and SiGe HBT.

An intrinsic base region for a 40 GHz f_T Si BJT was formed by N_2 annealing at 950 °C for 1 minute and wet oxidation (pyrogenic) at 800 °C for 5 minutes [13]. The N_2 annealing recrystallized the damaged Si surface immediately after BF_2 low-acceleration implantation, and the segregation by wet oxidation fixed the surface boron profile, which reduced the emitter-base leakage current. It may be possible to reduce the annealing time to recrystallize, but the oxidation time cannot be reduced because lengthy oxidation is needed to suppress the peak boron concentration at the Si surface. The process temperature during the intrinsic SiGe epitaxial growth

for 10 minutes is 670 °C, and that during cap-Si growth for 2 minutes is 740 °C. The heavy Ge concentration enhances the SiGe growth rate, so the thermal budget for the SiGe growth step is lower than that for the 800 °C H_2 bake.

The other thermal processes in the SiGe HBT process were adjusted to reduce the thermal budget, as shown in Fig. 13. The thermal budget for the SiGe process is lower than that for the conventional intrinsic base formation. A double-digit difference in the impurity diffusion coefficients at 800 °C and 700 °C is equivalent to a single-digit difference in the diffusion time at both temperatures [38]. However, a furnace process usually takes hours, so using the HDP process instead of the thermal CVD oxide process effectively reduces the total thermal budget during HBT formation. Since the SiGe HBT technology is more flexible than the Si BJT technology for adjusting the CMOS process, the SiGe HBT technology must be used instead of the Si BJT technology to integrate advanced CMOS. Low-thermal-budget SiGe HBT process technology has been demonstrated to be applicable from the 0.18 μm generation to the 90 nm and 0.13 μm generations [19], [20], [22].

IV. Conclusion

Use of a divide-into-dependent-blocks process flow and a low-thermal-budget bipolar process enable construction of a flexible 0.18 μm BiCMOS technology that can be applied without major change to CMOS process conditions. A minimal-moisture-desorption oxide process is used to reduce the H_2 bake temperature to 800 °C, resulting in a bipolar transistor yield of 99.99993 %. The height of a bipolar device was reduced to enable application to both 0.18 μm and 0.15 μm CMOS technologies. Full optimization throughout the series of BiCMOS technologies is needed to reduce the total cost of device development, reliability testing, and PDK preparation. The proposed technology can also be applied to the 0.13 μm generation.

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