A Study on Suppressing Crosstalk Through a Thick SOI Substrate and Deep Trench Isolation

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***Abstract*—Measurement and simulation studies are conducted on transmission crosstalk in thick silicon-on-insulator substrates. This paper focuses on the role of buried oxide layers and deep trench isolation in suppressing crosstalk. With radio frequency coupling paths on substrates depending on noise frequency, a deep trench guides noise signals to substrates and suppresses transmission crosstalk between input and output ports. Good agreement is obtained between electromagnetic field (EM) simulation and measurement results. The EM simulation results suggest different approaches might be used in designing deep trench isolation patterns for a middle resistivity (MR) substrate and a high resistivity (HR) substrate. Deep trench isolation plays a more important role in HR substrates than in MR substrates.**

***Index Terms*—Deep trench isolation, electromagnetic field simulator, silicon-on-insulator technology, transmission crosstalk.**

I. Introduction

BOTH THIN and thick silicon-on-insulator (SOI) substrates have been widely used for semiconductor products [1]–[11]. The bonded Si layer thickness of thin SOI substrates is around 0.1 μm, and that of thick SOI substrates is over 1 μm. Thin SOI substrates improve MOS device performance by suppressing short channel effects and reducing parasitic substrate capacitance [1], [2]. Thick SOI substrates do not directly enhance device performance as thin SOI substrates do, because impurity-diffused well layers are formed on thick SOI substrates in the same way as they are on conventional bulk Si CMOS substrates. However, combining thick SOI substrates with deep trench isolation makes it possible to achieve completely latchup-free CMOS circuit configuration [3]. Since even small noises can affect RF circuit performance, substrate noise transmission should be avoided for maintaining circuit stability. For instance, capacitors or resistors are added to suppress sensitivity to soft errors induced by α particles from space. However, such additions could degrade the circuit operation speed [5]. The buried oxide layer of the thick SOI substrates would protect the devices from the intrusion of noise carriers without degrading circuit performance. Thick SOI substrates also maintain high reliability of high-voltage switching ICs by blocking large surge noises under severe conditions [9], [10].

Substrate crosstalk is determined by various parameters, such as isolation structure and the kinds of substrate materials [12]–[19]. Many studies have previously been published on making guidelines for achieving optimized layout design, but they have treated only the simple substrate structure of a bulk Si wafer or thin SOI substrate. Devices with a thin SOI substrate are surrounded by a buried oxide layer, and crosstalk noises travel in the Si substrate under the buried oxide layer. On the other hand, the bonded layer of a thick SOI substrate should be treated as another crosstalk path candidate. This paper focuses on suppressing transmission crosstalk through bonded Si layer and narrow deep trench isolation technologies that will be discussed. Devices are surrounded by narrow deep isolation trenches in a bonded Si layer to block DC current. However, AC current may pass through the deep trench isolation structure due to capacitive coupling.

This paper reports our use of a three-dimensional (3-D) planar electromagnetic field (EM) ADS Momentum simulator [20] to simulate crosstalk. Crosstalk simulation results calculated by a two-dimensional (2-D) MEDICI device simulator and a 3-D daVinci simulator have previously been reported [12], [16], [21]. Because ADS Momentum has layers with only dielectric and resistive parameters, it cannot include the effects of a depletion layer tracing a real impurity profile. However, ADS Momentum is clearly advantageous for device simulation because it has close affinity with circuit simulation and its EM simulation results can be directly used in circuit designs. ADS Momentum has been widely used by many analog circuit designers, and it is advantageous for designers who do not own a device simulator to be able to simulate the effects of crosstalk in their designs. The results we obtained with this simulator indicated good agreement with measurements, and this work showed deep trench isolation could effectively suppress crosstalk on transmission lines.

The remainder of this paper is organized as follows. Section II introduces the technologies used in this work. On the basis of measurement results obtained in investigating crosstalk noise, Section III compares measured crosstalk characteristics among different wafer materials and different deep trench configurations, giving a good overview for a combination of a thick SOI substrate and deep trench isolation. Section IV presents simulation results based on experimental

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results to discuss crosstalk noise reduction. Section V concludes the paper with a summary of key points.

II. Substrate Configuration and Test Structure

Test structures were formed with the 0.25-μm SiGe-BiCMOS process in a 200-mm fabrication process line [7]. Buried n^+ doped layers, which electrically connect with a substrate, were used as the sinker layers of the collectors of NPN transistors. In the sinker layers, Sb ions of 2×10^{15} cm^{-2} and phosphorus ions of 5×10^{15} cm^{-2} were implanted. Since Sb ions were diffused by one-hour annealing at 1200 °C, the bottom of the sinker layer reaches the buried oxide layer. Si epitaxial growth of 0.35-μm thickness was performed between the Sb implantation and phosphorus implantation processing steps. The sheet resistance of the Sb diffused layer and the phosphorus diffused layer are 38 Ω/□ and 20 Ω/□, respectively. The cross section of a typical configuration using a bonded SOI substrate is shown in Fig. 1(a). The bonded Si layer of the SOI wafer has the same resistivity of 10 Ω· cm (ordinary doping of n-type is 4×10^{14} cm^{-3}) as that of an ordinary bulk Si wafer to form MOS and bipolar transistors, but the p-substrate has relatively high resistivity of 40 Ω · cm (p–type impurity concentration is 3×10^{14} cm^{-3}) to achieve better signal propagation performance. The thicknesses of the bonded Si layer and the buried oxide layer are 1.5 μm and 0.5 μm, respectively. After formation of 0.35-μm-thick shallow trenches, deep trenches are separately formed [6]. A 30-nm-thick pad oxide was formed at 1000 °C for before deposition of high density plasma (HDP) oxide for the shallow trenches, and a 4-nm-thick pad oxide was formed at 750 °C before filling the deep trenches by thermal oxide deposition at 800 °C. Both deposited oxide layers were densified at 950 °C for 30 minutes. Double deep trench isolation surrounding the sinker layers in Fig. 1(b) was also investigated to further suppress transmission crosstalk. The Si island sandwiched by two trenches is electrically floating, so it does not work as a grounded shield.

$TiSi_2$ salicide was formed on diffusion layers to achieve sheet resistance of 3.5 Ω/□. A 1.2-μm-thick oxide layer was formed under the first metallization layer. The basic concept of this technology is that deep trench isolation performs DC blocking even without a channel stopper [15], so channel stopper layers were not formed under the shallow trench isolation in this investigation. The thickness of the 200-mm Si wafers is 725 μm. Because the backside of the wafers is covered by a thermally deposited oxide layer of 1.0-μm thickness, the backside was electrically floating during measurements.

Fig. 2 shows the top view of our test structure, which is the same as the test structures reported in [12] and [15]–[18]. Two 50 μm × 50 μm n^+ buried layers, which were used as a noise source and sensor, were surrounded by deep isolation trenches. The two n^+ doped layer contacts were separated by distances ranging from 10 μm to 100 μm. On-wafer two-port measurements were taken using two ground-signal-ground (GSG) microwave probes. We used an HP8510C vector network analyzer for the high frequency range from 100 MHz to 40.1 GHz and an HP4194 gain-phase analyzer for the low frequency range under 100 MHz. The measurement system

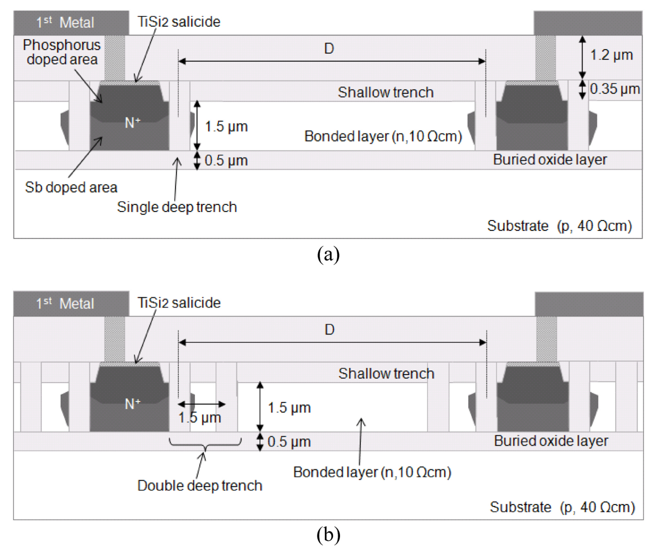

Fig. 1. Schematic cross section of test structures to measure the substrate coupling between two sinker layers on the thick SOI substrate, featuring (a) single deep trench isolation structure and (b) double deep trench isolation structure.

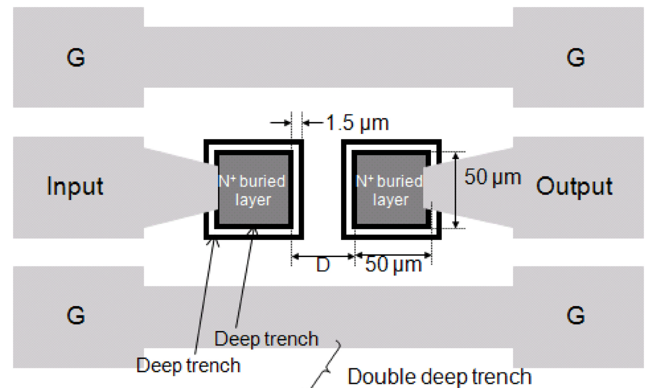

Fig. 2. Top view of test structure for crosstalk analysis. The structure has the double deep trench configuration shown in Fig. 1(b); the metallization pattern and sinker layer size are the same as those for the test pattern with single deep trench isolation structure.

was calibrated by using the impedance standard substrate (ISS) of Cascade Microtech. We did not perform open calibration using an on-wafer pattern that does not make contact between the metallization pattern and the buried layers, because we assumed it would overestimate the effects of the pad capacitance at high frequency.

III. Experimental Results

A. Effects of Deep Trench Isolation on SOI Substrate

The measurement results indicated deep trench isolation can reduce transmission crosstalk flowing in the bonded Si layer as shown in Fig. 3. Applying deep trench isolation changed the nearly flat frequency characteristics to full frequency dependency characteristics. For the case without deep trench isolation, extending the distance D from 10 μm to 100 μm reduced the coupling by 20 dB at 10 MHz. This means that a strong resistive coupling path determines the amount of transmission crosstalk when there is no deep trench isolation.

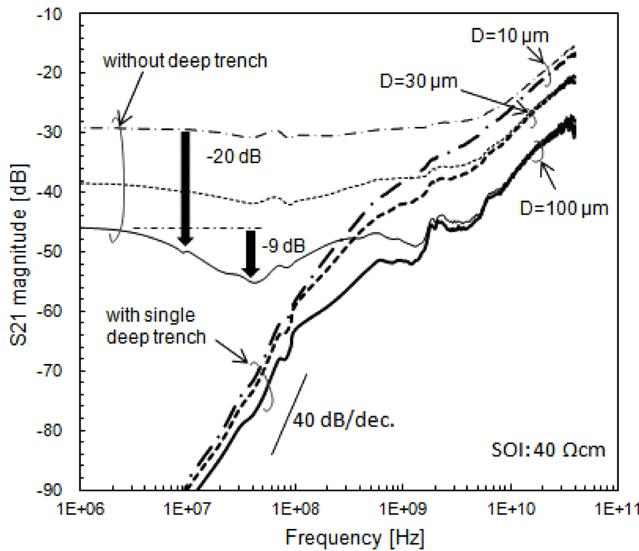

Fig. 3. Crosstalk measurement results on the thick SOI substrate with and without single deep trench isolation structure to divide DC current from input to output.

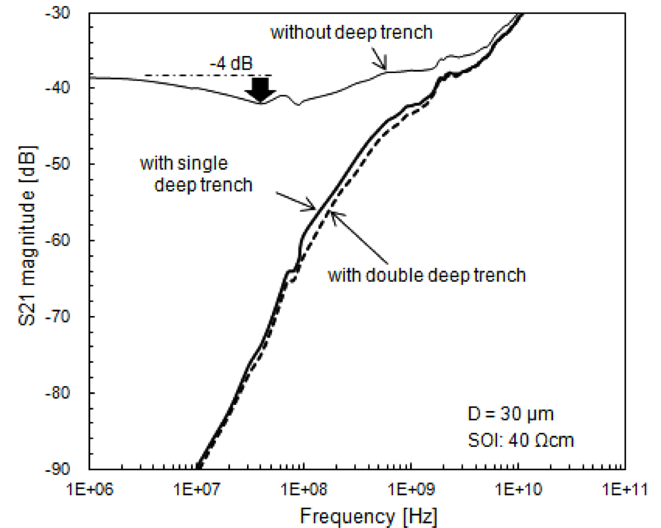

Fig. 4. Crosstalk measurement results on the thick SOI substrate with no/single/ double deep trench isolation structure. The distance D between two ports is 30 μm.

On the other hand, the deep trench isolation effectively suppresses crosstalk at the low frequency range of less than 2 GHz. The deep trench guides the crosstalk noise downward into the substrate in this frequency range, and capacitive coupling through the buried oxide layer determines the amount of transmission crosstalk. The thickness of the buried oxide layer and the width of the deep trench isolation structure are the same 0.5 μm, but the 50 μm $\times$ 50 μm size of the n$^+$ sinker area is about eight times that of the deep trench surrounding the sinker region. The initial slope of 40 dB/decade [12] indicates capacitive coupling through the buried oxide layer with a bonded Si layer. Stronger capacitive connection between substrate and sinker layer determines crosstalk characteristics in the low frequency range under 100 MHz. Transmission crosstalk for the configuration with deep trench isolation mainly flows in the 40 $\Omega\cdot$cm substrate, and double deep trench isolation was not effective for this case as shown in Fig. 4. Consequently, the effectiveness of double deep trench isolation was observed to be low from 100 MHz to 1 GHz.

Under all wafer and configuration conditions, the scattering parameter S21 starts to rise with slope of 20 dB/decade at frequency above 5 GHz. Above this frequency, the buried oxide becomes transparent and it no longer makes any difference whether trench isolation is applied.

For the configuration without deep trench isolation, transmission crosstalk mainly flows inside the bonded layer. However, small capacitive coupling with the substrate through the buried oxide can be observed. For distance D of 30 μm the S21 parameter dropped 4 dB, and for D of 100 μm it dropped 9 dB as shown in Figs. 3 and 4. The small capacitive coupling can make part of the crosstalk noise travel vertically downward into the 40-$\Omega\cdot$cm resistive substrate even without being guided by deep isolation trenches.

B. Effects of Substrate Resistivity

High resistivity (HR) substrates have been attracting wide attention among RF circuit designers [23]–[24] because they can suppress crosstalk noises [12]. When we replaced a low (40-$\Omega\cdot$cm) resistivity substrate with an HR (1-k$\Omega\cdot$cm) substrate, the resistivity of a bonded Si layer on the HR substrate was the same 10 $\Omega\cdot$cm as that for the bonded Si layer on the 40-$\Omega\cdot$cm substrate in Fig. 1. The 40-$\Omega\cdot$cm substrate is called a middle resistivity (MR) substrate in this paper. Since the HR substrate's impurity concentration is a very low 1×10^{13} cm^{-3}, the substrate's resistivity might fluctuate easily. Wafer vendor specifications guarantee at least 1-k$\Omega\cdot$cm resistivity. Thermal donor generation could be a parameter that induces fluctuation in HR substrate resistivity during the processing steps due to oxygen precipitation [25], [26]. Ref. [26] suggests that 1000 °C furnace annealing to form diffusion layers of devices could suppress new donor generation at relatively low temperature annealing of 450 °C during metallization formation [26], so the final resistivity of the HR substrate should maintain the initial 1 k$\Omega\cdot$cm during all of the processing steps.

Fig. 5 shows the crosstalk characteristics measured on the HR substrate. It indicates that for this substrate also the deep trench isolation was able to reduce crosstalk isolation. It also shows the wider advantage to a double deep trench structure in the range from 100 MHz to 1 GHz, compared with the Fig. 4 case. The reason for this result is that downward noise current decreases at the HR substrate more than at the MR substrate. This reduction of the downward noise can be seen also in the result for configuration without deep trench isolation. The reduction width in S21 was only 2 dB, and the S21 reduction point of the no-deep-trench structure for the HR substrate changes to a higher frequency than the 40 MHz for the MR substrate.

The transmission crosstalk in a bulk Si wafer was also investigated. The substrate resistivity and the depth of the deep trench isolation structure are 10 $\Omega\cdot$cm and 2.5 μm, respectively (Fig. 6). Because the type of doping for the bulk Si is different from that for the n$^+$ buried diffusion region, a depletion region spreads under the buried n$^+$ layer [27] and

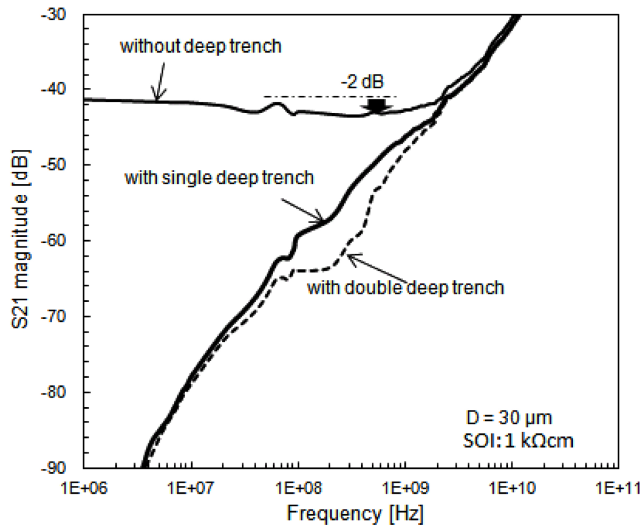

Fig. 5. Comparison of crosstalk performance measured on the thick HR SOI substrate for the no/single/double deep trench isolation structures. The distance D between buried N^+ layers is 30 μm.

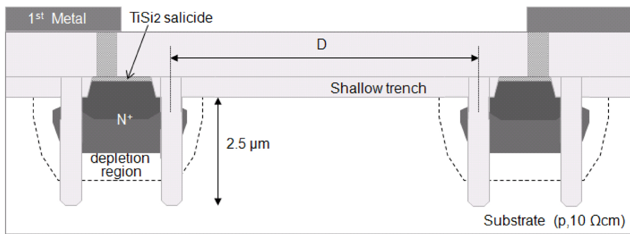

Fig. 6. Schematic cross section of a configuration to measure the bulk substrate coupling.

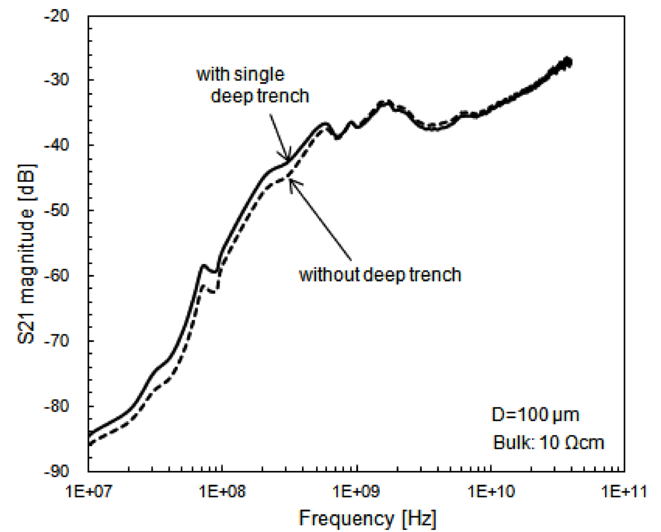

Fig. 7. Comparison of crosstalk performance measured on the bulk substrate for no/single deep trench isolation structure between buried layers.

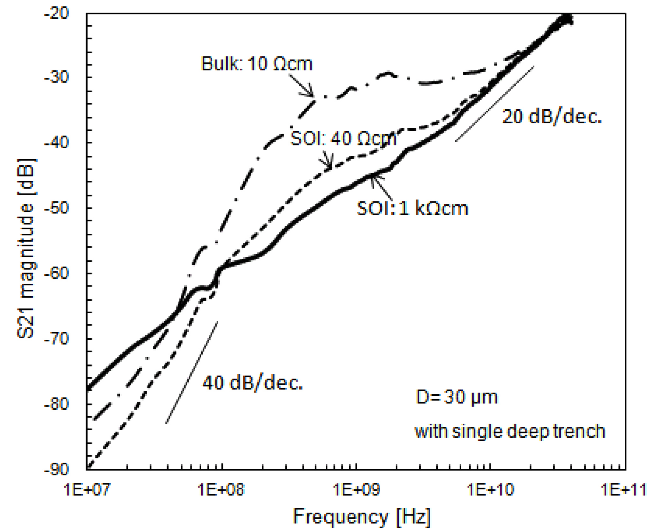

Fig. 8. Comparison of measured crosstalk characteristics with single deep trench isolation structure among bulk substrate, thick 40-$\Omega \cdot$cm SOI, and thick HR SOI wafer.

capacitive coupling through the depletion region produces the frequency dependency shown in Fig. 7. Deep trench isolation did not reduce transmission crosstalk for the bulk wafer case; this means that the addition of deep trenches extended the distance between the two ports by only 5 μm. It is assumed the small difference in crosstalk characteristics among the different configurations is due to the different depletion region widths caused by deep trench isolation.

Fig. 8 compares measured crosstalk characteristics measured on the Si substrates with different resistivity. A plateau can be observed between the 20 dB/decade slope for the higher frequency range and the 40 dB/decade slope for the lower frequency range. The coupling with the substrate through the buried oxide or depletion region leads to a plateau in the mid-frequency range from 100 MHz to 10 GHz, and the effect of increasing the substrate resistivity is to lower the plateau [12]. Transmission crosstalk was effectively suppressed when increasing the resistivity from 10 $\Omega \cdot$cm to 40 $\Omega \cdot$cm, but increasing it from 40 $\Omega \cdot$cm to 1 k$\Omega \cdot$cm showed little effect. First of all, it could be thought that a single deep trench is not enough to suppress noise current flow in a bonded layer. Additionally, the substrate's high resistivity characteristics might be negatively affected by the parasitic surface conduction underneath the buried oxide layer [28], [29]. Even though the composition surface of the bonded SOI wafer is between the buried oxide layer and a high resistivity Si substrate, we thought that high temperature annealing at 1200 °C during the fabrication process should eliminate the fixed oxide charge Q_{ox} at the SiO_2/Si interface. However, the low-frequency slope of S21, which experiment results showed was close to 20 dB/decade, suggests the existence of Q_{ox}.

IV. Simulation and Optimized Design

The number of trial-and-error methods is very limited, but simulation is a very useful one for reaching an optimized layout. The simulation pattern described in this paper (Fig. 9) does not include a metallization layer to avoid the effects of parasitic capacitance between substrate and metallization layer. The simulation area includes a Si layer that has a 50 μm distance between its boundary and the edge of a buried doped layer surrounded by a deep-trench, fully filled oxide layer. If this distance is too short, reflection waves

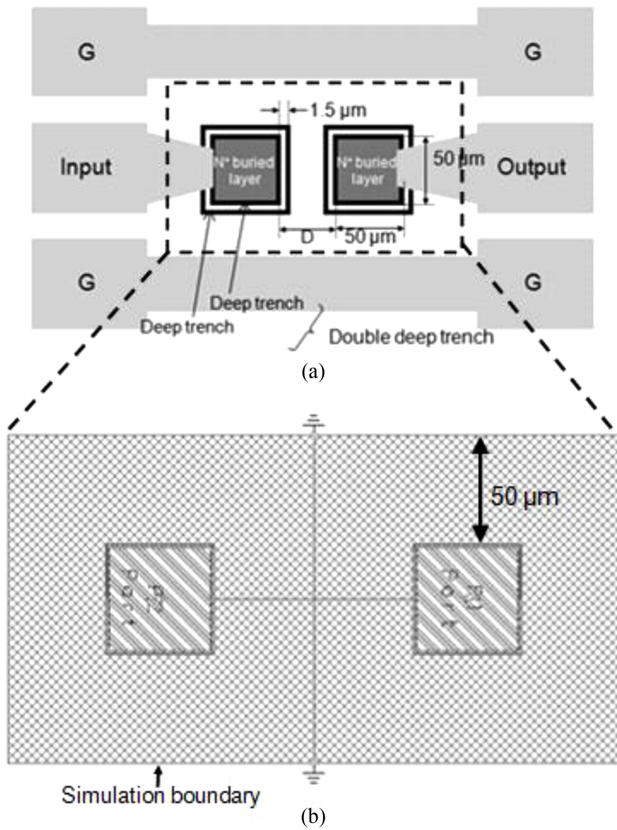

Fig. 9. Pattern of ADS Momentum Visualization on the screen. Measurement layout (a) includes a metallization layer, but the simulation pattern for ADS Momentum (b) includes only Si and SiO_2 layers.

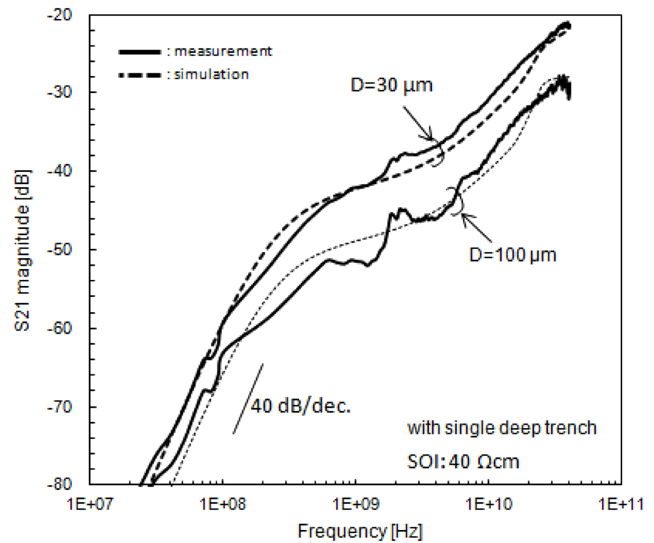

Fig. 10. Comparison of measurement and EM simulation results for the MR substrate with single deep trench isolation.

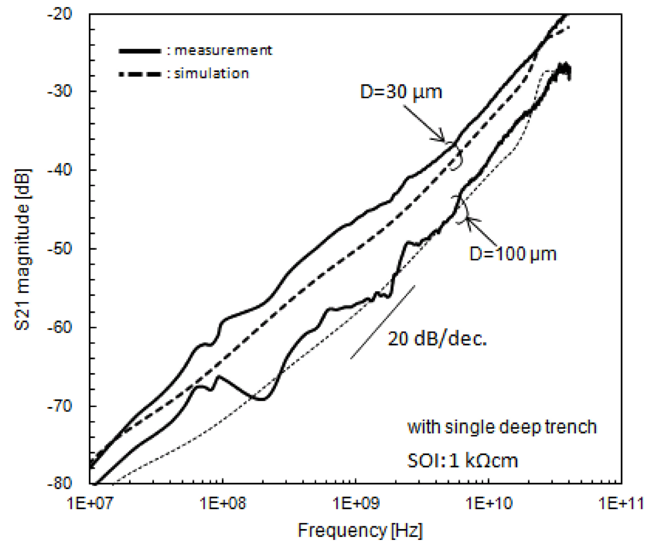

Fig. 11. Comparison of measurement and EM simulation results for the HR substrate with single deep trench isolation.

from the simulation boundary will appear in the simulation results. The 50-μm distance is long enough to avoid this effect. The substrate is absolutely grounded during simulation, although its backside was floating during the measurements. Fig. 10 shows good agreement between measurement and EM simulation results for the 40-$\Omega \cdot$cm SOI substrate. The slope of 40 dB/decade around 100 MHz obtained in the EM simulation is in good agreement with the device simulation and theoretical approach in [12]. On the other hand, the EM simulation for the 1-k$\Omega \cdot$cm SOI substrate shows a little bit lower transmission characteristics than measurement results (Fig. 11). This comparison also suggests high resistivity of the HR substrate was a little lowered during the fabrication process.

An optimized layout design leads to less transmission crosstalk, and it could be said that more accurate simulation is critical to achieving sophisticated RF circuit design. Fig. 3 shows that extending the distance from the noise source at low frequency was not effective, but reducing the circuit area size of the noise source can be expected to suppress the amount of transmission crosstalk. Through the EM simulation we were able to calculate the degree to which noise could be suppressed by reducing the circuit area size. Fig. 12 shows simulation results for the deep trench isolation dependency as one example of crosstalk noise suppression. They indicate that the isolation effect of multiple deep trenches is small for the 40-$\Omega \cdot$ cm SOI substrate and significant for the HR SOI substrate. This is the same tendency as that shown in Figs. 4 and 5. For the MR substrate, a single deep trench isolation structure is enough to suppress the transaction crosstalk noise. For the HR substrate, a multiple deep trench configuration suppresses the transmission crosstalk in the frequency range from 10 MHz to 1 GHz. We therefore consider that implementing deep trench isolation as much as possible will be effective in the case of using an HR substrate.

In our work, the sinker layer of an NPN transistor was chosen as the buried diffused layer. It was confirmed by ADS Momentum that a resistivity change in a buried doped layer does not significantly affect transmission simulation results. Even replacing the N-well layer of a P-MOS transistor with the sinker layer of an NPN transistor did not change the simulation results. The ordinary P-well layer of an N-MOS

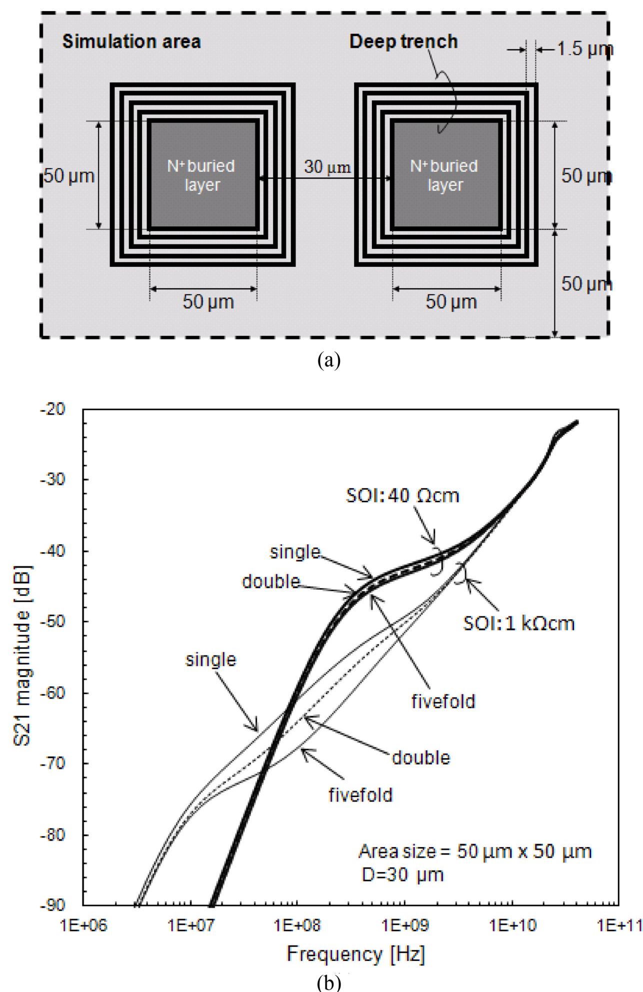

Fig. 12. EM simulation of deep trench and substrate resistivity dependency of crosstalk noise. (a) Schematic view of installed layout. (b) Simulation results.

transistor and the N-well of a P-MOS transistor both have sheet resistance of around 1 kΩ/□, and it should be expected that a depletion layer will be formed in such level doped layers. However, ADS Momentum cannot handle the parasitic capacitance in a depletion layer since it would change the amount of transmission crosstalk.

V. Conclusion

Trench isolation was confirmed to effectively suppress transmission crosstalk passing through the bonded Si layer on a thick silicon-on-insulator (SOI) substrate. However, the effectiveness of a multiple trench structure was found to be limited to the case of using a middle resistivity substrate for the thick substrate. The same good agreement was obtained between electromagnetic field (EM) simulation results and measurement results as that obtained with device simulators. It was determined that because the direction of crosstalk noise transmission depends on frequency, it is necessary to optimize layouts in accordance with the frequency being used. Simulation results suggest that implementing deep trench isolation as much as possible will be effective for the case of using a high resistivity (HR) substrate.

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