A Technique to Improve the Performance of an NPN HBT on Thin-Film SOI

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***Abstract*—The performance of an npn SiGe HBT on thin-film silicon on insulator (SOI) is investigated using 2-D numerical simulation. A technique of using N+ buried layer has been presented to improve the performance of an SiGe HBT on thin-film SOI. The tradeoff in the performance of HBT has been observed and the results are compared to the standard SOI HBT. The HBT offers better βV_A product at high collector currents. A 341 GHzV of $f_t BV_{CEO}$ product can be obtained by using this technique. The scalability of film thickness is applied and the enhancement in the speed is observed. The self-heating performance of the proposed HBT is studied and the BOX thickness has been scaled to improve the thermal performance. The maximum lattice temperature is obtained. The proposed HBT is suitable for RF applications and can be used in addition to the existing 130 nm SOI CMOS technology for better performance.**

***Index Terms*—Self-heating, Sentaurus, SiGe HBT, silicon on insulator (SOI), thin BOX.**

I. Introduction

PROCESS integration of npn SiGe HBTs, CMOS, and high-quality passive devices on thin-film SOI have been the active area of research in past two decades. The very large scale integration of high-performance HBTs and low-power CMOS has made the BiCMOS technology popular in electronics industry. The details on HBT can be found from [1]–[5]. The continuous improvement of device performance and high level of HBT integration with MOSFETs has made single-chip solutions realizable for several wire-line and wireless products. Details of some recent commercial BiCMOS technologies are given in [6]–[10]. The use of these technologies motivated designers to create new products in the emerging area like chipsets for 3G/4G cellular applications, automotive radar, imaging, and high data rate communication systems. Transceivers [11]–[14] using SiGe BiCMOS technology have been reported with promising performance for high-end commercial applications. The popularity of silicon on insulator (SOI) for low-power and high-speed digital system design motivated researchers to integrate npn HBTs with MOSFETs on SOI platform to offer npn only SOI BiCMOS technology that can be used for high-performance system-on-chip applications. The integration of SiGe HBT compatible with SOI CMOS is reported in [15]–[17].

Recently, a 0.25 μm SiGe-CBiCMOS technology on thick-film SOI was reported [18].

It has been observed that the performance of SOI CMOS is better at $T_{si} = L_g/3$ [19]. So, when the technology node shrinks, the film thickness needs to be reduced for SOI CMOS. To keep this in mind, the performance of the SOI HBT also needs improvement at low film thickness to offer advanced SOI BiCMOS technology. However, the SiGe HBT on thin-film SOI has poor performance due to high collector resistance of HBT and low driving strength. The high collector resistance is due to limited volume of Si collector and low driving strength is due to the self-heating of the transistor. The temperature rise in the HBT increases the collector current. When lattice temperature becomes very high, the thermal runaway occurs. As the self-heating is very critical for analog/RF applications, it is important to improve the performance of SOI HBT at low power. Therefore, it is of interest to study the self-heating effect of HBT and mechanisms are necessary to reduce this effect. The thin epilayers have been proven as the candidate to reduce the self-heating effect. However, thin base and thin collector in the HBT increase the resistance. To compensate for the increase in the resistance, doping of the layers need to be increased. The higher doping increases the electric field and causes the temperature rise in the junction. The self-heating effect of SiGe HBT on SOI is studied in [20] and [21]. Recently, in SOI CMOS technologies, thin BOX has been proposed to reduce the short-channel effects and the self-heating effects [22], [23]. Therefore, SOI BiCMOS technology with thin BOX could be a promising technology for analog/RF applications.

In this paper, a technique is adopted to improve the HBT performance at low supply voltage. The proposed HBT has a thin n+ buried layer in the collector region. The 2-D numerical simulations in Sentaurus device simulator [24] have been performed to obtain the characteristics of npn SiGe HBT on thin-film SOI. In Section II, the improvement in βV_A and $f_t BV_{CEO}$ product is reported for the proposed HBT. The self-heating performance of the new device is studied and compared with the standard HBT. The BOX thickness has been scaled to study the self-heating performance of the HBT and the maximum lattice temperature has been obtained in Section III. Subsequently, conclusion is given in Section IV.

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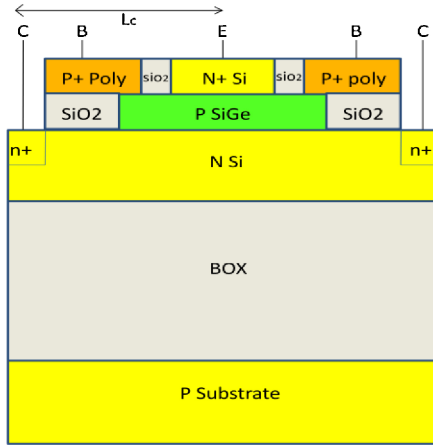

Fig. 1. Schematic of the npn SiGe HBT on thin SOI.

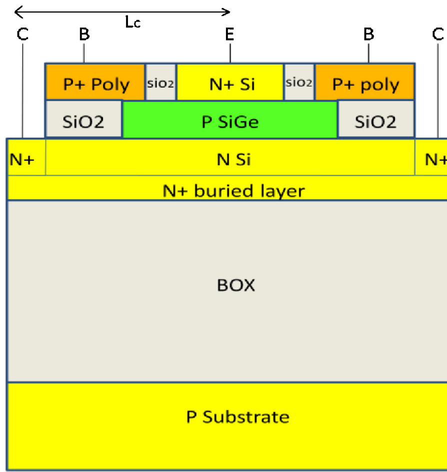

Fig. 2. Schematic of the npn SOI HBT with N+ buried layer (120 nm N Si and 40 nm N+ buried layer).

II. npn HBT on Thin-Film SOI

The schematic of a standard npn SOI HBT and the proposed SOI HBT with emitter area $0.15 \times 1.0\,\mu\text{m}^2$ are shown in Figs. 1 and 2, respectively. The parameters used for the npn HBT are mentioned in Table I. The details of the npn SOI HBT and its fabrication flow can be found in [25]. The simulation results of the HBT (in Fig. 1) agree closely with the experimental result obtained in [25]. The results of the proposed HBT (in Fig. 2) are compared with the HBT shown in Fig. 1. The fabrication flow for the proposed HBT is as follows. An SOI substrate is taken with 40 nm film thickness and 400 nm BOX thickness. The film is implanted with $5\text{E}^{19}\,\text{cm}^{-3}$ doping in the area where HBT is to be fabricated. Then, 120 nm of N-type silicon is deposited with $7.5\text{E}^{17}\,\text{cm}^{-3}$ doping. The rest of the HBT fabrication procedure can be used as given in [25]. The Ge profile was varied from 10% to 25% in the base layer. A 40 nm of emitter base spacer was used to isolate the emitter and extrinsic base. The HBT profiles have been obtained by process simulations from Sentaurus process simulator [26]. The base profile broadens in the HBT with 40 nm buried layer as shown in Fig. 3. The electrons injected from emitter are transported vertically to base–collector junction and subsequently the carriers travel laterally to the collector contact. In the device simulation, Philips unified mobility model [27], [28] is chosen due to separately modeling capability of majority and minority carrier mobility. Shockley–Read–Hall recombination with concentration dependent lifetimes is specified.

The material parameter Shockley–Read–Hall electron and hole lifetimes for SiGe were 3×10^{-6} and 1×10^{-6} s,

TABLE I
SiGe HBT Parameters

Parameter	Values	units
Emitter thickness	100	nm
Emitter width	150	nm
Base thickness	30	nm
Collector thickness	160	nm
Collector length	500	nm
BOX thickness	400	nm
Emitter doping	1×10^{20}	cm^{-3}
Base doping	1×10^{19}	cm^{-3}
Collector doping	7.5×10^{17}	cm^{-3}
Reach through doping	5×10^{19}	cm^{-3}
Substrate doping	1×10^{15}	cm^{-3}

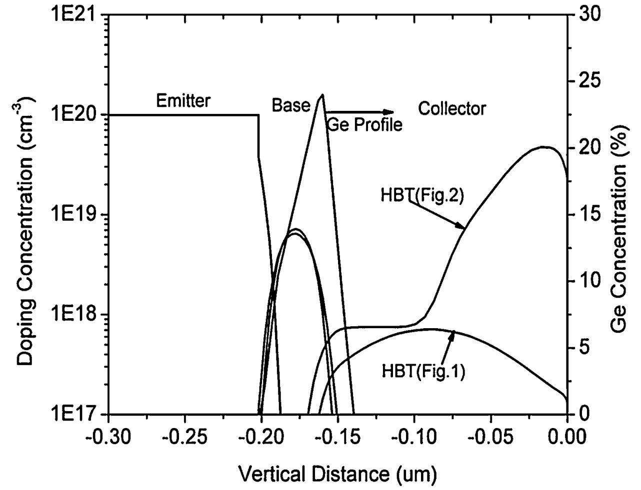

Fig. 3. Doping Profile of the npn SiGe HBT on thin-film SOI.

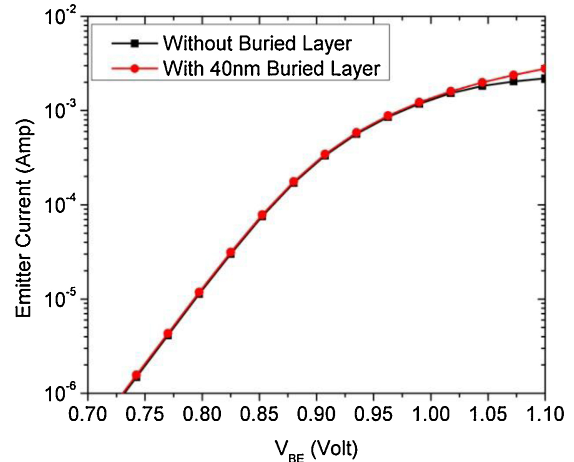

Fig. 4. Emitter current of the npn SiGe HBT.

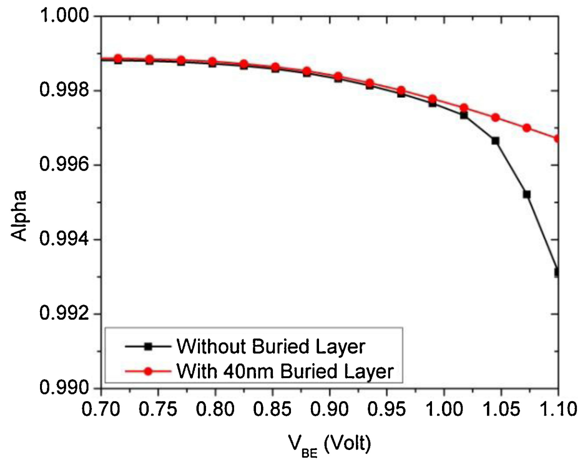

Fig. 5. Alpha of the npn SiGe HBT.

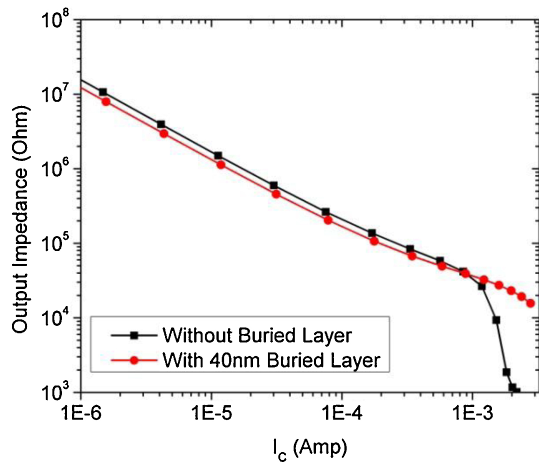

Fig. 6. Output impedance of the npn SOI HBT.

respectively. For SiGe, the Shockley–Read–Hall concentration parameter for electrons and holes was $1E^{17}\,cm^{-3}$. In Si, a value of $5E^{16}cm^{-3}$ was used for the Shockley–Read–Hall concentration parameter of electrons and holes. Slotboom bandgap narrowing model is used [29]. The bandgap narrowing voltage, concentration, and constant parameter for SiGe were 6.92 mV, $1.3E^{17}cm^{-3}$, and 0.5, respectively. A value of 12.6 was chosen for the relative permittivity of SiGe. The nonlocal impact ionization model [30] was used. With the help of aforementioned models, the current density of the HBT was calculated [24].

The proposed HBT has 40 nm of N+ buried layer and 120 nm of deposited film. In the device simulation, $V_{\rm CE}$ was 1.2 V and $V_{\rm BE}$ was varied from 0 to 1.1 V. The emitter currents are obtained and compared as shown in Fig. 4. At higher $V_{\rm BE}$, the injection from emitter is better in the HBT with N+ buried layer. The alpha value is plotted in Fig. 5. The HBT with N+ buried layer has high value of collector current due to better injection from emitter side and better alpha value.

The HBT with N+ buried layer has low $I_C R_C$ drop across extrinsic region. Hence, the available $V_{\rm CE}$ for the intrinsic transistor part is higher compared to the standard HBT. The output impedance is plotted as shown in Fig. 6. It has been observed that the output impedance ($r_0 \,||\, R_C$) is low in the HBT with buried layer when I_C is less than 0.88 mA which is due to the low value of collector resistance compared to the HBT without buried layer. But when $I_C > 0.88$ mA, the output impedance in the HBT with buried layer is higher than the HBT without buried layer. In the HBT with buried layer, the collector doping profile intersects the base profile at higher

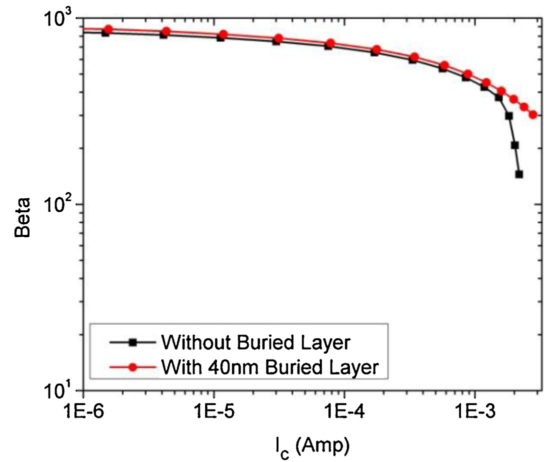

Fig. 7. Beta of the npn SOI HBT.

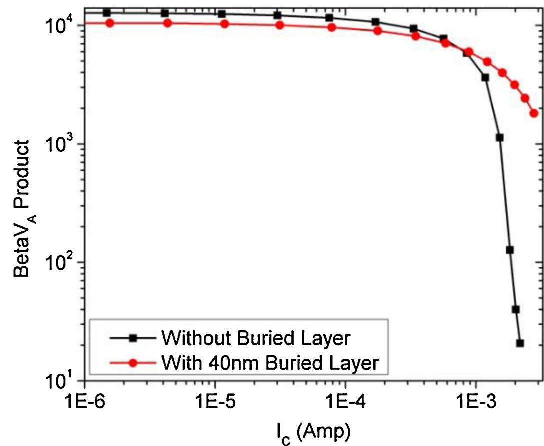

Fig. 8. βV_A product of the npn SOI HBT.

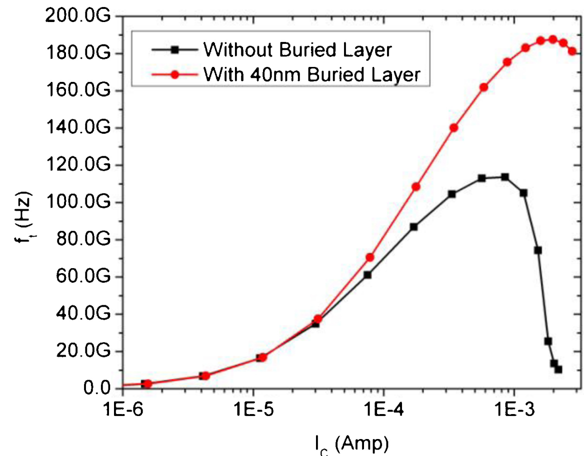

Fig. 9. f_t of the npn SOI HBT.

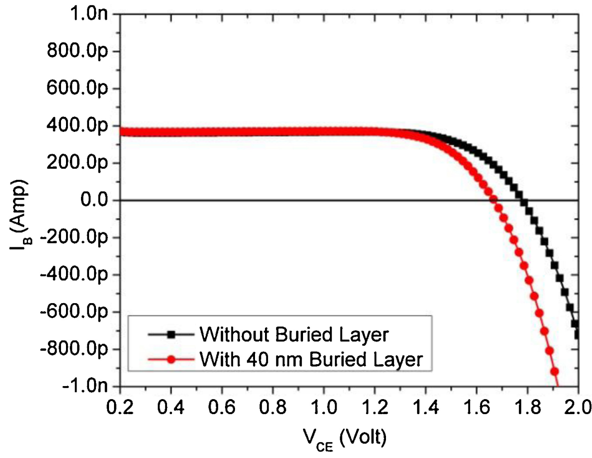

Fig. 10. BV_{CEO} of the npn SOI HBT measured from base current reversal point at V_{BE}= 0.7 V

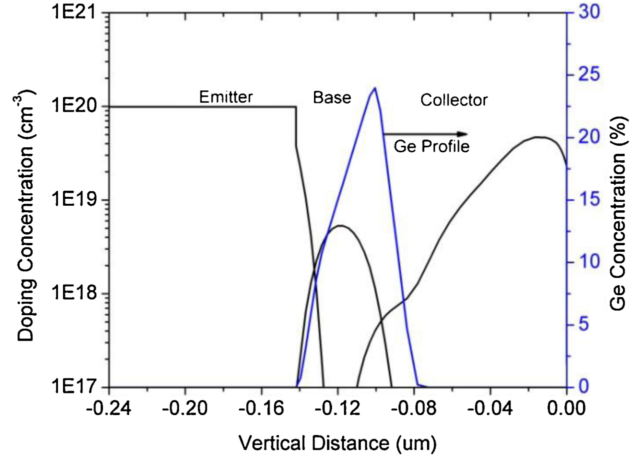

Fig. 12. Doping profile of the npn SOI HBT with 40 nm buried layer and 60 nm deposited film thickness.

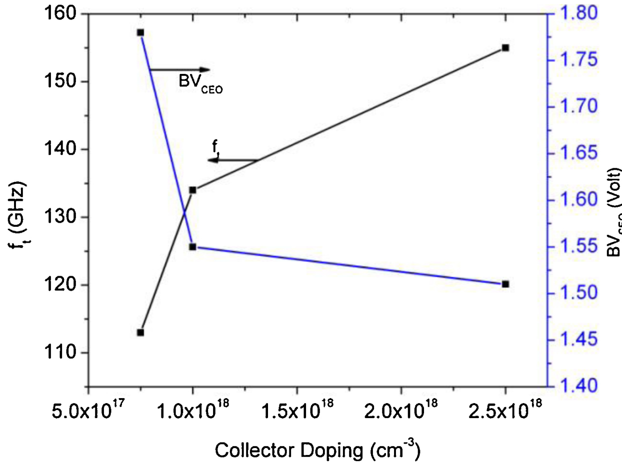

Fig. 11. f_t and BV_{CEO} of the npn SOI HBT without buried layer at high value of collector doping.

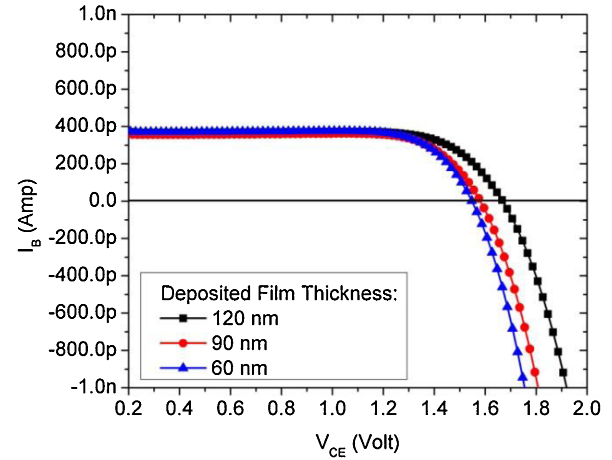

Fig. 13. BV_{CEO} of the npn SOI HBT with different film thicknesses measured at base current reversal point at V_{BE} = 0.7 V.

doping value (see Fig. 3) compared to the HBT without buried layer. At high injection, the high value of collector doping profile in the HBT with buried layer results in the high r_0 value resulting in high Early voltage. The better beta and better Early voltage results in improved βV_A product in the proposed npn HBT. The beta and βV_A product is shown in Figs. 7 and 8, respectively. The base collector space charge region expands at high injection and at very high current density, the depletion region gradually withdraws from the base. The f_t values of both HBTs are obtained and the results are compared in Fig. 9. A maximum of 187.5 GHz f_t value can be obtained. The f_t value of the npn HBT can be written as follows:

$$\tau_{ec} = \tau_b + \tau_c + \frac{V_t}{I_c}(C_{eb} + C_{bc}) + C_{bc}(r_e + r_c) \quad (1)$$

$$f_t = \frac{1}{2\pi\tau_{ec}} \quad (2)$$

where τ_{ec}, τ_b, τ_c, V_t, I_c, C_{eb}, C_{bc}, r_e, and r_c are total delay time, base transit time, collector transit time, thermal voltage, collector current, base–emitter capacitance, base–collector capacitance, emitter resistance, and collector resistance, respectively. The (C_{BE} + C_{BC}) and (C_{BE} + C_{BC})/g_m and I_C values are 15.7 fF, 0.479 ps, and 0.852 mA at the peak f_t of HBT without buried layer, whereas the HBT with buried layer has 12.1 fF, 0.159 ps, and 1.98 mA, respectively. In the presence of buried layer, the performance of the HBT is better in terms of f_t and the Kirk effect gets delayed. The total transit time of HBT without buried layer is 1.4 ps, whereas the HBT with buried layer has 0.85 ps. After computing $R_C(C_{BE}+C_{BC})$ and (C_{BE} + C_{BC})/g_m value for the two devices, reduction of 0.23 and 0.32 ps is observed in the case of HBT with buried layer. The reduction in the transit time is attributed to an improvement in transconductance to a large extent in the case of HBT with buried layer. Here, it is to be noted that the transconductance enhancement is due to delayed saturation. At higher V_{BE} ($V_{BE} > 1.0$ V), the (C_{BE} + C_{BC}) value increases very rapidly; as a result, any increase in the transconductance value does not contribute to the f_t improvement.

The breakdown voltage BV_{CEO} of the npn SOI HBT has been measured from base current reversal point at V_{BE} = 0.7 V. The BV_{CEO} of the HBT without buried layer and with buried layer are 1.78 and 1.67 V, respectively, as shown in Fig. 10.

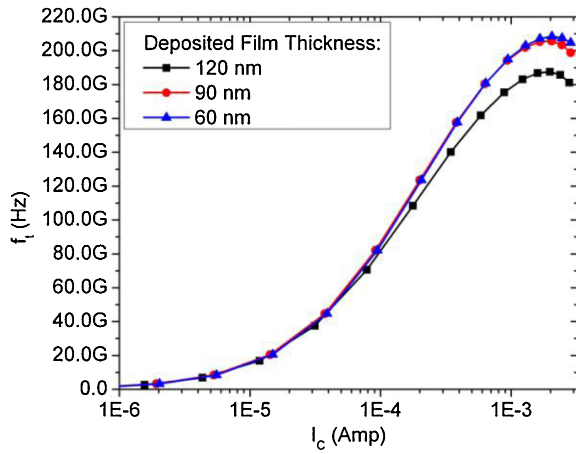

Fig. 14. f_t of the npn SOI HBT with different film thicknesses.

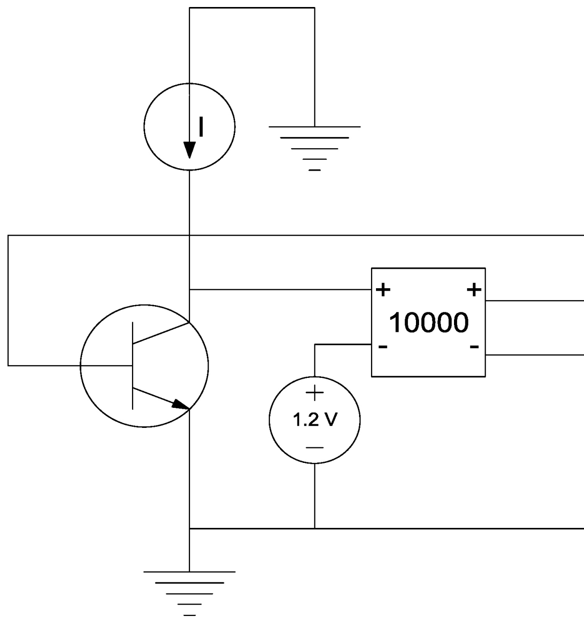

Fig. 15. Simulation setup for analyzing the self-heating effect of the npn SOI HBT.

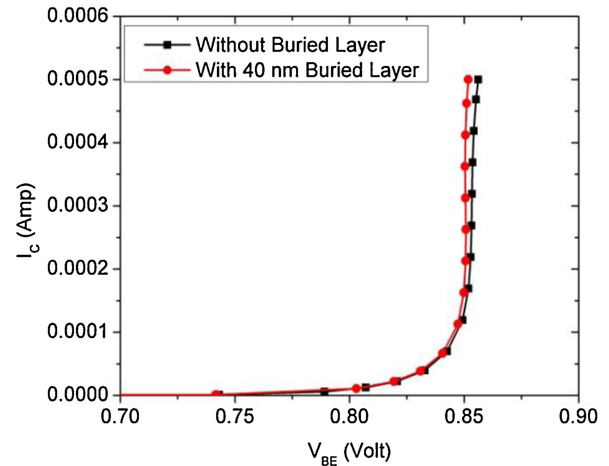

Fig. 16. Self-heating effect of the npn SOI HBT.

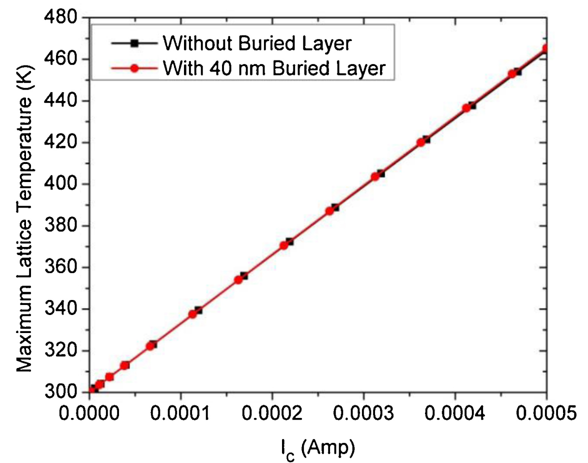

Fig. 17. Maximum lattice temperature of the npn HBT.

The $f_t BV_{CEO}$ product for the HBT without buried layer is 202 GHzV. A 313 GHzV of $f_t BV_{CEO}$ product can be obtained for the HBT with 40 nm buried layer. The 55 % increase in the $f_t BV_{CEO}$ product is observed by this technique. Fig. 11 shows peak f_t value and BV_{CEO} of HBT without buried layer for different collector doping. It can be seen that the maximum f_t value for such a device is 155 GHz with a collector doping of $2.5E^{18}cm^{-3}$. The f_t value of HBT with buried layer is much higher than the HBT with all implanted film at same $f_t BV_{CEO}$ value (1.6 V). By increasing the collector doping in the HBT with all implanted films, the R_C value decreases and C_{BC} value increases. The deposited film thickness has been scaled to study the tradeoff in the performance. The doping profile of the HBT with 40 nm buried layer and 60 nm epilayer is shown in Fig. 12. It has been observed that the buried layer diffuses toward the base in the HBT. The BV_{CEO} and f_t values are plotted in Figs. 13 and 14, respectively. The decrease in the breakdown voltage is due to the diffusion of buried layer toward base. By decreasing the deposited film thickness, the f_t increases and the BV_{CEO} decreases. The f_t values are 187.5, 205.6, and 208 GHz for the HBTs with deposited film thickness

120, 90, and 60 nm, respectively. The BV_{CEO} values are 1.67, 1.58, and 1.55 V for the HBTs with deposited film of 120, 90, and 60 nm. The $f_t BV_{CEO}$ product values are obtained as 313, 325, and 322 GHzV by depositing 120, 90, and 60 nm film thickness. The $f_t BV_{CEO}$ product of the HBT with 90 nm of deposited film is maximum, i.e., 325 GHzV. The Kirk effect gets delayed at low film thicknesses. This can be attributed to high transconductance value at peak f_t value. The maximum f_t value of HBT with 70 nm of n+ layer and 90 nm of epilayer is 216 GHz. The BV_{CEO} of this HBT is 1.58 V (similar as the HBT with 40 nm n+ layer and 90 nm epilayer). The $f_t BV_{CEO}$ product of this HBT is 341 GHzV. This HBT can be an added RF device to the existing 130 nm SOI CMOS technology.

III. Self-Heating Effect of the npn HBT

A theoretical and numerical analysis of the electrothermal behavior of single-finger bipolar transistors is proposed in [31]. The simulation setup for analyzing the self-heating effect of

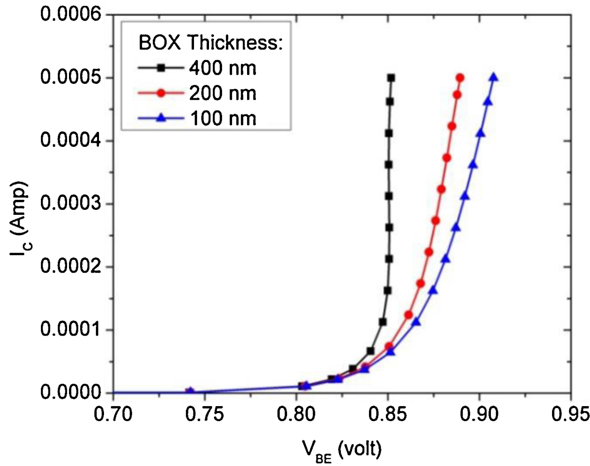

Fig. 18. Self-heating effect of the npn SOI HBT with different BOX thicknesses.

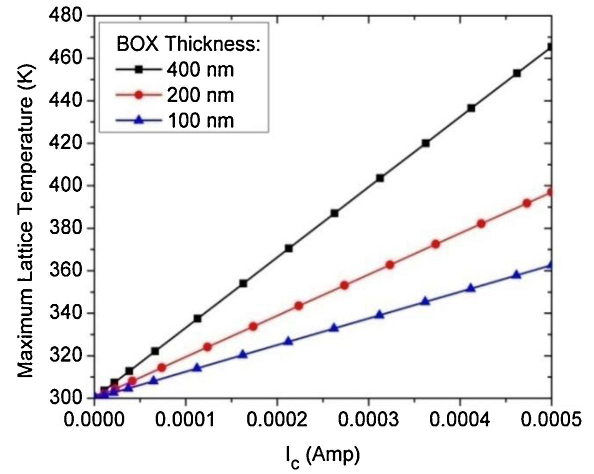

Fig. 19. Maximum lattice temperature of the npn SOI HBT with different BOX thicknesses.

the npn SOI HBT is shown in Fig. 15 [32]. For this device, 1.2 V of supply voltage was used. A feedback amplifier was used with voltage gain of 10 000 for applying the bias to the base terminal and the collector current was varied linearly so that the device can be heated slowly. The collector current heats the HBT resulting in the rise of lattice temperature. The rise in the lattice temperature increases the carrier concentration causing an increase in the collector current. Hence, less V_{BE} will be needed to keep the collector current constant. The feedback is applied to vary the V_{BE} value and keeping the V_{CE} value of 1.2 V. To simplify the analysis, a thermal electrode was used at the bottom of the device with surface resistance of 0.00004 $\mathrm{Kcm^2/W}$. The other electrodes were unaltered. Temperature was coupled to solve the heat equation for obtaining the lattice temperature due to self-heating. The value of specific mass density of SiGe was 2.92 $\mathrm{gm/cm^3}$. The specific heat model for SiGe was used by setting the model parameters cv, cv_b, cv_c, and cv_d as 1.72 $\mathrm{J/(Kcm^3)}$, $0.284\mathrm{E}^{-3}\mathrm{J/(K^2cm^3)}$, 0.0, and $-0.28\mathrm{E}^5\,\mathrm{J/(K^3cm^3)}$, respectively. The thermal conductivity model was used by setting the parameter values of A, B, and C as 0.36 cm K/W, 1.2E-3 cm/W, and $1.3\mathrm{E}^{-6}\,\mathrm{cm/(WK)}$, respectively. For silicon, the specific heat model parameters, cv, cv_b, cv_c, and cv_d were 1.98 $\mathrm{J/(Kcm^3)}$, $0.35\mathrm{E}^{-3}\mathrm{J/(K^2cm^3)}$, 0.0 and $-0.37\mathrm{E}^5\,\mathrm{J/(K^3cm^3)}$, respectively. The thermal conductivity model parameters, A, B, and C were 0.03 cm K/W, 1.56E−3 cm/W, and $1.65\mathrm{E}^{-6}\mathrm{cm/(WK)}$. The specific mass density of silicon was 2.32 $\mathrm{gm/cm^3}$. The self-heating effect of the HBT without buried layer and the HBT with buried layer is shown in Fig. 16. The maximum lattice temperature of the HBT as a function of I_C is obtained and plotted in Fig. 17. It has been observed that the thermal performance of the HBT with buried layer is nearly the same as the HBT without buried layer. Both HBTs have similar turn-on voltage. The lattice temperature of 465 K was obtained in base–emitter junction of HBT with buried layer at 0.5 mA of collector current. To reduce the self-heating effect, the scaling of BOX thickness was applied. The input dc characteristic of the npn HBT is shown in Fig. 18. Fig. 19 shows the maximum lattice temperature of the HBT with different BOX thicknesses. At 0.5 mA of collector current, the maximum lattice temperature is 361 K in the HBT with 100 nm BOX. The HBT with buried layer together with thin BOX has better performance in terms of self-heating. Therefore, it would be a potential candidate for the applications requiring high drive strength and high speed.

IV. Conclusion

The 2-D numerical simulation of the npn SiGe HBT on thin-film SOI has been performed with trapezoidal Ge profile in the base layer. The simulation studies of HBT with N+ buried layer are reported on thin-film SOI. The proposed HBT has 313 GHzV value of $f_t\mathrm{BV_{CEO}}$ product. The performance of the proposed HBT is increased by 55% compared to the SOI HBT without buried layer. The deposited film thickness is scaled to improve the $f_t\mathrm{BV_{CEO}}$ product. The study shows that the HBT with 70 nm n+ buried layer and 90 nm epilayer has a value of 341 GHzV $f_t\mathrm{BV_{CEO}}$ product resulting in 70% improvement. The thermal performance of the SOI HBT with buried layer is studied and the BOX thickness is scaled to reduce the self-heating effect. The study shows that the thin BOX HBTs are less sensitive toward self-heating effect as expected. The HBT is compatible with thin-film SOI CMOS technology and could be a potential candidate for the future SOI BiCMOS technology.

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