Semiconductor Logic Technology Innovation to Achieve Sub-10 nm Manufacturing

Klaus Schuegraf, Mathew C. Abraham, Adam Brand, Mehul Naik, and Randhir Thakur

***Abstract*—Moore's Law represents the cumulative effort by many participants to advance the productivity of electronic systems over the last 40+ years, resulting in enormous strides in the capability and ubiquity of electronics. This paper identifies the innovation challenges the semiconductor industry must overcome in order to propel the advance of semiconductor technology to the cadence of Moore's Law. Key examples will highlight the solutions needed to enable advanced transistor and nano-scale interconnect fabrication. Solutions for tomorrow's low voltage, low power process technologies will introduce new materials, unprecedented levels of interface control and new energy sources while at the same time addressing the increasing cost and complexity needed to sustain Moore's Law well into the future.**

***Index Terms*—Device scaling, Semiconductor manufacturing.**

I. Introduction

THIS PAPER surveys the key challenges faced in driving Moore's Law into the sub-10 nm regime. Primarily, the discussion covers the technical challenges facing the semiconductor industry as Moore's Law moves from its fifth to sixth decade. The technology roadmap to advance computing looks solid for the rest of this decade from a technical perspective. Therefore, the continuing revolution in computing technology towards ever increasing levels of capability and mobility is within reach.

The rapidly falling cost of computing has opened entirely new business models to monetize advanced technology. For example, in the consumer-facing end-market, vertical integration of capabilities including hardware, software, applications ("apps"), internet, e-commerce, and fulfillment has led to entirely different types of non-traditional "computer" companies in the form of Apple, Google and Amazon to name just a few. Given its tremendous economic and societal impact, this paper starts with a brief introduction to the significant economic challenges and business impact facing the semiconductor manufacturing industry. These challenges, if not met with creative, innovative and collaborative solutions, jeopardize sustaining the benefits of Moore's Law.

First, semiconductor manufacturing is increasing exponentially in complexity. This complexity has multiple facets. The sheer number of transistors in a leading-edge integrated circuit now numbers in the billions. Managing design, debug, development, product introduction, yield, and manufacturing requires continued advances in the capability of the entire semiconductor ecosystem. The number of different films, materials and critical interfaces in the process flow is increasing dramatically. Each interaction must be carefully understood, controlled, and made reproducible to obtain stable yields at the high production volumes necessary to achieve return on the extraordinary capital invested in state-of-the-art fabrication facilities.

Second, cost is becoming a dominant concern in semiconductor manufacturing. The cost of manufacturing, whether measured by capital expenditure to achieve a given capacity level or measured by the cost to manufacture an integrated circuit die, is rapidly increasing. In the past, increased capital intensity resulted in reduced die-level manufacturing cost. Going forward, this gain is at risk. Furthermore, the cost of research and development to create leading-edge manufacturing processes is increasing due to the cost of capital for development equipment sets and the cost of complexity with so many human and technical interfaces needing to be carefully managed to deliver new manufacturing technologies at the two-year cadence of Moore's Law.

Finally, the cost of manufacturing and development is leading to significant concentration in the semiconductor manufacturing base.The top three semiconductor manufacturers now routinely account for more than 60% of capital investment on an annual basis. This concentrated buying power of products and services is driving the associated trend of consolidation in the supplier base, particularly for semiconductor capital equipment suppliers. Recent examples in the past year alone include the acquisitions of Varian by Applied Materials, Novellus by Lam Research, FSI by Tokyo Electron, and Cymer by ASML. This concentration of activity is leading to a reduction in the diversity of competing technology solutions. As such, new business models and collaboration models are developing to align and tightly integrate development roadmaps between manufacturers and equipment suppliers. With such high research and development costs, there is little or no margin for delay or failure.

Manuscript received March 18, 2013; revised May 28, 2013 and June 23, 2013; accepted June 23, 2013. Date of publication June 27, 2013; date of current version July 18, 2013. This review of this paper was arranged by Editor-in-Chief R. P. Jindal.

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Digital Object Identifier 10.1109/JEDS.2013.2271582

On the technical front, this paper will explore the key drivers and responses to this business landscape. These include the challenges in patterning, the technology that creates the ever finer features needed for Moore's Law. Photolithography is a particularly critical technology, but so too are enabling technologies in precision etch and patterning films. Wafer scaling, the drive to migrate to more productive 450 mm wafers, is another critical technical problem, particularly for the equipment suppliers that must invent the new technologies needed to create films with precision requirements across a 50% larger manufacturing substrate. Finally, on the materials front, there is significant demand from the device roadmap for new materials for dielectrics and metals with excellent gap fill properties, thermal stability and compositional control. Additional challenges include the need to precisely engineer the interfaces between films. Metrology to assess in real time whether an interface, a film or a dimension is within manufacturing tolerance has become a critical capability for manufacturers and equipment suppliers alike.

II. Technology Roadmap

Fig. 1 illustrates the logic technology roadmap and alternatives for key components with timing for critical decision points for the next decade. Since logic technology has been driving the investment and innovation engine for semiconductor manufacturing for the last five years, this roadmap guides a significant fraction of R&D investments for device manufacturers and semiconductor capital equipment suppliers alike. Fig. 1 reflects an attempt by the authors to create a realistic, composite view of the technology roadmap. This view addresses a widespread concern that the ITRS roadmap insufficiently representsthe timing expected for introducing solutions to challenges for leading edge manufacture. As an illustrative roadmap, it is not meant to precisely communicate the roadmap of any particular semiconductor device manufacturer.

A. Wafer Scaling

At the top level of the manufacturing roadmap is the call to migrate from 300 mm to 450 mm wafers. The demand for this significant new capability arises in response to a rapid increase in process complexity and manufacturing cost.This manufacturing cost is particularly influenced by the rapidly rising cost of patterning. The objective of moving manufacturing technology to 450 mm wafers is to lower the overall manufacturing cost on an area basis, as measured by cents/mm^2.

B. Transistor

The transistor manufacturing process is experiencing an accelerating pace of innovation with the rapid migration to single-wafer processing. This trend is driven by the demand for new materials and unprecedented precision in film composition, dimensional control, and interface condition. First, new materials like SiGe were introduced with epitaxially-induced lattice strain for increased channel mobility. Then,

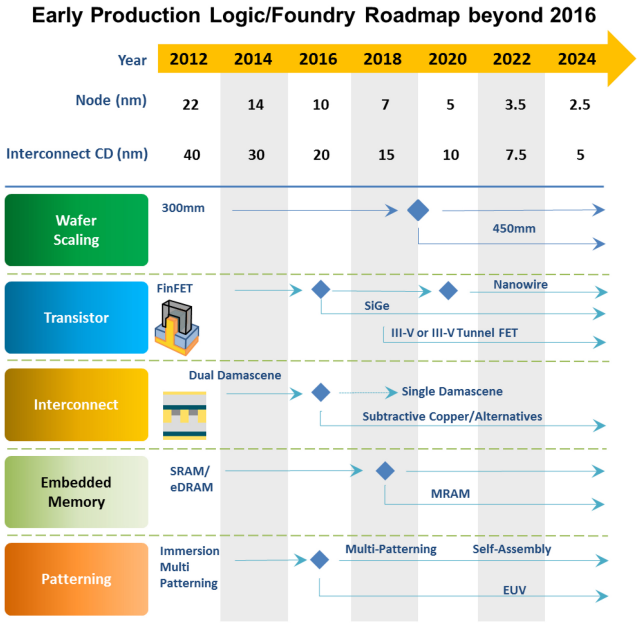

Fig. 1. Illustrates Logic technology roadmap and alternatives for key components with timing for critical decision points.

the entire gate stack was migrated to high-k gate dielectric and metal gate to scale the effective oxide thickness (EOT) of the gate dielectric. Now, the industry is aggressively focused on quickly migrating to the FinFET transistor architecture. This three-dimensional architecture has superior electrostatic control, but relies on new processes and materials with an emphasis on conformality for deposited films and doping. In addition, the 3Dnature of the structure places unique challenges on etch, planarization, and inspection processes to create a yielding device. With the FinFET, the fin now becomes the smallest dimension of the device, a role previously played by the gate dimension, requiring significant innovation in dimensional control, structural integrity, and interfacial preparation.

Going forward, the FinFET will see dimensional scaling and the introduction of new channel materials. The electrostatic advantage of the FinFET may be insufficient for technology nodes beyond 5 nm, leading to the evolutionary alternative of GAA (Gate All Around), also referred to as nanowire transistors [1]. Research into the more revolutionary ultra-low power alternatives such as Tunnel FET is also gaining momentum [2].

C. Interconnect

Copper dual damascene [3] has been the workhorse technology for 300 mm manufacturing. Looking forward, the critical RC-delay metric is rising alarmingly at the 22 nm and 14 nm technology nodes – leading to significant concerns from circuit designers that interconnect may limit technology scaling [4]. Fortunately, the promising alternatives of either single damascene or subtractive interconnect are under consideration. These alternatives rely on a radically different set of materials formation for the bulk wire, the barrier, and insulating dielectrics.

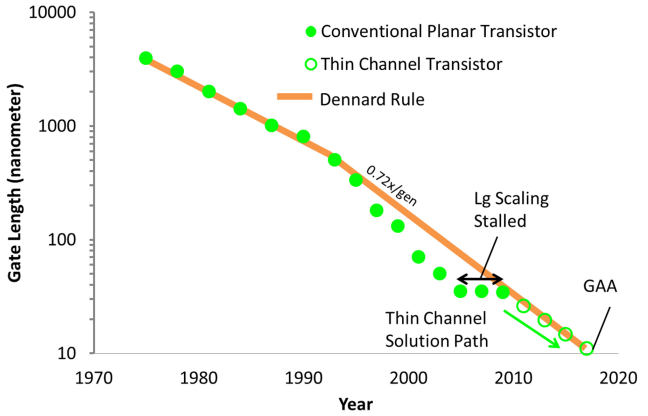

Fig. 2. Transistor channel length was scaled down according to Dennard's rules (0.72x per generation) till the turn of the century, corresponding to 350 nm node. Starting with 250 nm node, Intel accelerated gate length scaling, seen as deviation of the green dots from the Dennard line. From the 65 nm node channel length scaling slowed down due to power dissipation concerns, which is seen in flattening of the green dot line. To sustain Moore's law in the form of continued reduction in packing density, the gate length needs to follow the Dennard line again. Thin silicon channel architecture, FinFET or UTB-SOI, enables the continued gate length scaling beyond 32 nm node as shown by the open green dots. By the end of the decade, at 5 nm node we will likely see the adoption of GAA architecture [11].

D. Memory

Embedded SRAM has served logic technology well for generations due to transistor compatibility with digital CMOS. For some niche applications, eDRAM provides a high density alternative with reasonable performance and power performance [5]. With lower power operation at advanced nodes, the stability of the SRAM is becoming more marginal. Since SRAM consumes a significant die area for logic ICs, Spin Transfer Torque MRAM (STT-MRAM) has attracted great interest as a low power, area efficient memory [6]. Additionally, non-volatile MRAMcan offer power savings in stand-by and re-boot modes. The key challenges in MRAM technology include angstrom-level precision in the deposition of magnetic materials and damage-free patterning to preserve the magnetic properties of the unit bit at small dimensions.

E. Patterning

The key challenges in patterning relate to the availability of a high productivity,direct-patterning lithography solution. Direct patterning, the conventional combination of a single lithography exposure followed by an etching pattern transfer from resist to an underlying film, is being supplanted by multi-patterning in the absence of a mature Extreme Ultraviolet (EUV) lithography solution. Multi-patterning relies on a significant increase in process complexity by combining several exposure, etch and deposition steps [7], [8]. Furthermore, multi-patterning leads to severe layout restrictions and employs comprehensive use of computational lithography techniques. As multi-patterning evolves in progressive generations, the pain in terms of cost complexity and yield is rising. EUV remains a significant industry priority, but the search is increasing for alternatives. These include directed self-assembly and 3D vertical nanowires.

TABLE I
XTRAPOLATED DESIGN RULES FOR FINFET SCALING FROM WHAT IS IN PRODUCTION TODAY

Node		Critical dimension in nanometers			
		22	14	10	7
Gate	Pitch	88	56	40	28
	Length	27	20	15	11
Fin	Pitch	60	42	29	21
	Width	14	10	7	5
	Height	36	26	19	14
Contact	to Gate Width	66	46	32	23
	to Source/Drain Width	23	16	11	7
Interconnect	Pitch	88	56	40	28
	Width	44	28	20	14

Thislarge number of potential branch points in the technology roadmap is technically exciting and leaves room for competition to create an optimal solution. However, since manufacturing investments require certainty due to their long-term nature, it is important to create greater certainty in the roadmap direction prior to migrating to 450 mm manufacturing. Thus today there is intense effort to define "future proof" pathways for key aspects in the roadmap. To set a framework and context for the solutions needed for a roadmap consistent with Moore's law, it helps to begin with understanding the design rule boundary conditions.

III. DESIGN RULE FRAMEWORK

Fig. 2 illustrates the historical context of the dramatic reduction in integrated circuit feature according to Moore's law in the MOS transistor era. Gate length has been the defining critical dimension in advancing integration, providing benefits of improved performance, packing density, power consumption, and cost per transistor. Going forward, with the semiconductor industry transitioning to the 3DFinFET [9]–[11], the fin dimension supplants the gate as the smallest feature.

Table I provides an estimate to predict the trajectory of design rule scaling for critical dimensions in FinFET manufacturing technologies from the 22 nm to 7 nm nodes. Since today's state-of-the-art immersion 193 nm lithography systems can resolve features of approximately 40 nm on an 80 nm pitch, the table shows clearly that at 22 nm the fin layer, and in subsequent nodes, the interconnect layers will require alternative patterning solutions as EUV (13.6 nm) lithography with its promise to print 30 nm pitch structures is not yet viable. These solutions will likely draw on "multiple patterning" schemes based on immersion 193 nm lithography. One alternative relies on multiple Litho-Etch (LE) exposures, such as two-pass LE-LE or even three-pass LE-LE-LE. Conceptually, Litho-Freeze-Litho-Etch (LF-LE) offers an appealing alternative, but finds limited practical application [12]. The LE-LE techniques are best suited for semi-regular structures limited by overlay constraints. Alternatively, spacer-based pitch division techniques like Self-Aligned Double Patterning (SADP) and Self-Aligned Quad Patterning (SAQP) can be used for highly periodic grids.

The contact layer for a 10 nm node SRAM circuit illustrates the patterning complexity using immersion 193 nm

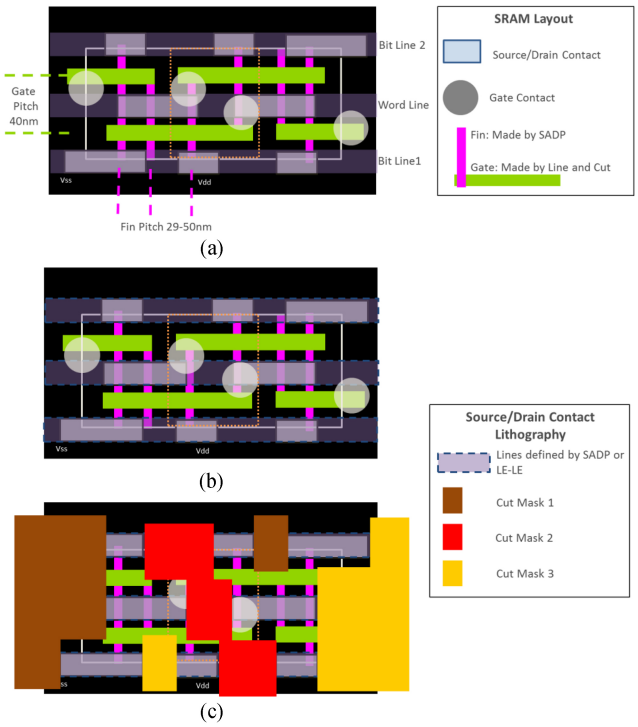

Fig. 3. a) Representitivelayout of SRAM FinFET layout and design rule at 10 nm node [13]–[15]. (b) and (c) illustrate the patterning steps needed to define contact to source/drain for 7 nm nodes as per design rules listed in Table 1.

lithography. Fig. 3(a) shows a representative layout of a typical SRAM cell [13]–[15], identifying the critical structural components desired in the SRAM cell, the fin, the gate and the contacts. Fig. 3(b) and (c) illustrate a likely sequence for patterning the source/drain contact layer. Fig. 3(b) shows a periodic set of lines with a 40 nm pitch to be likely formed using SADP. This structure will be transferred to a hard mask. Since contacts need to be electrically isolated to achieve unique access to each source and drain region, three 'cut' masks can be applied sequentially in LE-LE-LE fashion and transferred to the hard mask. Transferring the pattern from these four critical exposures (one for SADP, three for LE-LE-LE cut mask) completes the source/drain contact. The LE-LE-LE and SADP sequences are technically feasible and have reached production capability. Both techniques require new types of films for hard masks, conformal spacers, creative solutions for etch and materials removal with stringent dimensional uniformity requirements. These techniques also create the need for solutions with low defectivity to achieve high yield.

Similar analysis of the gate contact shows that it requires three patterning steps. In aggregate the contact layer requires seven patterning exposures unless the much anticipated EUV lithography using 13.6 nm wavelength can be introduced into-production. Apart from patterning, sculpting and dressing the features with various thin films with specific properties in 3D with atomic-level control of the interfaces is critical for device performance. The following two sections will cover some of the main challenges in scaled advanced transistor and nano-scale interconnect formation.

IV. Advanced Transistors

Transistor scaling for the planar MOS structure, as shown in Fig. 2 has largely followed the Dennard predictions for the structural dimensions of gate length (L_g),oxide thickness (X_{ox}) and junction depth (X_j), and to a lesser extent voltage scaling.Strict voltage scaling following the Dennard prediction has proven difficult in practice due to off-state leakage constraints, leading to limited scalability of device threshold voltage V_t and supply voltage V_{cc}. In practice, the supply voltage for planar CMOS integrated circuits has stopped scaling and has been stuck at approximately 1 Volt. This power and leakage constraint motivated the search for new pathways to achieve continued device performance improvements as aggressive gate length dimensional scaling became less practical. These newer pathways follow a "materials scaling" paradigm to differentiate from the classical dimensional scaling approach relying mostly on patterning and film thickness.

The materials scaling paradigm has led to an explosion of complexity in the new materials required to manufacture a modern planar MOS transistor. Each of these newly introduced materials brings its own unique challenges. These include material formation, compositional control, interfacial control, and metrology to name a few. With such stringent material constraints, single-wafer vacuum manufacturing processes are finding increasing use in front-end of line applications. Additionally, control over interfaces between these new and existing materials requires vacuum transfer to limit exposure to clean room and oxidizing ambients, leading to increased use of clustered vacuum processing in the manufacturing process.

New materials have been introduced for mobility scaling to complement L_g scaling, starting with compressive and tensile dielectric stressors [16], and leading to epitaxially-formed stress enhancement with SiGe [17]. Progressive generations of embedded SiGe stressors have incorporated increasingly higher Germanium concentrations to deliver improved transistor mobility [18], [19].

For the gate dielectric, dimensional scaling of the silicon dioxide gate insulator to approximately 2 nm oxide thickness was first enabled with single-wafer nitride hardening sequences [20]–[22]. Subsequently, materials with higher dielectric constant (high-k) were introduced to achieve the EOT predicted by the Dennard rule [18], [23]. These materials drove significant changes in planar transistor architecture with the need for atomic control over the dielectric interface to the silicon transistor channel, the deposition of the high-k dielectric itself, and customized annealing sequences to achieve stable interface trap densities. The change to the high-k gate dielectric itself proved insufficient and required a transition to metal gate electrodes chemically compatible with the high-k material. Where once a single, doped silicon polysilicon film was sufficient to form a gate electrode, now a complex stack with as many as six or seven thin metal films with precise dimensional and compositional control are needed to achieve desired device stability, workfunctions for V_t control, and gate resistance.

To achieve junction depth X_j scaling, various new implant and annealing technologies have found application. These include low-energy, high-purity implants as well as the adoption

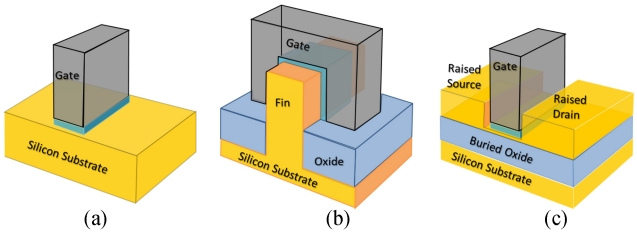

Fig. 4. The two new channel architectures, FinFET and UTB-SOI, are compared with the current industry-standard of planar CMOS architecture. The FinFET architecture employs a "fin" of silicon surrounded by the gate on three of its sides, left right and top surfaces, making it a 3D transistor. UTB-SOI employs an ultra-thin silicon channel which lies below the gate dielectric layer, and sits on top of the buried oxide. Note that these cartoons are not to scale. Table 1 shows possible FinFET dimension evolution, where the "fin" in the FinFET architecture would be approximately half the gate length, and for the UTB-SOI architecture the channel thickness would be approximately one fifth of the gate length [24].

of new species and conditions such as low temperature Carbon implants to scale junction thickness and improve junction leakage.

However, altogether all the new manufacturing technologies introduced to enable the material scaling paradigm have ultimately proved insufficient to achieve high-performance transistors operating at less than 1 Volt. The strong market growth and demand for mobile computing solutions is now driving transistor requirements. To create transistors with excellent performance below 1 Volt requires significant improvement in the electrostatic control of the transistor with the ultra-thin body transistor options of the FinFET or FD-SOI [24] device as shown in Fig. 4(b) and (c), respectively. The FinFET appears to be the primary transistor scaling path for 14 nm technology nodes and beyond. The FinFET presents an additional 3D scaling paradigm to complement materials and dimensional scaling approaches. The 3D scaling paradigm promises to add significantly greater complexity as transistor manufacturing technology reaches beyond 10 nm.

A. Advanced Transistor Scaling Challenges

Fig. 5 identifies some of the key challenges in creating process technologies to enable the manufacture of advanced FinFET transistors. As the fin dimension becomes the smallest critical dimension in the 3D structure, with a feature size approaching 10 nm or less, structural integrity of the fin becomes paramount. All sources of variation from lithography, etching, and subsequent process steps need precise control to limit fin width variation to 1 nm or less. Additionally, new techniques are finding adoption to prevent fin erosion from silicon consumption due to spacer etch or even short oxidation processes. Process recipes must be optimized to prevent the thermal and plasma shocks that can lead to pattern collapse. Solutions to achieve precise control over the recess of isolation dielectrics are necessary as the recess dimension determines the effective channel width, which must be closely matched across the integrated circuit independent of pattern density effects. As new Germanium and III-V-based channel materials will likely see adoption beyond 10 nm, techniques to form

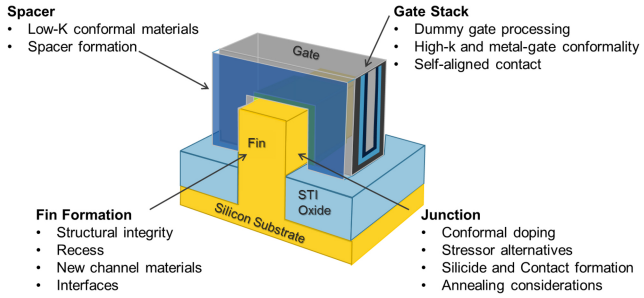

Fig. 5. Specific advanced transistor challenges in the formation of fin, spacer, gate stack and junction.

robust fins with new materials and manage interface states will be critical for FinFET scaling.

Fig. 5 illustrates many of the other key challenges in creating a robust and manufacturable FinFET technology. The 3D aspect of the FinFET places stringent requirements on the conformality of film deposition and doping processes. Similarly, etch processes must be tailored to avoid formation of undesired stringers and residues at the bottom of high-aspect ratio features. The gate stack adds considerable process complexity with the need for conformal dielectric and metal films that achieve the same requirements as advanced materials used in planar structures or their bulk equivalents. Conformal processes demand new chemistries, either avoiding organometallic pre-cursors or employing low-energy treatments to remove undesirable Carbon or other by-products that degrade film properties.

B. Metal Gate Scaling

Fig. 6 illustrates the complexity of interactions between the many films and materials needed to optimize a FinFET metal gate structure consistent with the requirement of a self-aligned contact (SAC) [10]. The left side of Fig. 6 is a complicated integration sequence with conventional materials to achieve a metal-gate structure. This sequence requires two metal recess etches to create a metal gate cappedwith dielectric material for SAC formation. First, the workfunction materials are removed to add a low resistance tungsten strapping layer to the metal gate. The tungsten must then be etched back to create a cavity for the dielectric capping layer. The simplified integration sequence as shown on the right side of Fig. 6, relies on a specially designed, low-resistance workfunction material that requires only a single etchback to insert the dielectric capping layer, avoiding the tungsten strapping layer. Furthermore, this approach shows better dimensional scalability in the form of improved small dimension resistance to enable simplified gate lengths scaling as shown in the center of Fig. 6.

C. Parasitic Control

To scale below 10 nm, the FinFET will likely see additional refinements to achieve continued low-power performance benefits. These improvements are best considered from two perspectives. First, Fig. 7 shows technology concepts to improve upon the resistive and capacitive parasitic elements limiting the FinFET extrinsically. Second, new technologies are in development to improve intrinsic transistor performance.

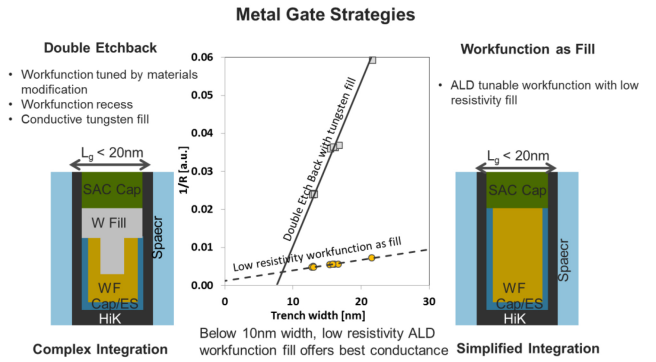

Fig. 6. Metal-gate integration strategies. Traditional double etch-back vs. simplified ALD tunable workfuction low resistivity material as fill.

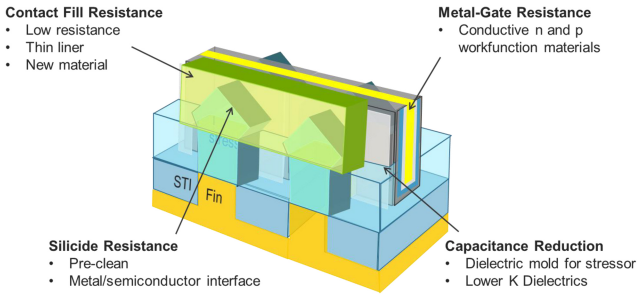

Fig. 7. Advanced transistor parasitic control challenges.

Fig. 7 shows the tremendous breadth of opportunities to use new scaled, conformal materials to reduce the parasitic limiters on FinFET performance. These include materials to improve metal gate resistance at small dimensions by engineering conformal, low resistivity n- and p-type workfunction metals. There are multiple approaches to attack various parasitic capacitances. These include gate-drain overlap capacitance resulting from the strong area overlap between the metal gate electrode and the stressor used to enhance mobility. Shaping technologies combined with conformal, low-k dielectrics to limit the overlap capacitance between gate and drain are promising as are new techniques to improve contact resistance by engineering the interface between the metal silicide and the junction. Additionally, fundamental improvements in the form of thinner barriers and new low-resistance fill materials promise to reduce contact resistance.

Enabling technologies to advance low-voltage intrinsic FinFET performance include higher-mobility channel materials based on Germanium and III-V compound semiconductors. Manufacturing will rely on processes that achieve low defect density by integrating the sequence of novel pre-clean techniques, lattice matching layers, and epitaxial growth of the channel material itself on a single vacuum mainframe. Gate dielectric scaling to thinner EOT on new-material 3D transistor channels will include conformal processes to control thinner interfacial layers, higher-k dielectrics and improved anneals to improve dielectric reliability for bias temperature instability and charge trapping. New channel materials will also drive improvements in annealing technology due to lower melting points and contact interface to overcome non-ohmic behavior.

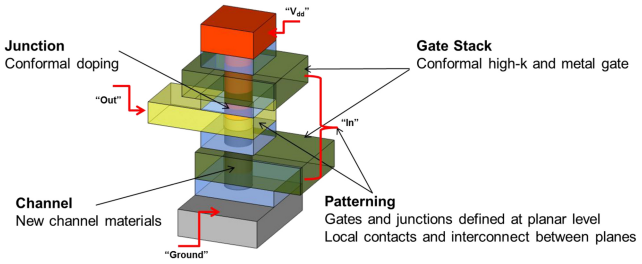

Fig. 8. Schematic of possible future stacked vertical GAA transistor architecture. These stacked transistors could possibly be interconnected to form universal gates which would deliver further compaction of circuit layouts.

D. Future Transistors

Beyond 7 nm, alternatives to the FinFET can take the form of evolutionary device architectures such as horizontal gate-all-around or nanowire structures which will require improved capability for nanowire formation, shape control and further refinements to conformality. Longer term and higher risk alternatives include vertical stacked gate-all-around (GAA) transistors, a schematic of which is shown in Fig. 8.These will enable further compaction, resulting in some easing in the need to scale critical dimensionsor III-V based Tunnel FET transistors targeting 300 mV operationfor dramatically low power [2], [25].

V. Nano-Scale Interconnect

A. Interconnect Performance

While much attention is focused on transistor innovation, it is interconnect performance that is also now challenging Moore's law because of its performance and scaling limitations [26], [4]. The last time interconnects were overhauled for performance reasons was more than 15 years ago when aluminum was replaced with copper interconnects fabricated in the revolutionary dual-damascene architecture [27].

Copper dual-damascene interconnects provided superior lower resistance, and the incorporation of porous low-k dielectrics into this architecture drove down the capacitance – together these two materials have reduced RC delay and reduced energy consumption. However, the reduction of the low-k dielectric constant has slowed in recent years because as they become more porous these dielectric materials become fragile, unable to cope with the mechanical stress that chips undergo during packaging, and are also not robust enough to maintain their low-k properties through the dual-damascene process integration steps. In addition, the resistance of the interconnect is rising dramatically because of three main factors: (i) the conventional tantalum nitride/tantalum high-resistance metallic barriers that block copper diffusion and prevent oxidation is taking up a larger fraction of the metal interconnect cross-section, (ii) surface scattering increases as critical dimension of the wire becomes smaller than the bulk mean free path of the electrons, and (iii) grain boundary scattering increases as the copper grain size scales approximately as the critical dimensions of the wire in dual-damascene fabricated interconnects [28]. Hence, the RC delay for interconnects has started to rise dramatically as the nodes shrink

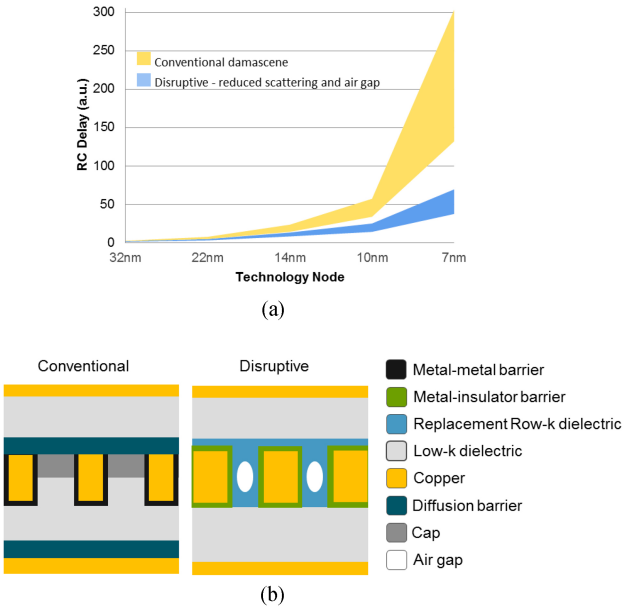

Fig. 9. (a) Modeled RC delay rising rapidly for conventional dual-damascene based interconnects driven by rise in resistance. Disruptive interconnect architecture such as the one shown in schematic cross-section (b), would reduce significantly the rise of RC delay.

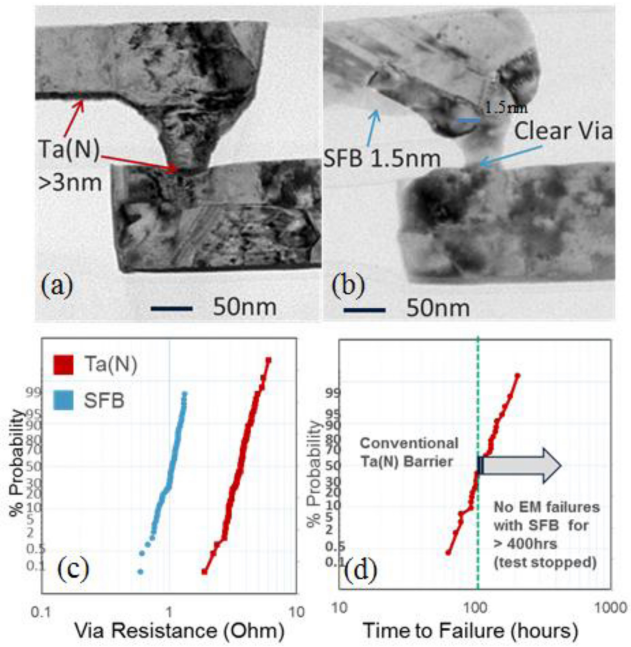

Fig. 10. Comparison conventional Ta(N) to self-forming barrier (SFB) for copper interconnects. TEMs of two level via structure used for electro-migration (EM) testing: (a) Dark region highlights conventional Ta(N) barrier >3 nm in thickness (b) Self-forming barrier of 1.5 nm (not clearly visible at large scale). SFB leaves no material at the bottom of the via leading to 3x lower via resistance (c) and electro-migration failure tests showed superior performance (d) as compared to conventional Ta(N) barrier, tests were stopped at 400hrs as no failures were detected.

beyond 22 nm, driven by the rise in resistivity for conventional damascene copper interconnects, as illustrated in Fig. 9(a). This dramatic rise in RC delay can be mitigated if disruptive technologies and integration schemes can be introduced to reduce electron scattering and significantly reduce the effective dielectric constant between interconnects.

We discuss below some of the possible solutions to reduce the RC delay rise. Fig. 9(b) is a schematic cross-section of a possible architecture that would include some of these disruptive technologies.

B. Solutions to RC Delay

(i) Self-Forming Barriers (SFB): It has been shown that manganese-based films can react with silicon based dielectrics to create a self-forming dielectric barrier [29]. As illustrated in Fig. 10(a) and (b), these barriers could consume much less volume than the conventional tantalum nitride/tantalum (Ta(N)) barriers if deposited using a highly conformal chemical vapor deposition (CVD) or atomic layer deposition (ALD), thus reducing the resistivity of the wire.

In addition, if these barriers are engineered precisely, it should be possible to form a smooth copper-dielectric barrier interface with good adhesion if the manganese used in forming the SFB is entirely consumed to form a dielectric self-forming barrier. Such a metal-dielectric barrier interface should have specular electron scattering as compared to diffuse scattering that occurs with conventional Ta(N) barrier layers [30]. Further, the high diffusivity of manganese in copper would ensure that there would be no barrier at the via interface connecting metal layers. Hence the via resistance with manganese based SFB would also be significantly less than those formed with a conventional Ta(N), also shown in Fig. 10(c) and (d).

(ii) Subtractive Copper: Apart from diffuse sidewall scattering, the second significant resistive electron scattering contribution for damascene-defined interconnects is grain-boundary scattering. It has been shown that the grain size scales proportionally to the critical dimension of the wire in copper damascene technology [28]. If one is able to define interconnects by patterning copper wires, e.g. by etching copper films deposited using physical vapor deposition (PVD), the grain size would then be much larger. Etching copper has several challenges andappropriate etching chemistry, hardmask, and robust hardware is yet to be discovered. Following copper etch, the copper surface would need to be encapsulated with barrier/liner material before dielectric is introduced between interconnects. Additionally, new concepts will have to be invented to realize self-aligned via to enable tightest pitches and better reliability.

(iii) Air-Gap Engineering: The schematic in Fig. 9(b) shows an air-gap between the interconnects, which can be achieved by either replacing the dielectric mold in a damascene architecture or filling the gaps between etched copper lines with a low-k dielectric whose conformality can be controlled to engineer a repeatable air-gap location and size. In both approaches the low-k dielectric between the wires would not be exposed to some of the harsher process steps in the conventional damascene flow and hence would also retain its as deposited dielectric constant. The concept of air-gap engineering is being assessed for logic applications [31] as it would significantly reduce capacitance. The repeatability and

mechanical reliability (electrical and mechanical) of air-gap engineered interconnects remain the biggest challenge.

(iv) Reliability: Double patterning is required to achieve sub-80 nm pitch interconnects in the absence of EUV lithography. Techniques such as LE-LE require precise overlay, which may lead to line-to-line and line-via shorting. While such techniques as self-aligned double patterning can be used for the metal to avoid intra-line issues, via patterning still requires LE-LE. Line-via shorting and time to dielectric breakdown (TDDB) metrics will be challenged. Self-aligned via is being used to solvethe via-metal overlay concerns at the same level, however, level-to-level mis-alignment will continue to drive TDDB concerns. Also, with the greater current densities achievable with advanced transistors, higher risk of electro-migration (EM) is a concern. Techniques such as selective capping using CoWP [32] or cobalt [33] of the most vulnerable top interface between copper and dielectric are at present being used to mitigate this risk but will probably need further interface engineering to increase bond strength at this interface.

C. Future Interconnects

Beyond the 7 nm node, materials such as tungsten could be viable alternatives to copper as metallic interconnects even though their bulk resistivity is higher than that of copper. The electron mean free path being shorter will lower the size-induced resistivity effect. Integration with no barrier-liner layers with low k will be key. The preferred material choice would depend on the specific integration scheme.Single damascene or subtractive approaches of defining the wires would open up the possibility of alternating conductor material options for wires and vias. Longer term options include carbon nanotubes [34],ribbons [35] as well as nanowires made of single crystal silicides [36].These options are subjects of intense research,although challenges remain in developing viable integration schemes and interface control. Further, high-end performance processors are trending towards highly parallel architectures where tens if not hundreds of computing cores could be made on a single die. Such dies would need terabits of data per second to be transferred onto and off the chip, data rates that are possibly steerable only with optical interconnects [37]. In the last few years, prototype chips with optical interconnects that are fully compatible with CMOS processing have been demonstrated, showing possible pathways for their adoption in products of the future [37].

VI. Conclusion

This paper broadly reviews the critical challenges in the semiconductor manufacturing roadmap and affirms that the outlook for innovative technical solutions is bright. However, the increasing capital intensity of sustaining Moore's Law calls for innovative solutions to fund research and development investment –for semiconductor manufacturers and capital equipment suppliers alike. These solutions will propel Moore's Law into its sixth decade, benefiting humanity with the unprecedented capabilities of future mobile integrated systems.

Acknowledgment

The authors would like to thank the talented and dedicated team at Applied Materials for its efforts to collaboratively synthesize innovation solutions to the increasingly more demanding challenges of semiconductor manufacturing.

References

[1] K. J. Kuhn, U. Avci, A. Cappellani, M. D. Giles, M. Haverty, S. Kim, R. Kotlyar, S. Manipatruni, D. Nikonov, C. Pawashe, M. Radosavljevic, R. Rios, S. Shankar, R. Vedula, R. Chaua, and I. Young, "The ultimate CMOS device and beyond," presented at the 2012 Electron Devices Meeting (IEDM).

[2] B. M. Borg, K. A. Dick, B. Ganjipour, M.-E. Pistol, L.-E. Wernersson, and C. Thelander, "InAs/GaSbheterostructure nanowires for tunnel field-effect transistors," *Nano. Lett.*, vol. 10, no. 10, pp. 4080–4085, 2010.

[3] P. C. Andricacos, C. Uzoh, J. O. Dukovic, J. Horkans, and H. Deligianni, "Damascene copper electroplating for chip interconnections," *IBM J. Res. Develop.*, vol. 42, no. 5, pp. 567–574, 1998.

[4] M. T. Bohr, "Interconnect scaling-the real limiter to high performance ULSI," in *Proc. IEDM,* 1995, pp. 241–244.

[5] R. E. Matick and S. E. Schuster, "Logic-based eDRAM: Origins and rationale for use," *IBM J. Res. Develop.*, vol. 49, no. 1, pp. 145–165, 2005.

[6] H. Yoda, S. Fujita, N. Shimomura, E. Kitagawa, K. Abe, K. Nomura, H. Noguchi, and J. Ito, "Progress of STT-MRAM technology and the effect on normally-off computing systems," presented at the 2012 Electron Devices Meeting (IEDM).

[7] C. Bencher, H. Dai, and Y. Chen, "Gridded design rule scaling: Taking the CPU toward the 16 nm node," *Proc. SPIE*, vol. 7274. 2009, p. 72740G.

[8] Y. Ma, J. Sweis, C. Bencher, Y. Deng, H. Dai, H. Yoshida, B. Gisuthan, J. Kye, and H. J. Levinson, "Double patterning compliant logic design," *Proc. SPIE*, vol. 7974. 2011, p. 79740D.

[9] D. Hisamoto, W.-C. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asano, T.-J. King, J. Bokor, and C. Hu, "A folded-channel MOSFET for deep-sub-tenth micron era," in *Proc. IEDM*, Jun.–Sep. 1998, pp. 1032–1034.

[10] C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyon, H. Liu, R. McFadden, B. McIntyre, J. Neirynck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roesler, J. Sandford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, C. Weber, P. Yashar, K. Zawadzki, and K. Mistry, "A 22 nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," in *Proc. Symp. VLSI Technol.*, 2012, pp. 131–132.

[11] K. Ahmed and K. Schuegraf, "Transistor wars," *IEEE Spectrum*, vol. 48, no. 11, pp. 50–66, Nov. 2011.

[12] G. Wakamatsu, Y. Anno, M. Hori, T. Kakizawa, M. Mita, K. Hoshiko, T. Shioya, K. Fujiwara, S. Kusumoto, Y. Yamaguchi, and T. Shimokawa, "Double patterning process with freezing technique," *Proc. SPIE*, vol. 7273. 2009, p. 72730B.

[13] E. Karl, Z. Guo, Y.-G. Ng, J. Keane, U. Bhattacharya, and K. Zhang, "The impact of assist-circuit design for 22 nm SRAM and beyond," presented at the 2012 Electron Devices Meeting (IEDM).

[14] C.-H. Jan, U. Bhattacharya, R. Brain, S.- J. Choi, G. Curello, G. Gupta, W. Hafez, M. Jang, M. Kang, K. Komeyli, T. Leo, N. Nidhi, L. Pan, J. Park, K. Phoa, A. Rahman, C. Staus, H. Tashiro, C. Tsai, P. Vandervoorn, L. Yang, J.-Y. Yeh, and P. Bai, "A 22 nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications," presented at the 2012 Electron Devices Meeting (IEDM).

[15] S. U. Engelmann, R. Martin, R. L. Bruce, H. Miyazoe, N. C. M. Fuller, W. S. Graham, E. M. Sikorski, M. Glodde, M. Brink, H. Tsai, J. Bucchignano, D. Klaus, E. Kratschmer, and M. A. Guillorn, "Patterning of CMOS device structures for 40–80 nm pitches and beyond," *Proc. SPIE*, vol. 8328. 2012, p. 83280B-1.

[16] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K.

Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, "A 90 nm high volume manufacturing logic technology featuring novel 45 nm gate length strained silicon CMOS transistors," in *Proc. IEDM Tech. Dig.*, 2003, pp. 11.6.1–11.6.3.

[17] P. Bai, C. Auth, S. Balakrishnan, M. Bost, R. Brain, V. Chikarmane, R. Heussner, M. Hussein, J. Hwang, D. Ingerly, R. James, J. Jeong, C. Kenyon, E. Lee, S. H. Lee, N. Lindert, M. Liu, Z. Ma, T. Marieb, A. Murthy, R. Nagisetty, S. Natarajan, J. Neirynck, A. Ott, C. Parker, J. Sebastian, R. Shaheed, S. Sivakumar, J. Steigerwald, S. Tyagi, C. Weber, B. Woolery, A. Yeoh, K. Zhang, and M. Bohr, "A 65 nm logic technology featuring 35 nm gate lengths, enhanced channel strain, 8 Cu interconnect layers, low-k ILD and 0.57μm2 SRAM cell," in *Proc. IEDM Tech. Dig.*, 2004, pp. 657–660.

[18] C. Auth, A. Cappellani, J.-S. Chun, A. Dalis, A. Davis, T. Ghani, G. Glass, T. Glassman, M. Harper, M. Hattendorf, P. Hentges, S. Jaloviar, S. Joshi, J. Klaus, K. Kuhn, D. Lavric, M. Lu, H. Mariappan, K. Mistry, B. Norris, N. Rahhal-orabi, P. Ranade, J. Sandford, L. Shifren, V. Souw, K. Tone, F. Tambwe, A. Thompson, D. Towner, T. Troeger, P. Vandervoorn, C. Wallace, J. Wiedemerand, and C. Wiegand, "45 nm High-k + metal gate strain-enhanced transistors," in *Proc. Symp. VLSI Technol.,* 2008, pp. 128–129.

[19] P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, W. Han, J. He, R. Heussner, R. James, J. Jopling, C. Kenyon, S.-H. Lee, M. Liu, S. Lodha, B. Mattis, A. Murthy, L. Neiberg, J. Neirynck, S. Pae, C. Parker, L. Pipes, J. Sebastian, J. Seiple, B. Sell, A. Sharma, S. Sivakumar, B. Song, A. St. Amour, K. Tone, T. Troeger, C. Weber, K. Zhang, Y. Luoand, and S. Natarajan, "High performance 32 nm logic technology featuring 2nd generation high-k + metal gate transistors," in *Proc. IEDM*, 2009, pp. 1–4.

[20] P. A. Kraus, K. Ahmed, T. C. Chua, M. Ershov, H. Karbasi, C. S. Olsen, F. Nouri, J. Holland, R. Zhao, G. Miner, and A. Lepertl, "Low-energy nitrogen plasmas for 65-nm node oxynitride gate dielectrics: A correlation of plasma characteristics and device parameters," in *Proc. Symp. VLSI Technol., 2003*, pp. 143–144.

[21] S. V. Hattangady, H. Niimi, and G. Lucovsky, "Controlled nitrogen incorporation at the gate oxide surface," *Appl. Phys. Lett*., vol. 66, no. 25, pp. 3495–3497, 1995.

[22] S. V. Hattangady, H. Niimi, and G. Lucovsky, "Integrated processing of silicon oxynitride films by combined plasma and rapidthermal processing," *J. Vac. Sci. Technol. A*, vol. 14, no. 6, pp. 3017–2023, 1996.

[23] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," *J. Appl. Phys.*, vol. 89, no. 10, pp. 5243–5275, 2001.

[24] J.-W. Yang and J. G. Fossum, "On the feasibility of nanoscale triple-gate CMOS transistors," *IEEE Trans. Electron. Devices*, vol. 52, no. 6, pp. 1159–1164, Jun. 2005.

[25] U. E. Avci, R. Rios, K. Kuhn, and I. A. Young, "Comparison of performance, switching energy and process variations for the TFET and MOSFET in logic," in *Proc. Symp. VLSI Technol., 2011*, pp. 124–125.

[26] *International Technology Roadmap for Semiconductors, 2011 Edition: Interconnects*.

[27] D. Edelstein, J. Heidenreich, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, P. Roper, T. McDevitt, W. Motsiff, A. Simon, J. Dukovic, R. Wachnik, H. Rathore, R. Schulz, L. Su, S. Luce, and J. Slattery, "Full copper wiring in a sub-0.25 μm CMOS ULSI technology," in *Proc. IEDM Tech. Dig.,* 1997, pp. 773–776.

[28] W. Steinhogl, G. Schindler, G. Steinlesberger, M. Traving, and M. Engelhardt, "Comprehensive study of the resistivity of copper wires with lateral dimensions of 100 nm and smaller," *J. App. Phys.*, vol. 97, pp. 023706-1–023706-7, 2005.

[29] Y. Au, Y. Lin, H. Kim, E. Beh, Y. Liu, and R. G. Gordon, "Selective CVD of manganese self-aligned capping layer for Cu interconnections in microelectronics," *J. Electrochem. Soc.*, vol. 157, no. 6, pp. D341–D345, 2010.

[30] B. Feldman, S. Park, M. Haverty, S. Shankar, and S. T. Dunham, "Simulation of grain boundary effects on electronic transport in metals and detailed causes of scattering," *Phys. Status Solidi B*, vol. 247, no. 7, pp. 1791–1796, 2010.

[31] G. Beyer, M. Pantouvaki, and Z. Tokei, "Air gaps for interconnects: Ready to go," *Solid State Technol.*, vol. 53, no. 6, pp. 39–40, 2010.

[32] T. Ko, C. L. Chang, S. W. Chou, M. W. Lin, C. I. Lin, C. H. Shih, H. W. Su, M. H. Tsai, W. S. Shue, and M. S. Liang, "High performance/reliability Cu interconnect with selective CoWP cap," in *Proc. Symp. VLSI Technol., 2003,* pp. 109–110.

[33] C.-C. Yang, B. Li, H. Shobha, S. Nguyen, A. Grill, W. Ye, J. AuBuchon, M. Shek, and D. Edelstein, "In Situ Co/SiC(N,H) capping layers for Cu/Low- k interconnects," *IEEE Electron. Device Lett.*, vol. 33, no. 4, pp. 588–590, Apr. 2012.

[34] J. W. Ward, J. Nichols, T. B. Stachowiak, Q. Ngo, and E. J. Egerton, "Reduction of CNT interconnect resistance for the replacement of Cu for future technology nodes," *IEEE Trans. Nanotechnol.*, vol. 11, no. 1, pp. 56–62, Jan. 2012.

[35] R. Murali, K. Brenner, Y. Yang, T. Beck, and J. D. Meindl, "Resistivity of grapheme nanoribbon interconnects," *IEEE Electron. Device Lett.*, vol. 30, no. 6, pp. 611–613, Jun. 2009.

[36] B. Li, Z. Luo, L. Shi, J. P. Zhou, L. Rabenberg, P. S. Ho, R. A. Allen, and M. W. Cresswell, "Controlled formation and resistivity scaling of nickel silicide nanolines," *Nanotechnol.*, vol. 20, p. 085304, 2009.

[37] K. Ha, D. Shin, H. Byun, K. Cho, K. Na, H. Ji, J. Pyo, S. Hong, K. Lee, B. Lee, Y.-H. Shin, J. Kim, S.-G. Kim, I. Joe, S. Suh, S. Choi, S. Han, Y. Park, H. Choi, B. Kuh, K. Kim, J. Choi, S. Park, H. Kim, K. Kim, J. Choi, H. Lee, S. Yang, S. Park, M. Lee, M. Cho, S. Kim, T. Jeong, S. Hyun, C. Cho, J.-K. Kim, H.-G. Yoon, J. Nam, H. Kwon, H. Lee, J. Choi, S. Jang, J. Choi, and C. Chung,"Si-based optical I/O for optical memory interface, *Proc. SPIE*, vol. 8267. 2012, p. 82670F-1.

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