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Cryogenic Small Dimension Effects and Design-Oriented Scalable Compact Modeling of a 65-nm CMOS Technology

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***Abstract*— This paper presents the cryogenic characterization and compact modeling of thin-oxide MOSFETs in a standard 65-nm Si-bulk CMOS technology. The influence of both short and narrow channel effects at extremely low temperature on key device parameters such as threshold voltage and ON current is highlighted, and the performance of this technology node for cryogenic analog circuit design is discussed. It is then demonstrated, for the widest range of gate geometries in literature, that the BSIM4 parameter editing approach can be successfully used to model small dimension effects at cryogenic temperature. In the absence of cryogenic foundry models, the robustness and simplicity of this modeling technique make it a preferred method to quickly build a design-oriented, fully scalable SPICE compact model. This restores complete freedom in device sizing for cryogenic analog circuit design.**

***Index Terms*— Characterization, Circuit simulation, CMOS technology, Cryogenic electronics, Modeling**

I. Introduction

Cryogenic CMOS circuits have become increasingly popular in recent years due to their application in quantum computing [1]. Still, they also find use in a much broader spectrum of applications such as gravitational wave detectors [2]–[4], infrared focal plane arrays, positron emission tomography, and quantum technology in general [5]. Modern thin-oxide devices are usually free of the anomalies that plague thick-oxide devices [6], [7], [9] and can therefore take full advantage of the benefits offered by the cryogenic environment, such as increased transconductance [9] and reduced leakage [15]. However, existing foundry models for CMOS technologies are still unable to reliably reproduce the behavior of MOSFETs at very low temperatures [8]. This also prevents the validation of the few cryogenic design methodologies proposed in the literature [23]. Despite the efforts of many research groups in characterization and modeling [9]–[22], there is no uniquely recognized approach to extract a cryogenic SPICE compact model for a CMOS technology yet. Moreover, the vast majority of works focuses on modeling very few gate geometries, thus severely limiting the degrees of freedom for analog design [24]. An increasingly popular modeling method is to modify model equations by changing the code of the Verilog-A model implementation. This approach has been shown to be sufficiently accurate when scaling the temperature and the size of devices [16], [17]. However, it is prone to errors as for some models (e.g., BSIM4 [25]), there is no official implementation in Verilog-A available. Moreover, the performance of Verilog-A implementations is highly code-dependent [26] and still falls short of SPICE models developed in C and hard-coded in commercial simulators, even when dedicated model compilers are employed [28], [29]. This becomes increasingly problematic as the number of transistors in the circuit increases. To circumvent these limitations, an alternative approach is editing only model parameters, to re-center the model on the target temperature [9], [19]. By retaining the original model code, this method is inherently less error-prone and preserves simulation performance. Furthermore, it allows reusing foundry statistical data for mismatch simulations, albeit to a limited extent [30]. However, to the best of the authors' knowledge, this modeling approach has so far only been applied to a limited number of gate geometries [9], [19]. Therefore, its full scaling capabilities have yet to be demonstrated. In this work, we present the cryogenic performance of a 65-nm Si-bulk CMOS technology and show that the modeling methodology based on BSIM4 parameter editing can be used to obtain a fully scalable cryogenic compact model. Although much of the most recent work in cryogenic device characterization and modeling focuses on nonplanar technologies [17], [18], the 65-nm node is still one of the most used for analog and mixed signal chip design, as demonstrated by the statistics from the latest International Solid State Circuits Conference (ISSCC) shown in Fig. 1.

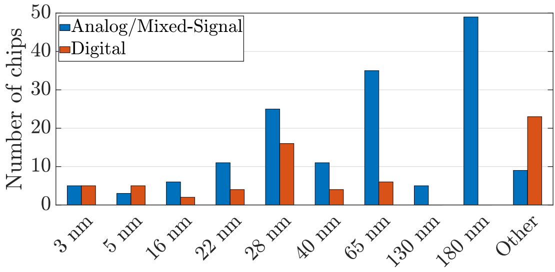

Fig. 1. Number of chips per technology node presented at ISSCC 2024.

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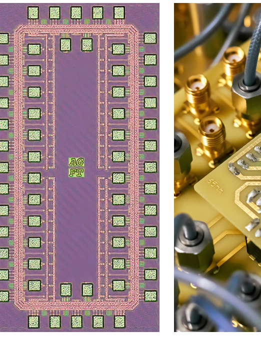
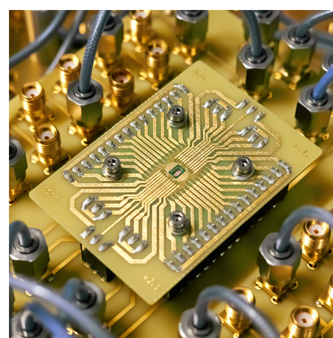
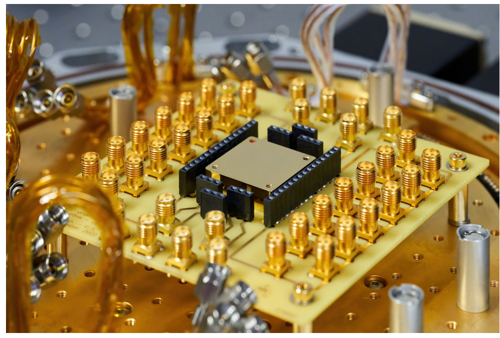
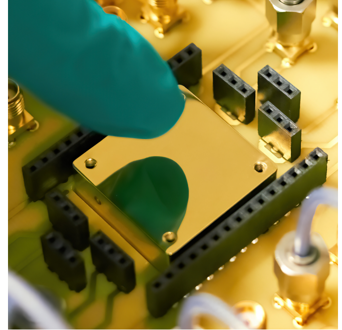
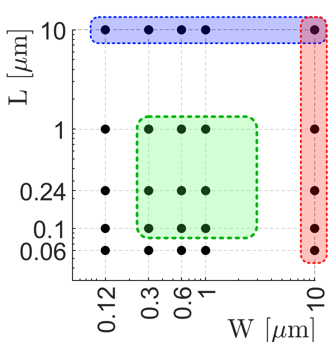





Fig. 2. From left to right: photomicrograph of the test chip; pictures of the sample mounting system employed for the characterization. To ensure the best possible thermal conductivity, the chip is fixed with silver paint on the metal surface of a gold-plated OFHC copper heatsink, placed in direct contact with a cold finger of the same material [32]. Sample temperature is measured with a Cernox® SD thermometer [33] on the chip heatsink.



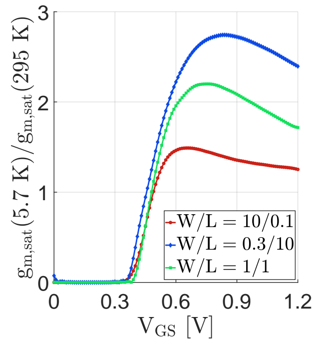


Fig. 3. Left: gate geometries of the test structures. Devices usually used to characterize short and narrow channel effects are highlighted in red and blue respectively. The green rectangle in the middle encompasses the gate geometries commonly of interest for analog circuit design [24]. Right: the glaring differences in relative increase of the saturation transconductance $\mathbf{g_{m,sat}}$ for three different NMOS geometries.

The paper is organized as follows: Section II describes the test structures and the measurement setup; Section III discusses the cryogenic behavior, with a focus on the impact of small dimension effects; Section IV discusses the cryogenic performance of the technology for analog circuit design; Section V presents the modeling procedure and the accuracy of the resulting model; finally, conclusions are drawn in Section VI.

II. Test Structures, Setup and Measurements

Low-threshold voltage (LVT) MOSFETs ($t_{ox} \approx 2.7$ nm) with 25 different gate geometries for both PMOS and NMOS (50 devices in total) were fabricated in a 65-nm Si-bulk CMOS technology. LVT devices were selected because of the known threshold voltage increase at cryogenic temperature [9], [12]. The chosen geometries, shown in the left side of Fig. 3, cover the entire design space available in the foundry PDK. The test transistors are divided into groups that share gate, source, and bulk terminals, while the drain terminals are independent to ensure accurate subthreshold current characterization. The interconnections are designed so that the impact of the overall series resistance on the measurements is negligible. The connections to the pads are made almost entirely of ultra-thick metal ($R \approx 5\text{m}\Omega/\square$ at room temperature) or thick metal ($R \approx 25\text{m}\Omega/\square$ at room temperature). These values are expected to reduce further at cryogenic temperature. The devices are positioned so that those with the largest aspect ratio W/L have the shortest connections to the pads. With these measures, the error on V_{DS} is always below 0.5%. To ensure that the measurements genuinely represented the process, all test dies were diced from a wafer certified as typical-typical (TT) by the foundry.

The samples were bonded directly to a PCB designed for cryogenic low-current measurements, with guarding [31] down to pad level, and placed in the cryogenic chamber of a Montana Instruments s200 cryostation, modified to extend the guarding along standard coaxial feedthroughs. A custom sample mounting system for in-vacuum cryogenic chip testing, depicted in Fig. 2, was employed to ensure proper thermalization of the samples [32]. The complete test setup achieves a base temperature of 5.7 K. Measurements were conducted with an array of four Keithley 2450 SMUs, connected with triaxial cables and triax-to-coax adapters [31] to the feedthroughs of the cryogenic chamber.

The characterization includes transfer characteristics ($I_D - V_G$) in linear ($|V_{DS}|$ = 50 mV) and saturation ($|V_{DS}|$ = 1.2 V) regions, and output characteristics ($I_D - V_D$) for multiple $|V_{GS}|$ values. Each measurement was repeated for several $|V_{BS}|$ for body-effect characterization. Devices were tested at room (T = 295 K) and cryogenic (T = 5.7 K) temperatures. This allowed to verify the correct operation by comparing room temperature measurements with simulations, enabling the rejection of any possibly damaged devices.

III. Experimental Results

In agreement with previous literature in the field, the test devices showed an overall increase in threshold voltage, a steep increase in subthreshold slope (SS), resulting in a reduction of more than three orders of magnitude in leakage, and a marked increase in transconductance due to increased free carrier mobility at cryogenic temperature [9]–[12]. The variation of electrical parameters with temperature is strongly dependent on channel length and width. The right side of Fig. 3 and the I-V characteristics of Fig. 4 clearly show how the gate geometry affects both the increase in transconductance and drive current at cryogenic temperature. No kink effect [9] was observed, in contrast to previous reports using both the same technology [34] and more recent nodes [35].

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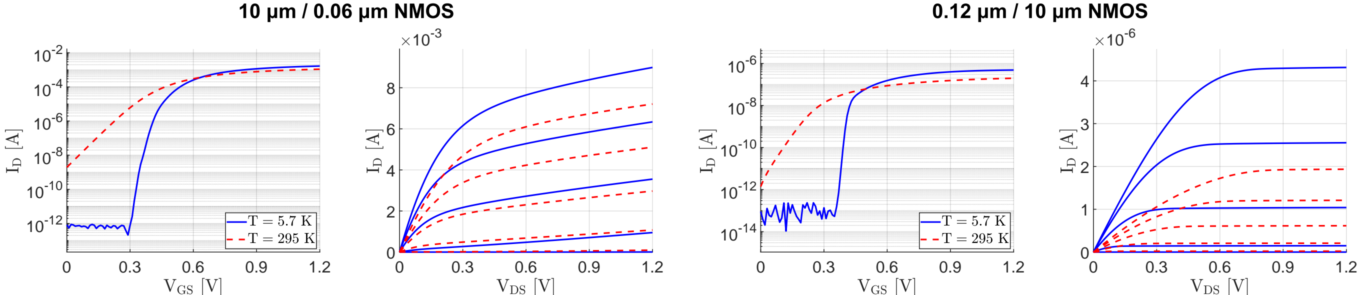

Fig. 4. Transfer characteristics with $\mathbf{V_{DS} = 50\,mV}$ and output characteristics for a wide/short (left) and a narrow/long (right) NMOS device. For the output characteristics, $\mathbf{V_{GS}}$ was stepped from 0.3 V to 1.2 V with a constant step size.

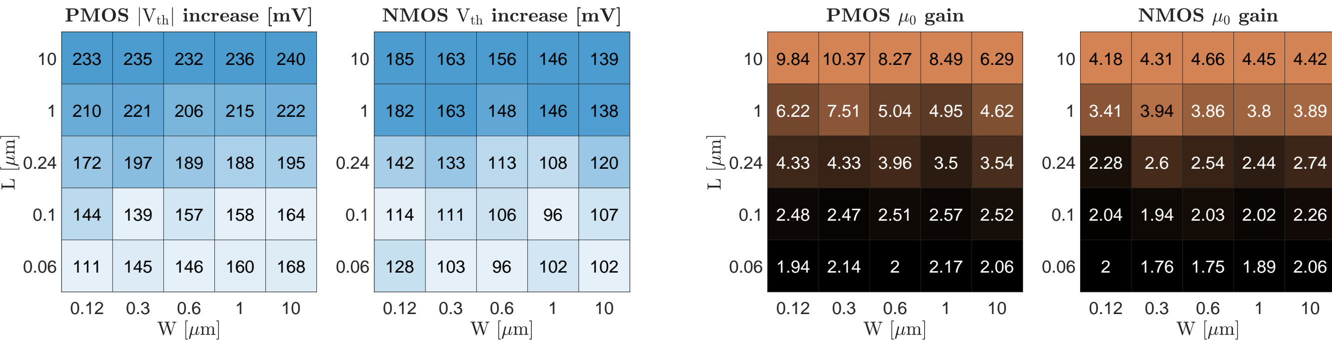

Fig. 5. Increase in threshold voltage $\mathbf{V_{th}}$ and low-field mobility $\mathbf{\mu_0}$ at cryogenic temperature. The gain in $\mathbf{\mu_0}$ is defined as the ratio $\mathbf{\mu_0(5.7K)/\mu_0(295K)}$. Both $\mathbf{V_{th}}$ and $\mathbf{\mu_0}$ were extracted using the Y-function method [36] with $|\mathbf{V_{DS}}| = \mathbf{50\,mV}$. Darker shades indicate less desirable cryogenic variations.

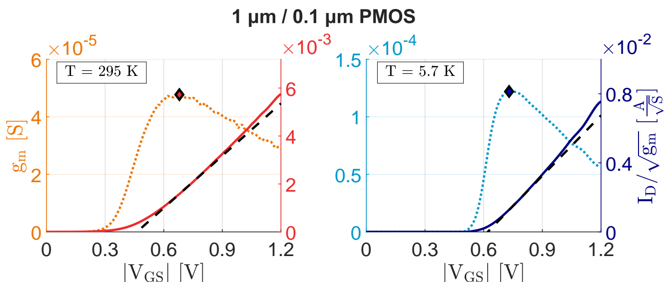

Fig. 6. Transconductance $\mathbf{g_m}$ for $|\mathbf{V_{DS}}| = \mathbf{50\,mV}$ (dotted lines) and Y-function [36] $\mathbf{I_D/\sqrt{g_m}}$ for a sample device, in both temperature conditions. Markers indicate the peak $\mathbf{g_m}$ point used for the extraction. Dashed lines indicate the linear approximation at the extraction point.

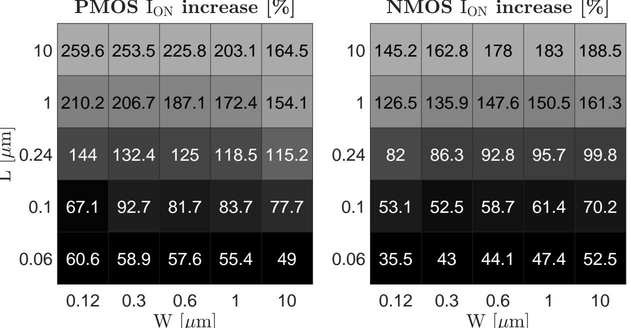

Fig. 7. Device ON current increase at cryogenic temperature. The ON current is defined as the maximum $|\mathbf{I_D}|$ for $|\mathbf{V_{DS}}| = \mathbf{50\,mV}$ and $|\mathbf{V_{BS}}| = \mathbf{0\,V}$. The increase is calculated as $|[\mathbf{I_{ON}(5.7K)} - \mathbf{I_{ON}(295K)}]/\mathbf{I_{ON}(295K)}| \cdot \mathbf{100}$. Darker shades indicate less desirable cryogenic variations.

Figure 5 shows the increase in threshold voltage V_{th} and in low-field mobility μ_0 (both extracted with the Y-function method [36]) at cryogenic temperature, for all fabricated gate geometries. It is worth noting that the extraction for thin oxide devices is complicated by the impact of mobility degradation due to surface scattering, which at cryogenic temperature becomes even more prominent and contributes to the bell-shaped appearance of the gate voltage dependence of mobility [37], [38]. Mobility becomes then a nonhomographic function of gate voltage [40], [41], thus limiting the applicability of extraction by Y-function to only the range of V_{GS} voltages in which it remains linear, as depicted in Fig. 6. Nevertheless, the effectiveness of this method for low-field mobility extraction of nanoscale devices at cryogenic temperature has been demonstrated before [21]. To corroborate the results and also gain more information about the impact of gate geometry, Fig. 7 adds information on the ON current increase. This allows to directly observe the correlation with the increase in V_{th} and mobility, thus consolidating the extraction results.

As previously reported for other technologies, short channel effects (SCE) have a larger impact on the threshold voltage at cryogenic temperature [19], also due to the weakening of the reverse short channel effect (RSCE) [42]. In contrast to room temperature conditions, however, at cryogenic temperature this has a positive effect on device operation since it limits the shift of V_{th} as channel length decreases. Unfortunately, as can be seen from Fig. 8, the cryogenic increase of V_{th} is still dominant and can become problematic, especially for PMOS devices. On the other hand, the impact of the reverse narrow

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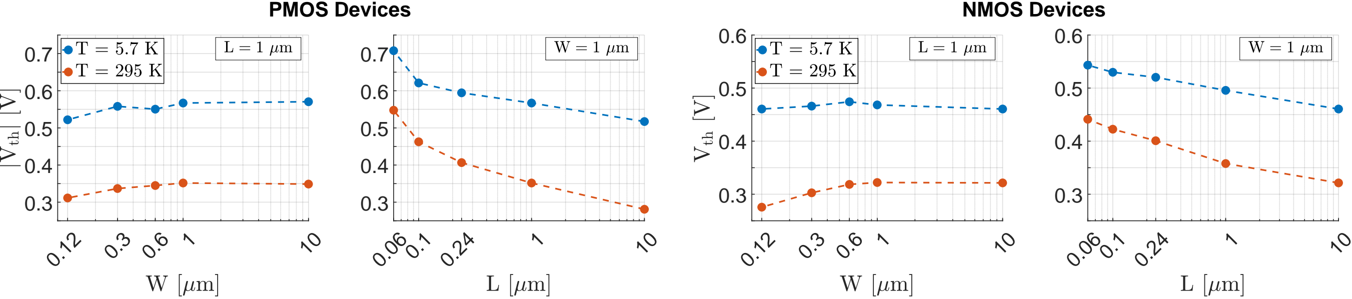

Fig. 8. Impact of short channel effects and reverse narrow channel effect on threshold voltage for both temperature conditions. $\mathbf{V_{th}}$ values extracted with the Y-function method at $|\mathbf{V_{DS}}| = \mathbf{50\ mV}$.

width effect (RNWE, i.e., the decrease in V_{th} for smaller W) [43] at cryogenic temperature is significantly suppressed for long NMOS devices, but shows little temperature dependency for long PMOS devices. The impact of channel width on V_{th}, however, appears to change as the channel length is reduced. In fact, short-channel PMOS devices seem to benefit from a smaller increase in threshold voltage as the channel narrows, while the opposite seems to happen for NMOS. This trend is also confirmed by the different increase in ON current (Fig. 7) for the minimum length devices, despite their insubstantial change in mobility gain with channel width. The mobility gain in these devices, in fact, is clearly dominated by the well-known mobility collapse for short channels and its weak temperature dependence [44], [45]. This behavior of V_{th} for short channel devices could then be attributed to the complex interactions between three-dimensional carrier scattering [15] and shallow trench isolation (STI) stress effects that occur in the device as the channel shrinks [46], [47], as the latter are enhanced by the significant thermal expansion/contraction at low-temperature [30]. This hypothesis is supported by the fact that STI stress is known to have an opposite impact on electron and hole mobility and a more pronounced channel width dependence in PMOS [48], which can also explain the opposite trend in long channel PMOS and NMOS for both the mobility and the ON current increase as the channel width is reduced. Further investigation with dedicated test structures would be needed for a complete evaluation of the STI stress behavior at cryogenic temperature.

Drain-induced barrier lowering (DIBL) and drain-induced threshold shift (DITS) [25] were characterized with the constant current method [50] and a normalized current $I_D/(W/L)$ equal to 100 nA. Both effects showed a very weak temperature dependence for this technology, as visible in Fig. 9.

The competing effects of threshold voltage and mobility at cryogenic temperature also have an impact on the output conductance g_o, which can be extracted from the output I-V characteristics. The increase in mobility seems to prevail when the devices are in strong inversion, resulting in a generally higher output conductance at cryogenic temperature. This corresponds to an overall reduction in output resistance $r_o = 1/g_o$, visible in Fig. 10, which in turn counterbalances the benefit of a larger saturation g_m (see again Fig. 3) for the intrinsic gain of the device.

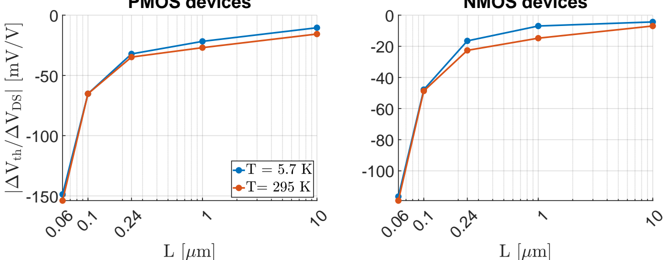

Fig. 9. DIBL (DITS for long channel) impact on $\mathbf{V_{th}}$ for both PMOS and NMOS devices. $\mathbf{W = 10 \mu m}$ for all the data points.

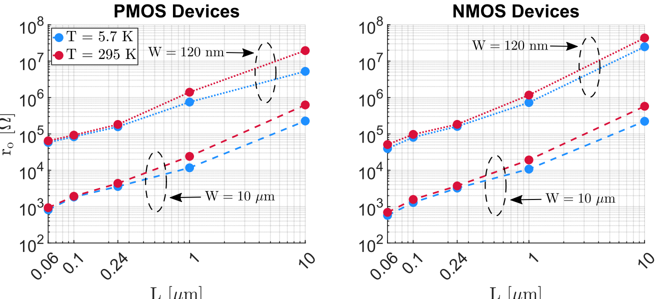

Fig. 10. Extracted saturation output resistance values in strong inversion ($|\mathbf{V_{GS}}| = |\mathbf{V_{DS}}| = \mathbf{0.9\ V}$) for several gate geometries.

IV. Technology Performance Metrics

Although essential for modeling, the characterization of physical parameters such as V_{th} and mobility does not allow to get directly valuable information about the performance of a technology at cryogenic temperature for circuit design. For this purpose, it is much more enlightening to use some of the figures of merit commonly used in analog design. To get a better view of the overall cryogenic performance, the following discussion is divided into saturation and linear region.

A. Saturation

A widely popular analog design methodology is based on the transconductance efficiency g_m/I_D [24]. To use the g_m/I_D methodology in this performance evaluation, the geometry in Fig. 11 is considered, being a common choice for gate fingers in this technology node [24]. It should be noted that such a gate geometry is almost exclusively affected by short channel effects. Because of the significant increase of g_m/I_D at cryogenic temperature in weak inversion [11], a fair comparison

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between the two temperature conditions based on the inversion level is not trivial. For this reason, Fig. 11 depicts the extracted g_m/I_D as a function of the overdrive voltage V_{OV}, in order to establish a link between the cryogenic and room-temperature values of g_m/I_D. In this analysis, the subthreshold region is excluded as the impact of mismatch makes biasing in weak inversion an undesirable choice at cryogenic temperature [30]. For the PMOS of Fig. 11, as an example, the subthreshold swing (1/SS) drops to about 12 mV/dec when the device is cooled down. This means that a variation of 10 mV on V_{th} will cause an error on the subthreshold current of almost one decade.

With reference to Table I, if the transistor is biased just outside the weak inversion region ($V_{OV} = 50$ mV), g_m/I_D at cryogenic temperature becomes significantly higher than at room temperature. Moving the bias point towards strong inversion ($V_{OV} = 200$ mV), however, causes the cryogenic g_m/I_D to drop rapidly, reaching values slightly lower than at room temperature. This aspect has already been reported in literature [9] and is a direct consequence of the enhanced impact of the vertical field-induced mobility degradation [17].

TABLE I
PERFORMANCE METRICS FOR A PMOS DEVICE WITH $\mathbf{W/L = 1\ \mu m/0.24\ \mu m}$

		g_m/I_D $[V^{-1}]$		I_D/W [A/m]	
		295 K	5.7 K	295 K	5.7 K
$*$	$\lvert V_{OV}\rvert = 50$ mV	21.4	34.6	0.9	1.9
□	$\lvert V_{OV}\rvert = 100$ mV	16.8	20.2	2.6	8.7
◊	$\lvert V_{OV}\rvert = 200$ mV	9.7	8.3	10.4	37.9

Symbols correspond to the markers in Fig. 11.

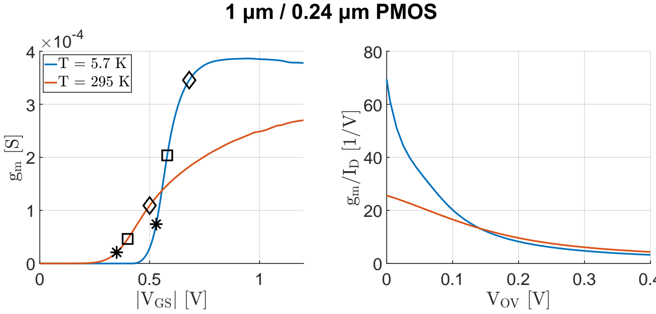

Fig. 11. Analog FoMs for a PMOS test device in saturation with $\mathbf{W/L = 1\ \mu m/0.24\ \mu m}$. Left: transconductance $\mathbf{g_m}$ in saturation; markers correspond to the different bias conditions listed in Table I. Right: transconductance efficiency $\mathbf{g_m/I_D}$ versus overdrive voltage $\mathbf{V_{OV} = |V_{GS} - V_{th,sat}|}$, where $\mathbf{V_{th,sat}}$ is the threshold voltage in saturation (extracted with the constant current method).

The current density I_D/W at cryogenic temperature is significantly higher than at room temperature for all three bias points. The difference from room temperature increases with the overdrive voltage, reaching an almost four times increase in strong inversion. Unfortunately, this means that keeping the same bias point (i.e. the same V_{OV}), from cryogenic temperature to room temperature, will lead to an increase in power consumption. Conversely, at constant current (constant I_D/W), the operating point will shift towards weak inversion as the temperature drops, leading to an increase in g_m/I_D and thus an increase in the transconductance g_m, as shown in Fig. 11. Considering that the gate-related capacitances are virtually insensitive to temperature [11], [16], the device will show a similar increase in its transit frequency f_T [24].

However, it should be noted that this shift of the bias point has a direct consequence on the design of low-power circuits. In optimizing power consumption at room temperature, in fact, biasing at or just above subthreshold is widely exploited [51]. By keeping the current (and thus power consumption) constant in the transition from room temperature to cryogenic temperature, the bias point will shift into deep weak inversion, incurring variability problems as highlighted above. This greatly complicates the optimization of low power circuits for a wide temperature range. A possible solution to this issue is to exploit the body terminal to compensate for the variations in V_{th}, as already proposed in literature for room temperature [52]. However, maintaining the bias in deep moderate inversion at cryogenic temperature is preferable to obtain a good compromise between matching and efficiency. This bias point has also been previously suggested as the optimal point for the design of cryogenic RF LNAs [53].

TABLE II
ON RESISTANCE PER UNIT WIDTH FOR A MINIMUM-LENGTH NMOS

	295 K	5.7 K
$V_{GS} = 0.6$ V	$2031.2\ \Omega \cdot \mu m$	$3118.6\ \Omega \cdot \mu m$
$V_{GS} = 0.9$ V	$716.2\ \Omega \cdot \mu m$	$488.8\ \Omega \cdot \mu m$
$V_{GS} = 1.2$ V	$502.3\ \Omega \cdot \mu m$	$326.6\ \Omega \cdot \mu m$

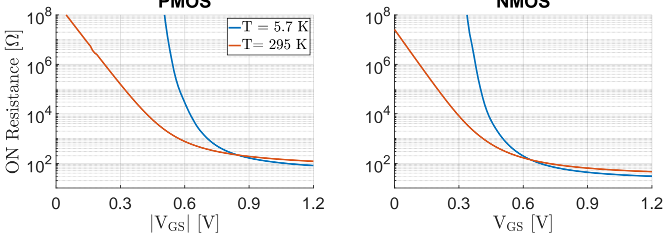

Fig. 12. Extracted ON resistance for a PMOS and NMOS transistor versus the applied $\mathbf{V_{GS}}$. $\mathbf{W/L = 10\ \mu m/60\ nm}$ for both devices.

B. Linear region

The most common use of the MOSFET transistor in linear region is as a switch. For this reason, the cryogenic performance in linear region can be evaluated using the ON resistance of the switch. Table II shows the values of ON resistance per unit gate width of a minimum length NMOS transistor, for three different values of V_{GS}.

From the values shown in the table, it is evident that the cryogenic increase in mobility results in better MOS switches only when the switch turn-on voltage is sufficiently high. For $V_{GS} = 0.6$ V, in fact, the resistance per unit width is larger at cryogenic temperature, so the switch behavior is clearly dominated by the increase in V_{th}.

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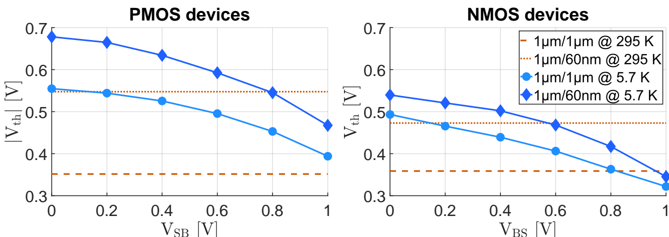

Fig. 13. Threshold voltage for $|\mathbf{V_{DS}}| = \mathbf{50\,mV}$ (extracted with the Y-function method) at different levels of body biasing. Dashed lines indicate the extracted $\mathbf{V_{th}}$ at room temperature with no body effect.

Figure 12 shows the ON resistances for a PMOS and NMOS of a given size. For the PMOS device, given the larger increase in $\mathrm{V_{th}}$ at cryogenic temperature and the fairly limited gain in mobility due to the short channel (see also Fig. 5), the minimum voltage required to exceed the performance at room temperature is even higher. Using complementary transmission gates, therefore, does not bring substantial benefits.

This counter-intuitive aspect of cryogenic switch performance can force design compromises in critical blocks, resulting in higher power consumption [54]. For both high-precision and high-speed applications, circuit techniques such as bootstrapping [55] should be used to circumvent this problem. Another technique that can be effectively used to deal with the increase in $\mathrm{V_{th}}$ is the forward body biasing (FBB) [56]. By taking advantage of the increased turn-on voltage of parasitic diodes at cryogenic temperature, it is indeed possible to use the body terminal as a back-gate, similar to FDSOI technologies, without incurring large increases in leakage currents to the substrate. As shown in Fig. 13, in fact, the FBB technique allows to considerably reduce the threshold voltage, bringing $\mathrm{V_{th}}$ even below its nominal value at room temperature. However, the application of FBB appears to be less effective on long channel PMOS devices. While for the NMOS it is always possible to bring $\mathrm{V_{th}}$ below the room temperature value, the long PMOS suffers from both a much greater increase in $\mathrm{V_{th}}$ at cryogenic temperature (see Fig. 5) and a lower FBB effectiveness.

V. Modeling and Simulation

Similarly to most previous works in the literature [9]–[19], the modeling effort in this work focuses on the device DC characteristics. This is not a limitation for using the model for analog and mixed-signal circuit design, since MOSFET gate capacitances in inversion are practically independent of temperature [11], [16], [58], [59].

In developing the model, temperature scaling was ignored, since 1) the temperature is stable and well controlled in the target environments (cryogenic chambers), and 2) the properties of Si nanoscale CMOS devices do not change significantly for $T < 50$ K [15], [21], [57].

The modeling procedure begins by extracting the target model card from the library in the foundry PDK. The binning in the original model card is exploited to generate a *point model* for each of the measured devices. A custom modeling flow for cryogenic parameter extraction and optimization, depicted in Fig. 14, is then applied *to each point model* in order to re-center it on the cryogenic measurement data.

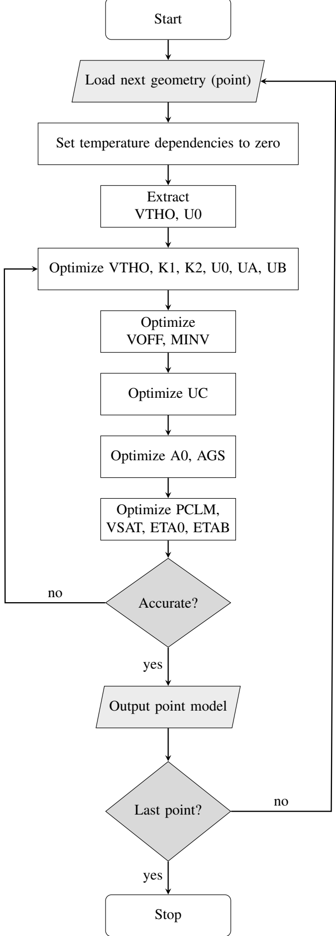

Fig. 14. Simplified cryogenic modeling flow diagram for the individual gate geometries (points). The point models used in this flow are generated starting from the foundry binning and, after being processed with the flow, they are subsequently used to re-build the original binning.

At the beginning of this process, temperature dependencies are set to zero [9], as they lead to a considerable error in the estimation of the parameters at cryogenic temperature (see Fig. 17). The parameters that most influence device behavior are those related to threshold voltage, mobility and bulk charge effect [49]. Therefore, the flow focuses primarily on these parameters. A complete list of parameters used in the flow is given in Tab. III. The simulation temperature for parameter optimization is set to T = -220°C to match the (average) subthreshold slope, as the BSIM4 model is not able to represent the SS deviation at cryogenic temperature [11].

The optimization steps in Fig. 14 should minimize the error on a weighted combination of both the I-V curves and their derivatives (e.g., $\mathrm{g_{ds}} = \partial \mathrm{I_D}/\partial \mathrm{V_{DS}}$) [46]. A standard Levenberg-Marquardt algorithm can be used for curve fitting. However, since there are many combinations of parameters that can lead to essentially the same quality of model fit on the measured data, care must be taken in the optimization steps. The parameter values should always be limited within reasonable ranges. Physical parameters, in particular, should show values similar to those resulting from direct extractions

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TABLE III
LIST OF BSIM4 MODEL PARAMETERS EDITED IN THE FLOW

Parameter	Description
VTHO	Long-channel threshold voltage at $V_{BS} = 0$
K1	First-order body bias coefficient
K2	Second-order body bias coefficient
U0	Low-field mobility
UA	Coefficient of first-order mobility degradation
UB	Coefficient of second-order mobility degradation
UC	Coefficient of mobility degradation due to body-bias
VSAT	Saturation velocity
A0	Coefficient of L dependence of bulk charge effect
AGS	Coefficient of V_{GS} dependence of bulk charge effect
KETA	Body-bias coefficient of bulk charge effect
VOFF	Offset voltage in subthreshold region for large W and L
MINV	V_{gsteff} fitting parameter for moderate inversion condition
ETA0	DIBL coefficient in subthreshold region
ETAB	Body-bias coefficient for the sub-threshold DIBL effect
PCLM	Channel length modulation parameter
RDSW	Zero-bias LDD resistance per unit width

on measurement data.

The overall output of this flow is a set of re-centered cryogenic point models, which are then used to rebuild a single cryogenic model card with binning. At this stage, the model can be further optimized with measurement data, if necessary. The use of binning also provides additional degrees of freedom for fitting and allows the normal scaling capabilities of BSIM4 to be extended [46].

This binned cryogenic model card is then compared with the original one, and the differences in the target parameters are applied to the latter. The modified model code is finally used to overwrite the corresponding section in a copy of the foundry library, thus obtaining a modified version that can be used for cryogenic analog circuit design and simulation.

The model obtained with this procedure shows a good fit of the experimental data, visible in Figs. 15, 16 and 17. As shown in Fig. 15, the re-centered model manages to simulate with satisfactory accuracy the body effect at cryogenic temperature, including forward body biasing. It is therefore possible to evaluate the use of this promising technique in simulation. The RMS errors in Fig. 16 are defined as follows [60]:

$$\text{Error}_{\text{RMS}}\ [\%] = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(\frac{X_{\text{meas}} - X_{\text{sim}}}{\max\{|X_{\text{meas}}|, |(X_{\text{sim}}|\}}\right)^2} \quad (1)$$

where X is the quantity of interest (e.g. the drain current). Normally, a fit is considered of excellent quality if the RMS error is below 2% [60]. Although the standard BSIM4 model is clearly not a good candidate for a physically rigorous cryogenic model, the re-centered model constitutes an effective rapid enabler to cryogenic circuit simulation and considerably reduces the foundry model error, which for some geometries can be of more than 200%.

Finally, it is important to note that re-centering the parameters in the modeling procedure in Fig. 14 alters only their nominal value, leaving the statistical changes applied to the parameter unaffected. This allows the modified model to retain mismatch simulation capabilities. Although the results obtainable with the modified model provide only an estimate, they still allow a qualitative assessment that would otherwise be impossible. Even considering resorting to the foundry model only for this type of simulation, the results would not be representative at all because of the shift in the operating point discussed in the previous section.

As an example, Table IV shows the results of a Monte Carlo simulation with 1000 iterations of the circuit in Fig. 18. The strong deterioration of matching in weak inversion due to the steep slope of the subthreshold current, visible in Fig. 18, is very clear from the simulation results.

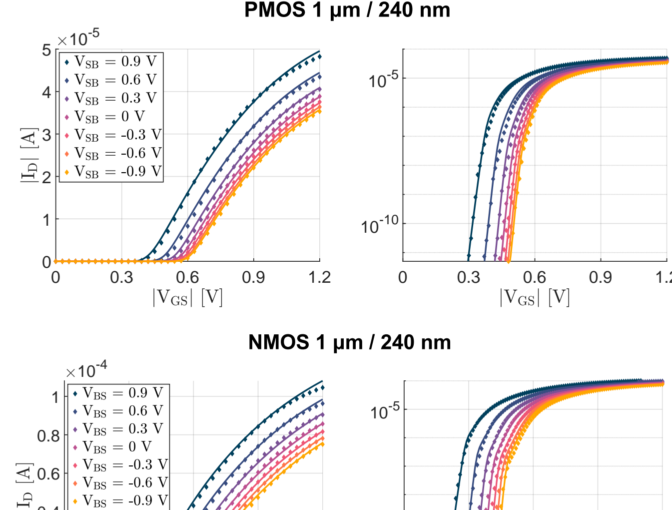

Fig. 15. $\mathbf{I_D - V_G}$ transfer characteristics in linear and logarithmic scale for two sample devices with $|\mathbf{V_{DS}}| = \mathbf{50\ mV}$ and different body biases. Markers: measurement data at $\mathbf{T = 5.7\ K}$. Lines: simulation with the re-centered model ($\mathbf{T_{SIM} = -220°C}$).

TABLE IV
MONTECARLO SIMULATION RESULTS FOR THE NMOS CURRENT MIRROR OF FIG. 18

Simulation temperature	27°C		-220°C	
	I_{REF}	σ_{IOUT}	I_{REF}	σ_{IOUT}
Weak inversion	300 nA	17.4 nA	10 nA	4.6 nA
Moderate inversion	10 µA	0.38 µA	30 µA	1.6 µA
Strong inversion	150 µA	1.8 µA	500 µA	6.1 µA

The operating points are shown in Fig. 18.

VI. CONCLUSION

The cryogenic characterization of a 65-nm Si-Bulk CMOS technology was presented, highlighting the impact of gate geometry effects on the device behavior at cryogenic temperature. The performance of the technology in the context of analog circuit design was discussed. Although the cryogenic environment offers advantages such as the marked increase in transconductance, it also poses challenges for the circuit designer. A design-oriented, robust modeling procedure was proposed, which allows to obtain a fully scalable cryogenic compact model with simple BSIM4 parameter re-centering.

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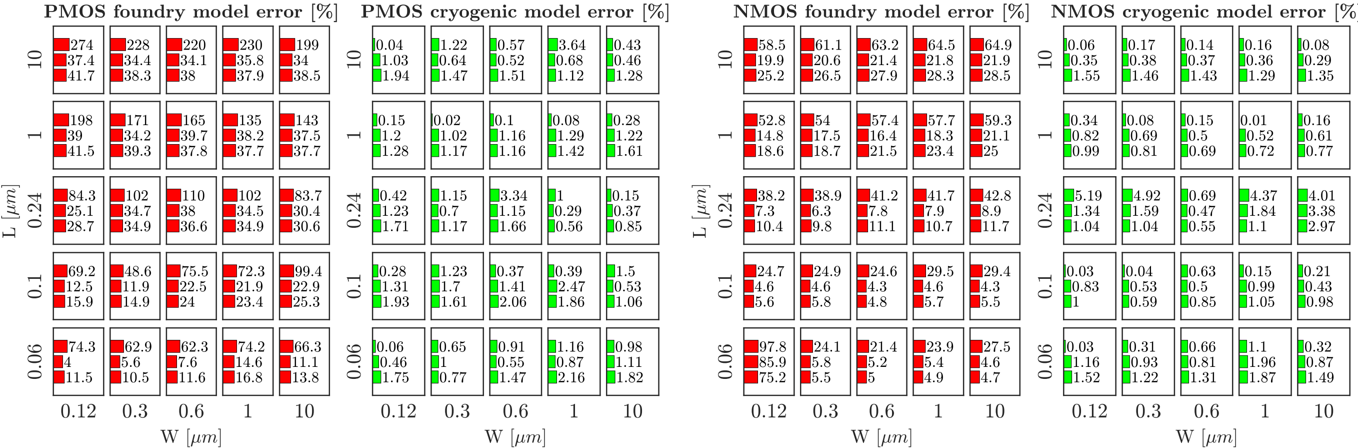

Fig. 16. Accuracy of the foundry model and the cryogenic model for both PMOS and NMOS. For each device, starting from the topmost error bar: 1) error on $\mathbf{I_{ON}}$, defined as the maximum $|\mathbf{I_D}|$ for $|\mathbf{V_{DS}}| = \mathbf{50\ mV}$ and $\mathbf{V_{BS}} = \mathbf{0\ V}$; 2) average RMS error on the $\mathbf{I_D}$-$\mathbf{V_{GS}}$ characteristics in saturation, for $|\mathbf{V_{DS}}| = \mathbf{1.2\ V}$ and several values of $\mathbf{V_{BS}}$; 3) average RMS error on the $\mathbf{I_D}$-$\mathbf{V_{DS}}$ characteristics for several values of $\mathbf{V_{GS}}$.

Fig. 17. Cryogenic measurement data versus simulations for the four corner NMOS geometries. From top to bottom: $\mathbf{I_D} - \mathbf{V_G}$ transfer characteristics in logarithmic and linear scale for $\mathbf{V_{DS}} = \mathbf{50\ mV}$; output $\mathbf{I_D} - \mathbf{V_D}$ characteristics for several values of $\mathbf{V_{GS}}$; transconductance $\mathbf{g_m}$ in saturation ($\mathbf{V_{DS}} = \mathbf{1.2\ V}$); output conductance $\mathbf{g_{ds}}$ in saturation for three different $\mathbf{V_{GS}}$ voltages (foundry model data omitted due to extremely large error). Data points in linear scale are decimated. Measurement temperature $\mathbf{T} = \mathbf{5.7\ K}$. Simulation temperature $\mathbf{T_{SIM}} = \mathbf{-220°C}$.

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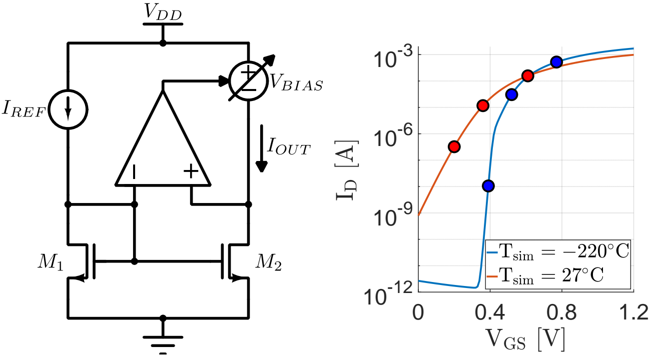

Fig. 18. Left: testbench circuit used for Montecarlo simulations. Transistors M_1 and M_2 are sized identical, $\mathbf{W/L = 6\ \mu m/0.6\ \mu m}$. The ideal feedback loop equalizes the voltage at the two drain terminals. Right: the operating points chosen for the local mismatch simulations.

The proposed approach can be applied to any nanoscale CMOS technology using a model that lacks a Verilog-A official implementation, or another way to access the model equations directly. This improves the design possibilities of cryogenic analog and mixed-signal circuits.

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