1-Mbit 3D DRAM using a Monolithically Stacked Structure of a Si CMOS and Heterogeneous IGZO FETs

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***Abstract*—We present a three-dimensional (3D) DRAM prototype, which is formed using oxide semiconductor FETs (OSFETs) monolithically stacked on a Si CMOS. The OSFETs are composed of a one-layer planar FET and two-layer vertical FETs (VFETs). The 1T1C memory cells in the VFET layers and a primary sense amplifier in the planar FET layer, which are formed using heterogeneous OSFETs, provide various circuit functions in the DRAM. The operation of the 3D DRAM in a 1-Mbit memory array is demonstrated for the first time. The results show that the proposed DRAM operates with read and write times of 60 ns and 50 ns, respectively. The leakage current of the memory cell is extremely low (comparable to an 2.2 × 10^{-19} A/cell at 85°C), indicating that over 99% of the data are retained in the memory array after one hour at 85°C without refresh.**

***Index Terms*—Extremely low off-state current, heterogeneous OSFETs, monolithic stacking, oxide semiconductor (OS), planar FET, vertical FET, 1T1C.**

I. INTRODUCTION

IMPROVEMENTS in the CPU and GPU performance in the era of IoT and AI have increased the amount of processed data. This necessitates the need for wide-bandwidth memories. Large-capacity memories, such as the high-bandwidth memory and the hybrid memory cube, where DRAM dies are connected using a through-silicon via (TSV), have attracted attention because of their ability to achieve wide bandwidths. However, the pitch of a TSV is quite large (of the micrometer order), and thus the bus width is limited [1], [2]. Additionally, although the frequency of memory access must be increased when processing massive data, a low-power memory is necessary [3] for the reduction of the power consumed due to memory access. The one oxide semiconductor (OS) FET–one capacitor (1OS1C) DRAM [4] is a low-power memory employing an OS FET (OSFET), which typically includes In–Ga–Zn–O (IGZO) as an OS. This memory can retain charge stored in the cell capacitor for a long time by utilizing, as an access transistor, the OSFET having an ability to exhibit an extremely low off-state current. Furthermore, as shown in the concept image of Fig. 1, the OSFET can be formed in a Si CMOS back end of line (BEOL) and directly connected to a Si circuit under the OSFET through a via. In a DRAM employing OSFETs (OS DRAM), as shown in Fig. 1(b), many sense amplifier (SA) circuits formed using Si FETs can be placed under a 1OS1C memory array formed in an OS layer. This configuration reduces the number of memory cells connected to a bit line (BL); additionally, it reduces the physical length of BLs. This technology leads to a decrease in the BL capacitance (C_{bl}), resulting in a small cell capacitance (C_s) [5], [6]. In addition, in the OSFET stacking technology, the memory and the Si circuits can be connected through vias; accordingly, many connections can be easily formed, and a wide bandwidth can be achieved. As other OS technologies, a technique of monolithically stacking OS layers [7], [8] and FETs using vertically formed channels (VFETs) [9], [10], [11], [12], [13] have also been reported. In this paper, we propose a three-dimensional (3D) DRAM, which is a developed form of the 1OS1C DRAM. In the proposed DRAM, heterogeneous OSFET layers are monolithically stacked to form vertically stacked memory cells.

The rest of the paper is organized as follows. Two types of OSFET device structures and the proposed layer structure of a 3D OS DRAM are presented in Section II. The electrical characteristics of OSFETs in each layer are presented in Section III, and a circuit diagram of the 3D OS DRAM is presented in Section IV. The chip measurement results are presented in Section V. Finally, Section VI concludes the paper.

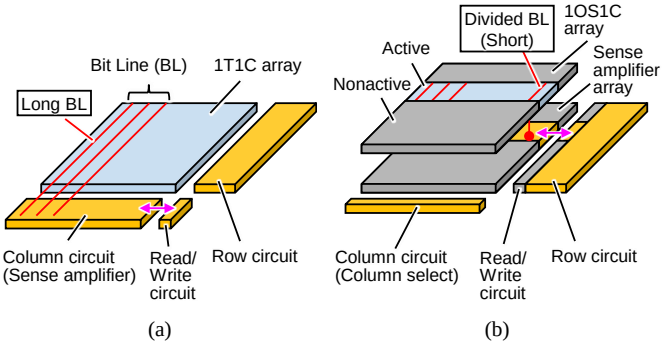

Fig. 1. Concept image of an OS DRAM.

II. Structure of OSFETs and 3D OS DRAM

Since an OSFET can be formed in a Si BEOL, many OSFET layers can be stacked [7], [8]. In this study, two types of OSFETs with different structures are formed in a Si BEOL. The first type is a planar FET, as shown in Fig. 2. The planar FET has a shape similar to that of previously reported OSFETs and has been used in various applications [14], [15], [16], [17]. The planar FET includes a bottom gate (BG) electrode and a top gate (TG) electrode; the threshold voltage (V_{th}) of the planar FET can be controlled by varying the BG voltage [7]. Although the planar FET with a channel length L = 60 nm and a channel width W = 60 nm is used in a prototype chip in this paper, L and W can be varied, and its characteristics can be optimally tuned to perform a specific circuit function.

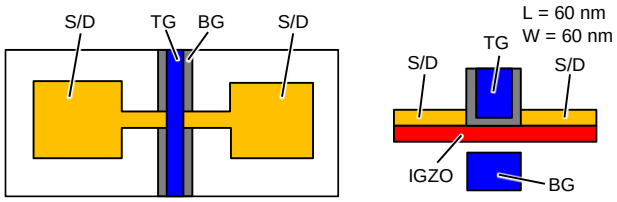

Fig. 2. Planar FET structure.

The second type of OSFET used in the proposed 3D OS DRAM is a VFET with a vertical channel. The VFET can be used in various applications such as display backplanes [11] and LSIs [12]. Fig. 3(a) shows the proposed VFET structure. Fig. 4 shows the process flow of the VFET. The VFET has a structure in which a spacer, which is formed of an insulating film, is sandwiched between source/drain (S/D) electrodes. The spacer has a thickness corresponding to L. The VFET in the prototype has a spacer thickness (= L) of 40 nm. A channel hole penetrates through the top S/D electrode and the spacer, and IGZO is formed on the inner wall of the channel hole. Additionally, a gate-insulating film and a gate electrode are formed in the hole, resulting in a TG structure. The channel hole is positioned at the intersection of the gate metal and the S/D metal. In this study, the VFET is applied to a 1T1C (1OS1C) memory cell by forming a 3D metal–insulator–metal (MIM) below the VFET, as shown in Fig. 3(b); the cell area of this structure is a $4F^2$ square layout. The bottom S/D electrode of the VFET also serves as the upper electrode of the 3D MIM, enabling a simple connection between the VFET and the 3D MIM.

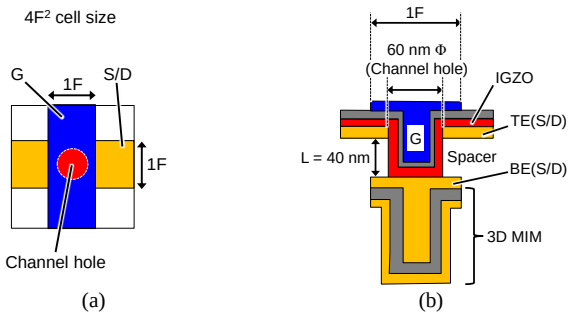

Fig. 3. VFET and 3D MIM structures.

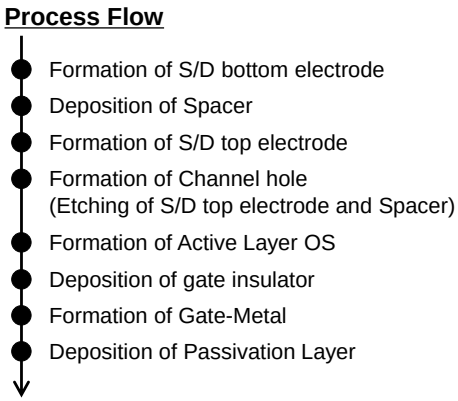

Fig. 4. VFET process flow.

The layers of the two OSFET types are monolithically stacked to form a 3D OS DRAM. Fig. 5 shows the layer structure of the 3D OS DRAM, where three OS layers are monolithically stacked on a Si CMOS. The planar FET, which is a four-terminal device with two gate electrodes TG and BG, is formed in the first OS layer (control circuit layer: OS-CL). As mentioned earlier, the OSFET V_{th} can be controlled by varying the BG voltage. The planar FET is used in the first SA circuit. In the second and third OS layers (memory layers: OS-ML1, OS-ML2), VFETs and 3D MIMs are employed to form 1OS1C memory cells. Using the OS technology, optimal OS structures can be combined to perform the intended circuit function.

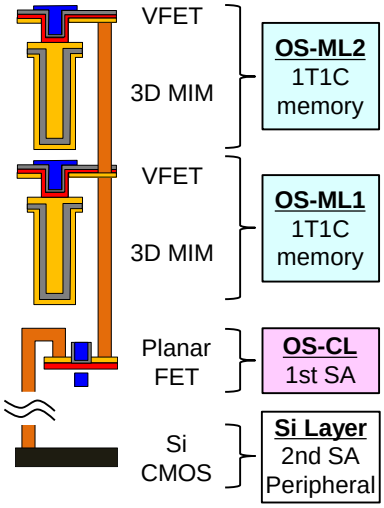

Fig. 5. Stacked structure of a 3D OS DRAM.

III. Characteristics of the Two OSFET Types

Fig. 6 shows the static characteristics of the OSFETs. Fig. 6(a) shows the I_d–V_{tg} curves (V_{tg}: TG voltage) of the planar FET (OS-CL). V_{th} of the planar FET can be adjusted by varying the BG voltage (V_{bg}), and the planar FET can be driven by V_{bg} optimized for the intended circuit function. Figs. 6(b) and (c) show the I_d–V_g curves of the VFETs in the OS-ML1 and OS-ML2, respectively. The top and bottom S/D electrodes of the

VFETs are asymmetric, and the electric field from the gate is different between the top and bottom S/D electrodes; thus, the I_d–V_g curves differ, depending on the current flow direction. The VFETs in both OS-ML1 and OS-ML2 exhibit almost identical characteristics.

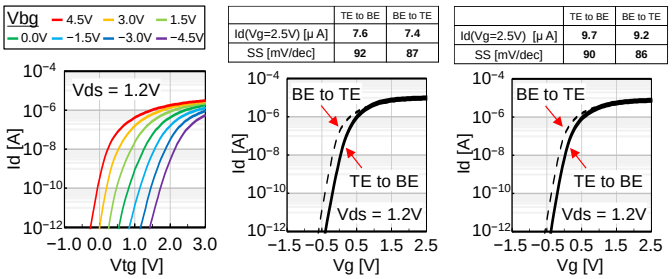

Fig. 6. Static characteristics of (a) a planar FET (OS-CL), (b) a VFET (OS-ML1), and (c) a VFET (OS-ML2); BE: bottom electrode, TE: top electrode.

Fig. 7 shows the leakage current characteristics of a planar FET (OS-CL). An OSFET shows an extremely low off-state current. This current was measured using the method reported in [13], [18] and estimated using an Arrhenius plot to be 1.6×10^{-21} A/FET at room temperature (27°C). Fig. 8(b) shows the VFET and 3D MIM leakage currents in the memory cell shown in Fig. 8(a). Using an Arrhenius plot, we estimated the 3D MIM and VFET leakage current values (5.2×10^{-21} A/Cell and 1.5×10^{-22} A/Cell), respectively, at room temperature (27°C). The 3D MIM leakage current is higher than the VFET leakage current. In other words, if the variation of the 3D MIM leakage current is small, the leakage current variation of the entire memory cell can be suppressed, even when the VFET leakage current varies. As shown in Fig. 8, the leakage current in this memory cell is extremely small; thus, the data can be retained in a node SN for a long time. Fig. 9 shows the voltage variation of the node SN as a function of the retention time, assuming that the memory cell leakage current is constant. The amount of voltage variation at the node SN in the memory cell, including the VFET, after 1000 s was estimated at 45 mV at 85°C and 1 mV at 27°C. A Si FET cell with a leakage current $I_{leak} = 10^{-15}$ A and a capacitance C_s = 10 fF was used as a reference. The amount of voltage variation at the node SN in the cell after 1 s was estimated at 900 mV, indicating difficulties in long-term data retention.

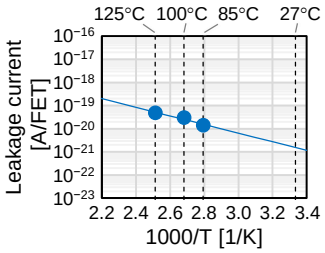

Fig. 7. I_{off} characteristics of a planar FET.

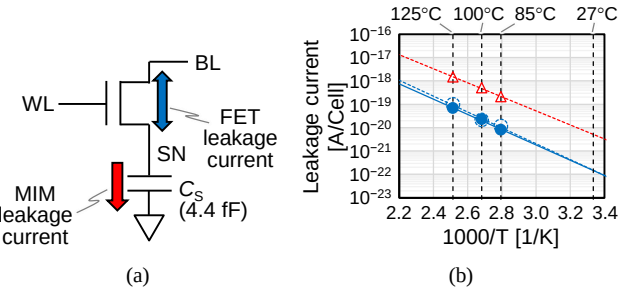

Fig. 8. (a) Circuit and (b) I_{off} characteristics of the formed memory cell; WL: word line, BL: bit line, SN: storage node.

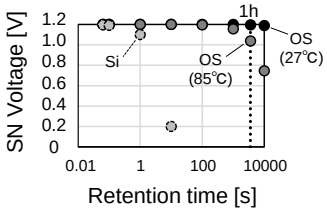

Fig. 9. SN voltage variation as a function of the retention time without performing a refresh operation estimated from the off-state Si FET and OS VFET currents; these currents were calculated for the OS using the circuit and cell leakage currents (at 27°C and 85°C) shown in Fig. 8 and for Si assuming $C_s = 10$ fF and $I_{leak} = 10^{-15}$ A.

IV. 3D OS DRAM Design

A. 3D OS DRAM Circuit Diagram

In this section, we present the structure of a 1-Mbit 3D OS DRAM prototype, which is illustrated in Fig. 10. The structure includes 32 memory subarrays arranged in a row direction. Each memory subarray has a 32-kbit memory capacity; thus, the capacity of the full DRAM is 1 Mbit. Each memory subarray consists of 1024 memory SA blocks (MS blocks). 32 2nd SA arrays are placed in parallel in a row direction in the Si CMOS layer, and a 2nd SA array in a specific row is activated in response to the input row address. Other blocks in the Si CMOS layer include memory peripheral circuits such as a row driver, a column driver, a controller, and a W/R driver. The 1st SA is formed using the planar FETs in the OS-CL, and the 1T1C (1OS1C) memory array is formed in the OS-ML1 and OS-ML2.

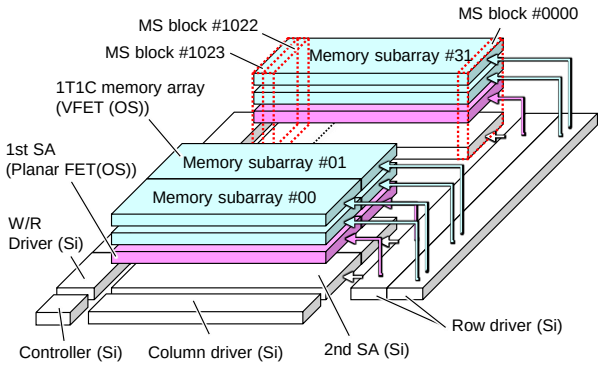

Fig. 10. Block diagram of the full 1-Mbit 3D DRAM.

Fig. 11 presents the circuit diagram of an MS block. The MS block includes the 2nd SA, which is formed using Si FETs. Above the 2nd SA, eight MS subblocks are monolithically stacked; the 2nd SA and the MS subblocks are connected through a global BL (GBL) and an inverted global BL (GBLB). GBL is divided into GBL1 and GBL2 by a BL switch (BLS), and four MS subblocks are connected to GBL1. Each MS subblock consists of one 1st SA and four 1T1C (1OS1C) memory cells (Fig. 12). Data stored in a cell capacitor are read to a local BL (LBL) due to charge sharing. The 1st SA outputs data corresponding to the voltage of LBL to GBL. The voltage output to GBL is susceptible to the V_{th} variation of a read FET (MR) shown in Fig. 12; thus, V_{th} compensation (V_{th}-CP) is desirably performed on the MR before a reading operation. The V_{th}-CP is described in Section IV.*B*.

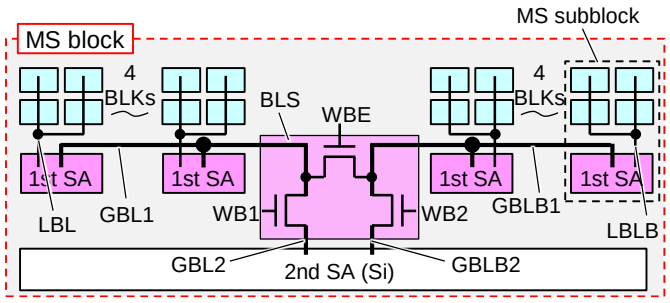

Fig. 11. Circuit diagram of an MS block.

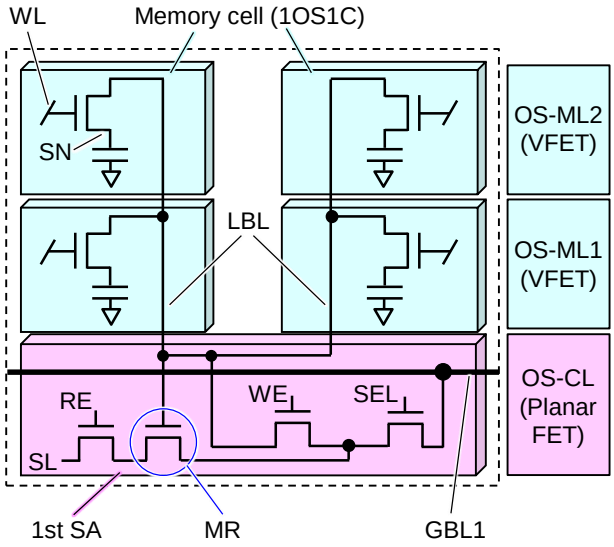

Fig. 12. Circuit diagram of an MS subblock.

According to the 3D OS DRAM design concept, any number of memory layers (OS-ML) can be stacked; however, a large number of stacked layers increases the number of cells connected to a BL; accordingly, C_{bl} increases. In turn, a large C_{bl} requires a large C_s. The proposed 3D OS DRAM inhibits C_{bl} from increasing by dividing BL with the 1st SA positioned between the 2nd SA (Si) and the memory layers (OS-ML), as stated in this paper. As shown in Fig. 13, a GBL connected to the 2nd SA (Si) can be divided into four LBLs through the 1st SA (OS). This structure reduces the number of memory cells connected to the LBL and therefore reduces C_{bl}. Fig. 14 shows layout excerpts of the memory subarray. Each GBL and the wiring for other signals are routed through a wiring layer placed between the 2nd SA and the 1st SA. The two OS-MLs can have the same layout.

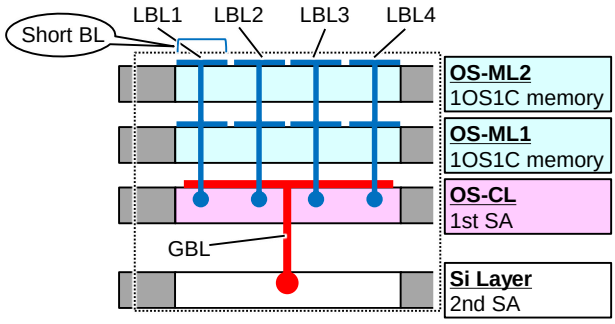

Fig. 13. BL division in the 3D OS DRAM.

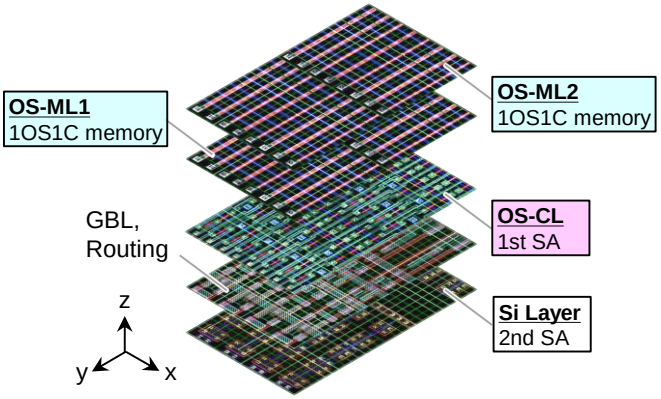

Fig. 14. Layout of the 3D stacked structure (excerpt of the memory subarray).

B. 3D OS DRAM Timing Diagram

Here, we describe the operation mechanism of the 3D OS DRAM. Fig. 15 shows a timing diagram of the reading operation. As described above, it is desirable to perform V_{th}-CP on the MR before a reading operation is performed. V_{th}-CP is performed in two phases: (i) LBL precharge and (ii) LBL discharge. In the LBL precharge phase (i), SEL and WE are brought to the high level; accordingly, LBL is precharged to the high level. Then, in the LBL discharge phase (ii), RE and WE are set to the high level; accordingly, LBL is discharged to a source line (SL). During this time, the LBL voltage is saturated at the SL voltage V_{SL} + V_{th} (MR). In this way, V_{th}-CP can be performed. Subsequently, similar to the DRAM, the word line is set to the high level; accordingly, charge sharing (iii) between C_s and the LBL capacitance (C_{lbl}) is performed, and the data in the memory cell are read to LBL. After charge sharing, this circuit performs the 1st read (iv) using the 1st SA to output the data corresponding to the voltage of LBL to GBL (GBL1 and GBL2). At the end of the reading operation, amplification (AMP) (v) is performed by the 2nd SA (Si); accordingly, the data are read to the 2nd SA. Since the 1st SA can be regarded as a common source in the 1st

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read phase (iv), the inverted data are output to the GBL in the AMP phase (v). The time required for the 1st read phase (iv) is defined as the read time. The three phases of LBL precharge (i), LBL discharge (ii), and charge sharing (iii) are necessary to perform the reading operation. As shown in Figs. 7 and 8, the off-state currents of the planar FET and VFET, respectively, are extremely low. The LBL, which is the node surrounded by the planar FET and the four VFETs, is in a floating state and can retain a voltage for a long time when the peripheral OSFETs are all in the off state. Hence, by performing LBL precharge (i), LBL discharge (ii), and charge sharing (iii) at any time before the reading operation, the LBL voltage can be retained for a long time, and the 1st read (iv) can start at the desired time.

Fig. 16 shows a timing diagram of the writing operation, where the writing operation is performed after the reading operation, specifically, after the 1st read (iv) and AMP (v) phases. We assume a case where the memory on the GBL side is accessed and the low-level data are retained in the node SN in the reading operation. Initially, in AMP phase (v), the GBL voltage is brought to the high level, which corresponds to the inverted data of the SN data. Next, in the write-back phase (vi), the BLS connection is changed; accordingly, the connection between GBL and GBLB changes, and the original low-level data are written back to the node SN. In the writing phase (vii), the written data are supplied by the 2nd SA. The GBL voltage is inverted, and the high-level data are written to the node SN. Then, in the precharge phase (viii), GBL and GBLB are precharged.

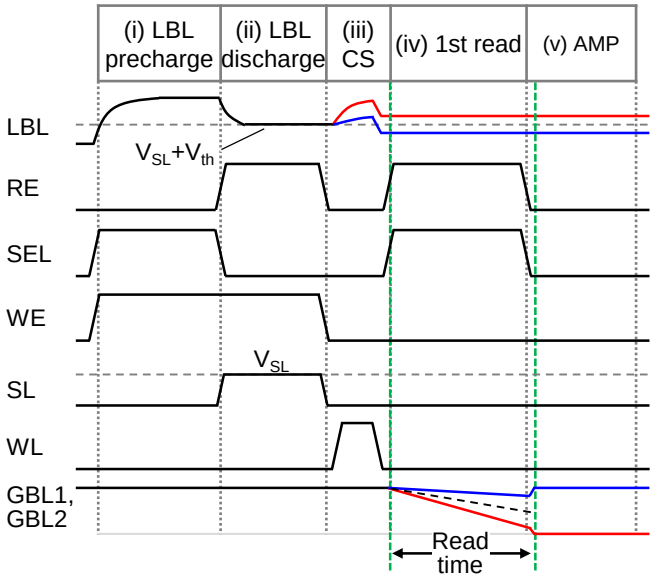


Fig. 15. Timing diagram of the reading operation (CS: charge sharing).

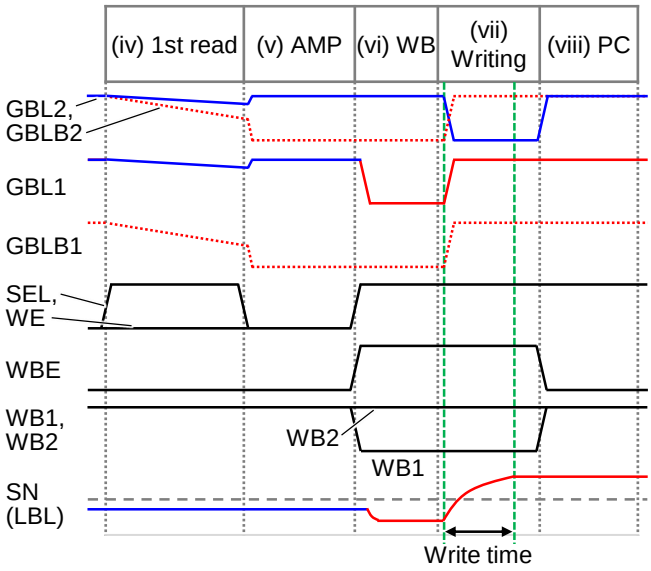


Fig. 16. Timing diagram of the writing operation (AMP: amplification, WB: write back, PC: precharge).

V. Measurement Results

In this section, we present a chip prototype and measurements results. Fig. 17 shows a 3D OS DRAM prototype, which was fabricated using a hybrid process. We employed foundry-manufactured 130-nm Si FETs combined with in-house 60-nm OS FETs. Fig. 18 shows a cross-sectional photograph of the whole fabricated 3D OS DRAM, and Fig. 19 shows enlarged cross-sectional photographs of single memory cells. As shown in Figs. 18 and 19, six wiring metal layers were placed on a Si layer, and three OS layers were monolithically stacked on the metal layers. Both types of OSFETs (planar FETs and VFETs) can be formed in a Si BEOL.

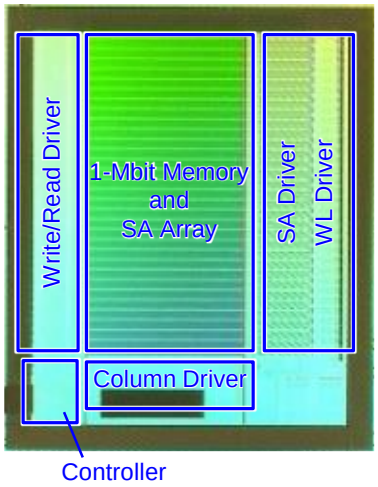


Fig. 17. Die photograph of the fabricated 1-Mbit 3D DRAM.

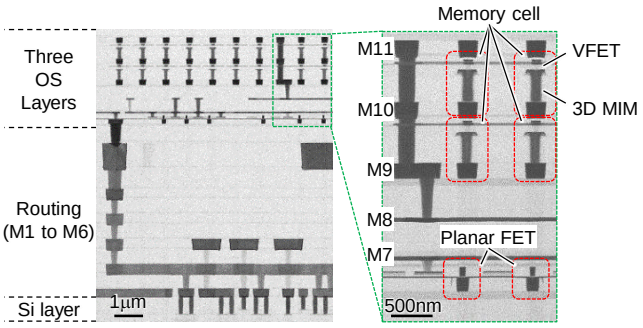
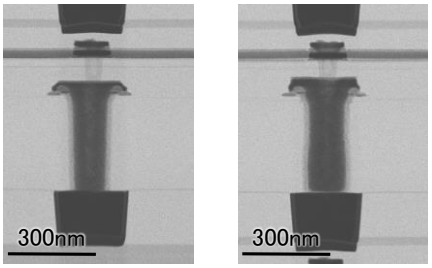


Fig. 18. Cross-sectional photograph of the whole fabricated 3D OS DRAM.



(a) (b)

Fig. 19. Enlarged cross-sectional photographs of single memory cells in (a) OS-ML1 and (b) OS-ML2.

As described earlier, since the 1st SA shown in Fig. 12 is susceptible to the V_{th} variation of MR, V_{th}-CP can be desirably performed on MR. Fig. 20 shows that after performing V_{th}-CP, the initial error was reduced by 92.7%. As shown in Fig. 21, the 3D OS DRAM prototype can operate with a 60-ns read time and a 50-ns write time. The chip prototype also exhibits favorable data retention characteristics. Fig. 22 shows the data retention characteristics of the fabricated 1-Mbit 3D OS DRAM. Since the leakage current is significantly small in the memory cell, including the VFET and the 3D MIM, long-term data retention in the node SN can be achieved. The proposed 3D OS DRAM retains over 99% of data after 1 h at 85°C and exhibits favorable retention characteristics.

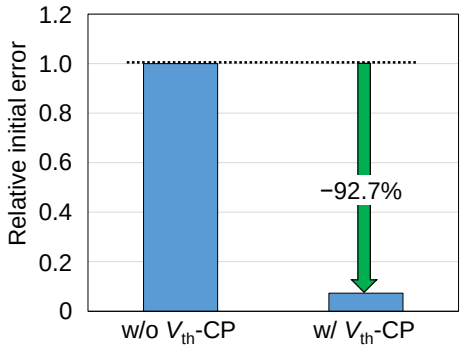
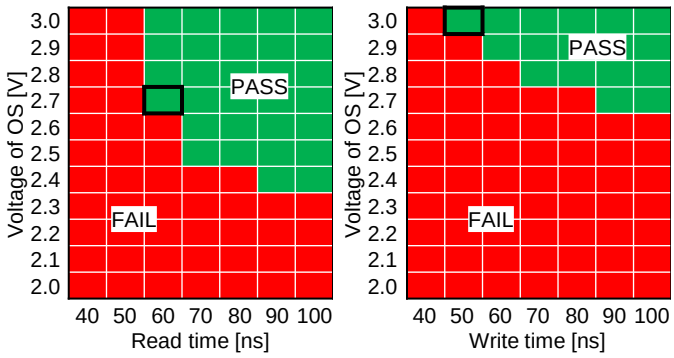


Fig. 20. Initial error reduction after performing V_{th}-CP.



(a) (b)

Fig. 21. Shmoo plots of the (a) reading and (b) writing operations.

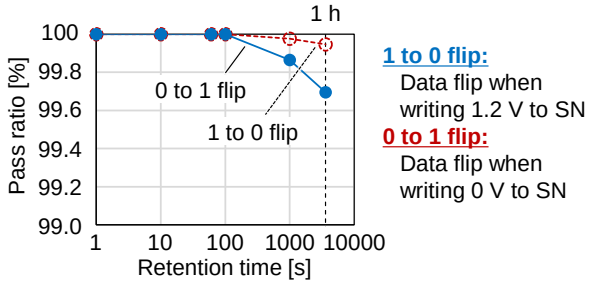


Fig. 22. Data retention characteristics of the fabricated 1-Mbit 3D DRAM.

In TABLE I, we compare the memory proposed in this work with other OS memories. Although a planar FET and a VFET, each including an OS as a channel material, have been reported in the literature [4], [19], [10], monolithically stacked heterogeneous OSFETs employing a planar FET and VFETs have not been reported. For the first time, we present the operation of a special 1-Mbit memory array to demonstrate that the 3D stacked memory chip prototype can perform the expected operations.

TABLE I
COMPARISON OF THE PROPOSED MEMORY WITH OTHER OS MEMORIES

	VLSI 2017 [4]	IEDM 2020 [19]	IEDM 2022 [10]	This work
Technology	OS 60 nm, Si 55 nm	OS	OS	OS 60 nm, Si 130 nm
Layer Structure	Planar FET (OS) Si CMOS	Planar FET (OS)	VFET (OS)	VFET (OS) VFET (OS) Planar FET (OS) Si CMOS
Cell Type	1OS1C	2OS0C	2OS0C	1OS1C
Stacking Structure	1 OS layer is stacked over Si CMOS	No stacking	No stacking	3 OS layers are stacked over Si CMOS
Cell size	2.9 μm²	NA	NA	0.66 μm²
Capacity	1 Mbit	Single cell	Single cell	1 Mbit
# of cells/BL	4	-	-	4/16 (LBL/GBL)
Voltage	Si: 1.2 V OS: 3.3 V	NA	NA	Si: 1.2 V OS: 3.0 V
Read time	10 ns	NA	NA	60 ns
Write time	10 ns	NA	NA	50 ns
Retention	1 h	400 s	190 s	1 h

VI. Conclusion

We present a 3D OS DRAM prototype, which is formed using OSFETs monolithically stacked on a Si CMOS. The 3D OS DRAM is composed of heterogeneous OSFETs, that is, a one-layer planar FET and two-layer VFETs. The DRAM prototype operates with read and write times of 60 ns and 50 ns, respectively. Furthermore, using OSFETs with extremely low off-state currents enables over 99% of data to be retained after one hour at 85°C without a refresh operation. The proposed structure decreases parasitic C_{bl}, which influences charge sharing, resulting in a small C_s. Therefore, stacking layers of this structure can increase the cell density while keeping the 3D MIM low in height.

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