A Physical Charge-based Analytical Threshold Voltage Model for Cryogenic CMOS Design

Hao Su, Yiyuan Cai, Shenghua Zhou, Guangchong Hu, Yu He, Yunfeng Xie, Yuhuan Lin, Chunhui Li, Tianqi Zhao, Jun Lan, Wenhui Wang, *Student Member, IEEE*, Wenxin Li, Feichi Zhou, Xiaoguang Liu, *Senior Member, IEEE,* Longyang Lin, *Senior Member, IEEE,* Yida Li, *Senior Member, IEEE*, Hongyu Yu, *Senior Member, IEEE, and* Kai Chen, *Member, IEEE*

***Abstract*—This paper proposes a physical charge-based analytical MOSFET threshold voltage model that explicitly incorporates interface-trapped charges which have been identified as playing a dominant role in defining threshold voltage trends in deep cryogenic temperatures. The model retains standard threshold voltage definition by various charges across the MOSFET capacitor while being analytical in its form, therefore, suitable for cryogenic CMOS VLSI design. Consequently, a model covering each and all above characteristics is proposed for the first time. Excellent fit between the model and measurement data from 180-nm bulk foundry devices is shown from room temperature to 4 K.**

***Index Terms*—bulk CMOS, threshold voltage, cryogenic, analytical, compact, universal, model, interface traps.**

I. INTRODUCTION

TO address the challenges in quantum computing in cryogenic temperature regime [1]–[3], the temperature-dependent threshold voltage $V_{th}(T)$ of metal-oxide-semiconductor field-effect transistor (MOSFET) down to cryogenic temperature has been characterized [4]–[15] and remodeled [16]–[25] for cryogenic CMOS chip design in recent research. Among physical effects such as dopant freezeout on Fermi potential [24], [26]–[28], metal-semiconductor work function difference [16], field-assisted dopant ionization on depletion charges [17], [29], [30], as well as bandgap variation with temperature. Although the Fermi potential is what governs the overall $V_{th}(T)$ behaviors over temperature, it is also known that the interface-trapped charges dominate the saturating or kicking-up trend towards deep cryogenic temperature [31]–[36].

Several attempts have been made to model the temperature behavior of $V_{th}(T)$ down to 4 K regime [16], [18], [19], and different modeling strategies have been taken as summarized in Table I. It shows that a $V_{th}(T)$ model that both explicitly incorporates interface-trapped charges dominant in defining deep cryogenic behaviors of $V_{th}(T)$ and follows the standard definition by charges across the MOSFET capacitor, C_{ox}, is still unavailable, not to mention an analytical one that is needed for cryogenic CMOS chip design.

TABLE I
COMPARISON OF DIFFERENT MODELING STRATEGIES TOWARDS CRYOGENIC THRESHOLD VOLTAGE $V_{TH}(T)$

Serial No.	Items	This Work	[16]	[18]	[19]
1	Explicitly incorporates interface-trapped charges	Yes	Yes	No	No
2	Standard $V_{th}(T)$ definition by charges across MOS capacitor	Yes	Yes	No	Yes
3	Unified $V_{th}(T)$ equation for both N- & P-MOSFETs while retaining the physical meaning of C_{ox}	Yes	No	Yes	No
4	An analytical expression for compact modeling	Yes	No	Yes	Yes

To model interface-trapped charges explicitly, a Gaussian distribution as a function of energy near the band edge [33], [37] is assumed [16]. However, this $V_{th}(T)$ model was only applicable to N- and one type of P-MOSFET that tend to saturate in deep cryogenic temperature as illustrated in Fig. 1(a) and (b), labeled as "N-type" and "P-type I", respectively. It failed to capture the $V_{th}(T)$ behavior of the other type of P-MOSFET that kicks-up abruptly in deep cryogenic temperature, labeled as "P-type II" in Fig. 1(b). Table II summarizes additional literature results in this respect. The two different $V_{th}(T)$ behaviors specific to P-MOSFETs reported to date may be attributed to different processes proprietarily developed worldwide.

The $V_{th}(T)$ model in [16] does not capture the two different types of $V_{th}(T)$ behaviors specific to P-MOSFETs in deep cryogenic temperature. Additionally, the error function term $erf(T)$ is not an analytical solution, compromising computing efficiency for VLSI design.

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Hao Su, Yiyuan Cai, Yunfeng Xie, Yuhuan Lin, Jun Lan, Wenhui Wang, Wenxin Li, Feichi Zhou, Xiaoguang Liu, Longyang Lin, Yida Li, Hongyu Yu are with the School of Microelectronics, Southern University of Science and Technology, Shenzhen 518055, China.

Kai Chen is with the School of Microelectronics, Southern University of Science and Technology, Shenzhen 518055, China, and also with Shenzhen Institute for Quantum Science and Engineering, Southern University of Science and Technology, Shenzhen 518055, China (e-mail: chenk6@sustech.edu.cn).

Guangchong Hu is with International Quantum Academy, Shenzhen 518048, China.

Shenghua Zhou and Yu He are with Shenzhen Institute for Quantum Science and Engineering, Southern University of Science and Technology, Shenzhen 518055, China, and also with International Quantum Academy, Shenzhen 518048, China and Guangdong Provincial Key Laboratory of Quantum Science and Engineering, Southern University of Science and Technology, Shenzhen 518055, China.

Chunhui Li and Tianqi Zhao are with Institute for Quantum Science and Engineering, Southern University of Science and Technology, Shenzhen 518055, China.

In order to model both types of $V_{th}(T)$ behaviors specific to P-MOSFETs as illustrated in Fig. 1(b), an empirical term $C_{ox,eff}(T)$ was proposed to replace the physical C_{ox} [16]. However, this both losses the physical meaning of standard definition of threshold voltage by charges across C_{ox} and complicates the engineering process of parameter extraction when generating a Process Design Kit (PDK).

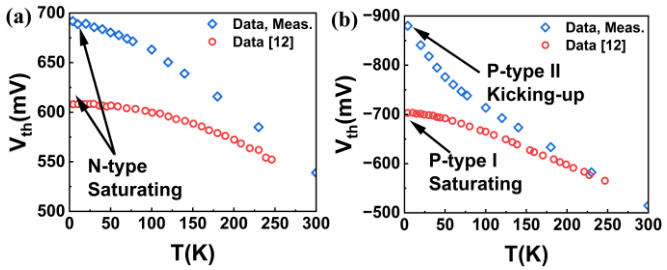

Fig. 1. With the decrease of temperature, (a) the $V_{th}(T)$ of N-MOSFETs tends to be saturated. (b) The $V_{th}(T)$ of P-MOSFETs shows two trends, one is similar to N-, it tends to be saturated, and the other kicks-up continuously.

TABLE II
Summary of Two Types of P-MOSFETs $V_{th}(T)$ Behaviors

[Ref]	W / L (μm / μm)	Temp. Range (K)	Tech. Node	Tech. Type	$V_{th}(T)$ Behavior Type
[6]	1 / 0.014	0.34 - 300	14 nm	SOI FinFET	I
[12]	0.12 / 0.04	4.2 - 300	40 nm	Bulk	I
[17]	10 / 10	6 - 300	350 nm	Bulk	II
[16]	10 / 1	4.2 - 300	28 nm	Bulk	II
This work	10 / 1	4 - 300	180 nm	Bulk	II

To address these issues, this paper, for the first time, proposes a physical charge-based $V_{th}(T)$ model that includes interface-trapped charges near the band edge. This model strictly adheres to the standard $V_{th}(T)$ definition by various charges throughout the MOSFET capacitor. Additionally, we developed an analytical model desired for cryogenic VLSI design. The proposed model was verified with not only the measurement data collected from this work but also literature data showing different temperature behaviors by N- and P-MOSFETs. As a result, the proposed model handles different temperature behaviors of N- & P-MOSFETs originated from various processes in a universal way that keeps the physical meaning of C_{ox}.

Cryogenic CMOS design for quantum computing currently in 4 K temperature imposes unique challenges comparing to room temperature design. CMOS circuits performing qubit control and measurement usually composes VCO, LNA, ADC, PLL, MUX and so on. Design of these various CMOS circuits require accurate threshold voltage model in deep cryogenic temperature to predict circuit performance and reduce design margins, especially in high-precision and power sensitive circuits required for applications such as quantum computing. A key bottleneck to achieve this has been the missing of accurate models in cryogenic temperature because the physical mechanisms of MOSFET devices significantly change. Accurately modeling one of the most fundamental MOSFET parameters $V_{th}(T)$ in its standard physical definition term not only meaningful by itself but also would pave the way for modeling other key device parameters such as mobility in a cryogenic environment because they can be physically decoupled.

II. MODEL DEVELOPMENT

Following the standard definition of $V_{th}(T)$ for MOSFETs by various charges across C_{ox}, the mathematical formula incorporating interface-trapped charges near the Si band edge is generally expressed as follows:

$$V_{th}(T) = \psi_s' + \Phi_{ms} - \frac{Q_{dep}(\psi_s')}{C_{ox}} - \frac{Q_{it}(\psi_s')}{C_{ox}} \quad (1)$$

where the physical parameters ψ_s', Φ_{ms}, Q_{dep}, Q_{it} and C_{ox} are the inversion threshold, the metal-semiconductor work function difference, the depletion charge density, the interface-trap charge density, and the gate-oxide capacitance, respectively.

A. Physical Charge-based Threshold Voltage Model

Current state of art models are empirical [16], [18] and differ from the standard definition of threshold voltage, which is based on the charges across the MOS capacitor, C_{ox}. A new model is proposed in this study that preserves the standard definition of threshold voltage.

At cryogenic temperature, ψ_s' (including dopant freezeout) can be expressed as $2\Phi_F - \Delta\Phi_F$ [16], where $\Delta\Phi_F$ is the difference between Fermi energy levels including and not including dopant freezeout.

The difference in the metal and semiconductor work functions Φ_{ms} (including dopant freezeout) is given by $\Phi_{ms} = \Phi_m - \Phi_F + \Delta\Phi_F - \chi - E_g/(2q)$, where χ the electron affinity and E_g represents the Si bandgap and $E_g(T)$ is lightly temperature dependent (Varshni model [38]). $V_{th}(T)$ can be expressed as:

$$V_{th}(T) = \Phi_F + \Phi_m' - \frac{Q_{dep}(\psi_s')}{C_{ox}} - \frac{Q_{it}(\psi_s')}{C_{ox}} \quad (2)$$

where $\Phi_m' = \Phi_m - \chi - E_g/(2q)$.

The depletion charges, Q_{dep}, are determined by $Q_{dep} = -\Gamma_b C_{ox}\sqrt{2\Phi_F - \Delta\Phi_F}$, where Γ_b is the body factor. The charge density per unit area of interface states Q_{it} can be divided into two parts: $Q_{it} = Q_u + Q_0$. Q_u represents the standard uniform distribution of traps in the bandgap (due to dangling bonds) and Q_0 models the exponential increase of the interface-trap density near the band edge (due to disorder, strain, defects, etc.). These effects are researched in FETs at cryogenic temperatures [34],

[35]. Therefore, formula (2) can be expressed as:

$$V_{th}(T) = \Phi_F + \Phi_m' - \frac{Q_{dep}(\psi_s')}{C_{ox}} - \frac{Q_u(\psi_s')}{C_{ox}} - \frac{Q_0(\psi_s')}{C_{ox}}$$
$$= \Phi_F + \Phi_m' + \Gamma_b\sqrt{2\Phi_F - \Delta\Phi_F} - \frac{Q_u(\psi_s')}{C_{ox}} - \frac{Q_0(\psi_s')}{C_{ox}} \quad (3)$$

At cryogenic temperatures, $\Delta\Phi_F$ requires adjustment. The $\Delta\Phi_F$ produced by carrier freezing is given by $\Delta\Phi_F = U_T ln\frac{1+\sqrt{1+(4\alpha N_A)/n_i}}{2}$, where $U_T \triangleq k_B T/q$ is thermal voltage. $\alpha = g_A exp(-\Phi_A/U_T)$, where $\Phi_A \triangleq (E_i - E_A)/q$ and $g_A = 4$ is a degeneracy factor. n_i is the intrinsic carrier concentration. As n_i approaches to zero at extremely low temperature (< 4 K), it becomes impossible to calculate $\Delta\Phi_F$ directly. Since $4\alpha N_A/n_i \gg 1$, $\Delta\Phi_F$ can be adjusted to $\Delta\Phi_F = \frac{U_T ln(\alpha N_A/n_i)}{2}$ at low temperature.

Although model (3) can fit N-type and P-type I well, it cannot accurately fit P-type II [16], [17]. To address this issue, we propose the existence of an additional component of interface-trap charges at cryogenic temperature. We assume an exponential distribution of interface traps, refer to as "Exp", in terms of temperature Q_e. Modify model (3) to include this component as follows:

$$V_{th}(T) = \Phi_F + \Phi_m' + \Gamma_b\sqrt{2\Phi_F - \Delta\Phi_F} - \frac{Q_u(\psi_s')}{C_{ox}} - \frac{Q_0(\psi_s')}{C_{ox}} - \frac{Q_e(\psi_s')}{C_{ox}} \quad (4)$$

B. Analytical Threshold Voltage Model Development

To make (4) analytical, a triangular shape is introduced as illustrated in Fig. 2, whose integral results in polynomial form. The different distributions of the interface traps are shown in this figure, D_u, D_0 and D_e correspond to the distribution of charges Q_u, Q_0 and Q_e, respectively. Although other shapes, including trapezoids and rectangles, were considered, the triangle model requires the fewest parameters and is therefore the most straightforward approach. Hence, the triangular model has been selected for adoption.

As indicated in Fig. 2, $D_{it}(E) = D_u(E) + D_0(E) + D_e(E)$ where D_{it} is the total distribution of interface traps over energy.

The corresponding charge can be obtained by integral and

$$Q_{it} = -q\int_{E_i}^{+\infty} D_{it}(E)f(E)dE \quad (5)$$

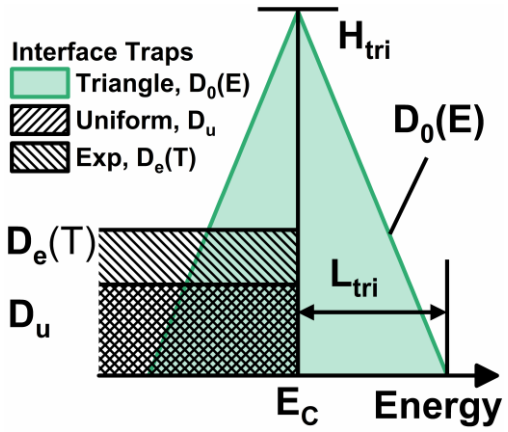

Fig. 2. Different distributions of interface traps.

where $f(E)$ is assumed as a step function. Therefore, $Q_u = -q\Phi_F D_u$, $Q_e = -q\Phi_F D_e$. In addition, unlike D_u, $D_e(T)$ is assumed to be temperature-dependent, and thus modified as:

$$D_e(T) = D_{e0}\exp(-T/T_0) \quad (6)$$

where D_{e0} is the distribution $D_e(T)$ when T trends towards 0 K and is a constant.

The triangle distribution $D_0(E)$ is given by:

$$D_0(E) = \frac{H_{tri}}{L_{tri}}|E - E_C| \quad (7)$$

where parameters H_{tri} represents the height of the triangular shape and L_{tri} represents half the length of the bottom side, that are extracted from measurement data. For the triangular distribution, $D_0(E)$ becomes zero on condition that $|E_F - E_C| > L_{tri}$. This gives:

$$Q_0 = -\frac{qH_{tri}}{2L_{tri}}\left[L_{tri}^2 + (q\Phi_F - E_g(T)/2)^2 + 2L_{tri}\left(q\Phi_F - E_g(T)/2\right)\right] \quad (8)$$

Consequently, the $V_{th}(T)$ model in (4) can be simplified to:

$$V_{th}(T) = \Phi_F + \Phi_m' + \Gamma_b\sqrt{2\Phi_F - \Delta\Phi_F} + V_{th,Uniform}(T) + V_{th,Exp}(T) + V_{th,Triangle}(T) \quad (9)$$

and

$$V_{th,Uniform}(T) = \frac{q\Phi_F D_u}{C_{ox}} \quad (10)$$

$$V_{th,Exp}(T) = \frac{q}{C_{ox}} D_{e0}\Phi_F exp(-T/T_0) \quad (11)$$

$$V_{th,Triangle}(T) = \frac{Q_0}{C_{ox}} \quad (12)$$

The proposed $V_{th}(T)$ model in (9) presents two significant progresses. Firstly, it presents more physical meaning to device behavior than introducing an empirical parameter with no physical meaning since (9) sticks to the standard $V_{th}(T)$ defined by charges across the physical capacitor C_{ox} associated with the MOSFET structure. Secondly, an analytical model is suitable for compact models in cryogenic VLSI design of CMOS technology.

C. Discussion of The Proposed Model Components

To better understand the role of each parameter in (9), Fig. 3 examines each constituent component of (9). The variation trend of $V_{th}(T)$ of N-type & P-type I with the decrease in temperature is shown in Fig. 3(a). The variation trend of $V_{th}(T)$ of P-type II with the decrease in temperature is shown in Fig. 3(b). Different from the previous situation, the "kicking-up"

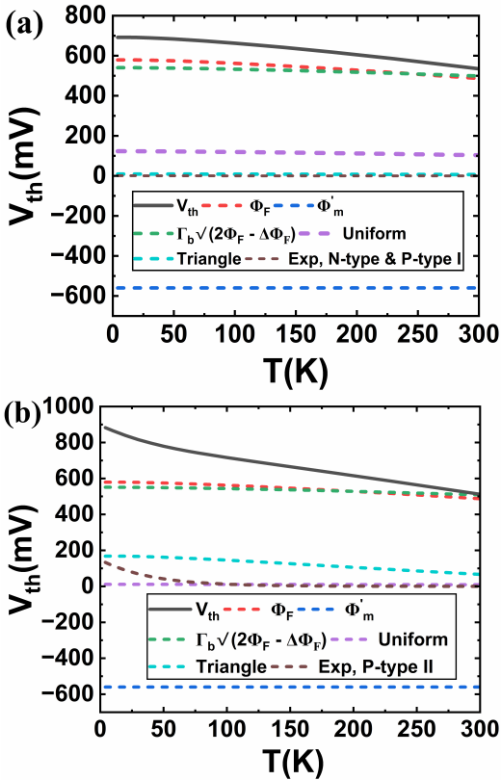

Fig. 3. Each component of $V_{th}(T)$ model (9) changes differently with decreasing temperature, namely (a) "saturating" for N- & P-type I and (b) "kicking-up" for P-type II.

trend of $V_{th}(T)$ of P-type II at low temperature is mainly due to the addition of the exponential "Exp" term.

The "Uniform" part, the "Triangle" part and the "Exp" parts of two different situations are shown in Fig. 4(a). Notably, $V_{th}(T)$ contribution stemming from the "Exp" distribution is considerably more pronounced than that of uniformly distributed charge, particularly in the case of P-type II MOSFETs, when operating at low temperatures.

Fig. 4(b) shows that (9) can well fit $V_{th}(T)$ of N-type and two different kinds of P-type, realizing the unification of the model at cryogenic temperature.

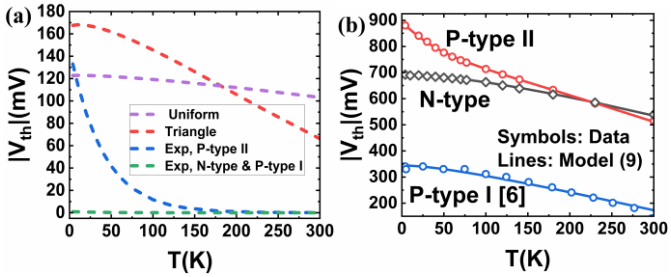

Fig. 4. (a) Effect of different fractions of interfacial trap charges on $V_{th}(T)$ with decreasing temperature. (b) Model (9) unifies the $V_{th}(T)$ model of N-type and two different P-type from room temperature to cryogenic temperature.

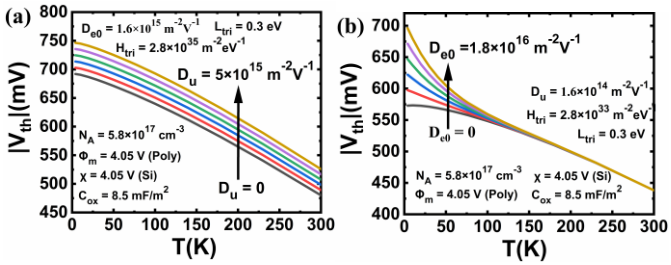

Fig. 5. (a) D_u does not change the qualitative behavior of $V_{th}(T)$ varying with temperature. (b) Add a key parameter D_{e0} to change the trend of $V_{th}(T)$ at cryogenic temperature.

D. Discussion of Interface Trapped Charges Parameters

D_u and D_{e0} are assumed to be temperature independent, and the effect of their variation on the $V_{th}(T)$ of the MOSFET is shown in Fig. 5(a) and (b), respectively. D_u does not change the qualitative behavior of $V_{th}(T)$ with temperature. D_{e0} is a key parameter that affects the trend of $V_{th}(T)$ at cryogenic temperature. H_{tri} and L_{tri} are the two parameters of the triangular distribution that affect the distribution of the interface trap charges, and the effect that a change in each parameter would have on $V_{th}(T)$ is shown in Fig. 6(a) and (b). The effects of H_{tri} and L_{tri} on $V_{th}(T)$ become more obvious with the decrease in temperature. But in comparison, the influence of H_{tri} at low temperature is greater than that of L_{tri}.

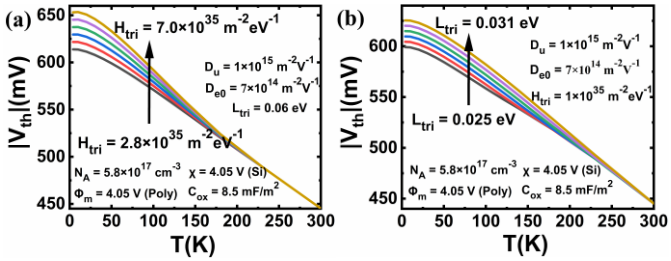

Fig. 6. Adding a triangle distribution of additional traps close to the band edge can change the qualitative behavior of $V_{th}(T)$ over temperature. The saturation of $V_{th}(T)$ is delayed to lower temperatures and the overall trend is more linear around 50 to 100 K if (a) H_{tri} or (b) L_{tri} increases.

As shown in Fig. 7 (a) and (b), taking P-MOSFETs as an example, the Fermi level increases near the conduction band with the decrease in temperature. As evidenced in the shaded regions of the figures, the increase in H_{tri} and L_{tri} will exert a progressively greater impact on the $V_{th}(T)$ with the decrease in temperature. However, the disparity lies in the fact that as the temperature decreases, the rise in $D_0(E)$ generated by the

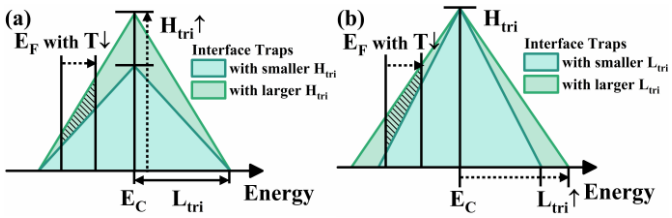

Fig. 7. When the temperature decreases, the Fermi level is close to E_C. At this point, the triangular interface charge increases. The increase of H_{tri} and L_{tri} will increase this part of the charge, as shown in (a) and (b), respectively.

increase in H_{tri} exceeds that resulting from the increase in L_{tri}. Comparing Fig. 7(a) with (b), it is obvious that the increase of $D_0(E)$ caused by the increase of H_{tri} is more and more. However, the increase of $D_0(E)$ caused by the increase of L_{tri} becomes incrementally lesser.

When the temperature approaches 0 K, the Fermi level tends to Ec-1/2 $E_D \approx$ 22.5 meV, hence, when L_{tri} is less than 22.5 meV, its effect on $V_{th}(T)$ becomes independent of temperature.

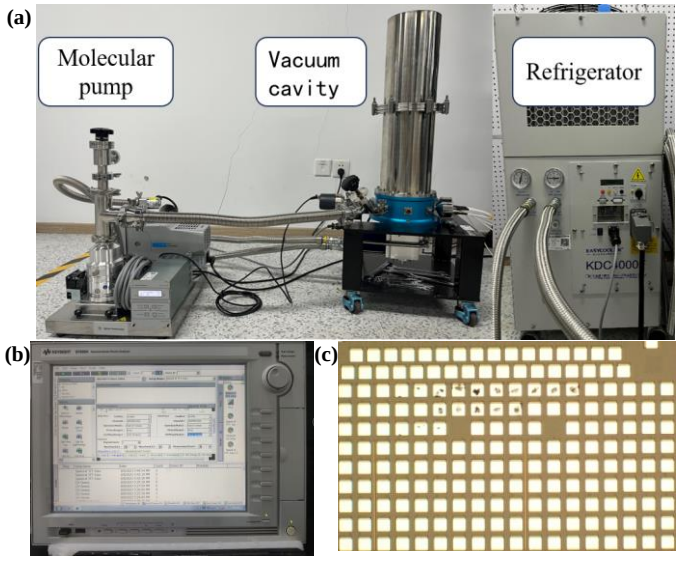

Fig. 8. Measurement setup equipment: (a) A pulse tube refrigerator system. (b) The semiconductor Analyzer B1500A. (c) The microscope image of the chip where the devices are on.

III. Experimental Data

N- and P-MOSFETs with the same channel width W 10 μm and length L 1 μm were fabricated with commercial 180-nm bulk CMOS process. For electrical characterizations, a Keysight B1500A semiconductor analyzer attached to a pulse tube refrigerator was used. Experimental measurements were conducted over a temperature range spanning from 300 K down to 4 K. Fig. 8 shows the measurement set up system. A complete refrigerator system is shown in Fig. 8(a). Fig. 8(b) is the semiconductor analyzer B1500A. Fig. 8(c) shows the microscope image of the chip where the devices are on. Fig. 9(a) and (b) show the experimental transfer characteristics data for N- and P- (type II) MOSFETs, respectively. The transconductance g_m of the N- and P-MOSFETs devices in the linear regime ($|V_{DS}|$ = 100 mV and $|V_{SB}|$ = 0 V) are shown in Fig. 10(a) and (b), respectively. $V_{th}(T)$ was extracted using the maximum g_m method. Fig. 11(a) and 11(b) show the output characteristic curves for N-MOSFETs in 4K and 300 K, respectively. Fig. 12(a) and 12(b) show the output characteristic curves for P-MOSFETs in 4 K and 300 K, respectively. The subthreshold swing (*SS*) data that are fitted by the relevant *SS* model [39], [40] of the N- and P-MOSFETs are shown in Fig 13(a) and (b) respectively.

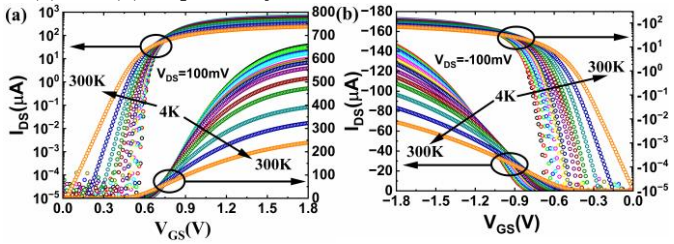

Fig. 9. Measurement data of (a) N- and (b) P-MOSFETs I_{DS} VS. V_{GS} characteristics in both linear and logarithmic scales, respectively, from 300 K to 4 K.

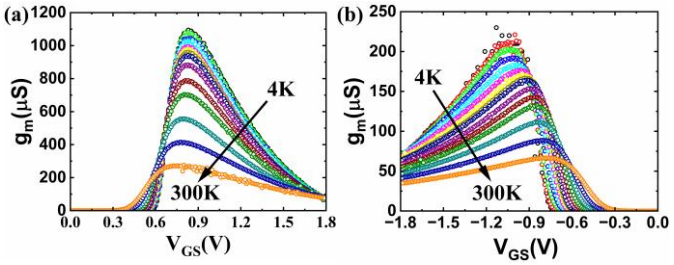

Fig. 10. Transconductance g_m VS. V_{GS} for N- and P-MOSFETs from 300 K to 4 K are shown in (a) and (b), respectively.

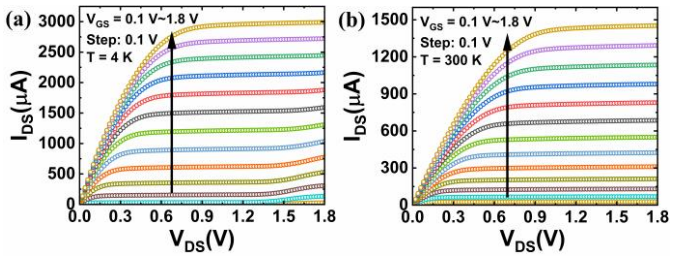

Fig. 11. Measurement data of N-MOSFET I_{DS} VS. V_{DS} characteristics from V_{GS} = 0.1 V to V_{GS} = 1.8 V at (a) 4 K and (b) 300 K.

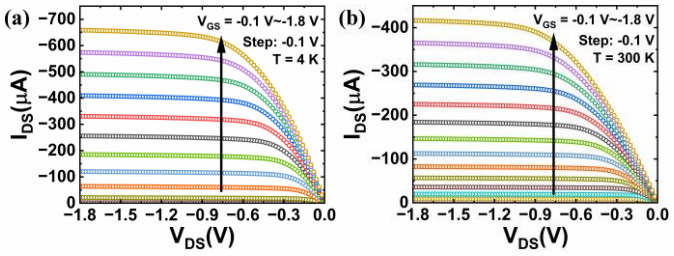

Fig. 12. Measurement data of P-MOSFET I_{DS} VS. V_{DS} characteristics from V_{GS} = -0.1 V to V_{GS} = -1.8 V at (a) 4 K and (b) 300 K.

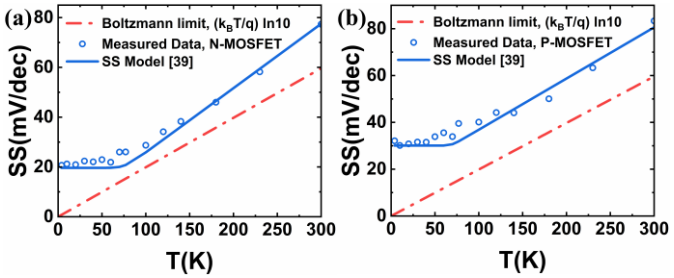

Fig. 13. (a) N- and (b) P-MOSFET *SS* VS. *T* characteristics from 4 K and 300 K.

IV. Modeling Results

A. Fitting Measurement Data

Fig. 14(a) and (b) show the excellent fit between the proposed analytical model (9) and measurement data from 300 K all the way down to 4 K, in both linear and logarithmic scales. Table III summarizes the different set of parameters extracted for two different behaviors of "saturating" for N-type and "kicking-up" for P-type II $V_{th}(T)$, respectively, for the unified model (9).

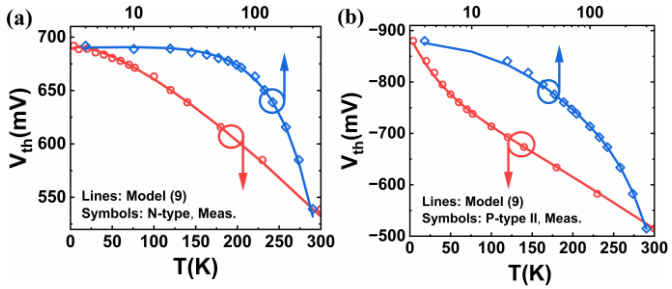

Fig. 14. The unified analytical model (9) can fit measurement data well for both (a) "saturating" N-type and (b) "kicking-up" P-type II $V_{th}(T)$, respectively, in both linear and logarithmic scales.

TABLE III
MODEL PARAMETERS USED IN FIG. 14 FOR 180 NM BULK CMOS PROCESS

Serial No.	(W / L=10 μm /1 μm)	NMOS	PMOS
1	N_A (cm^{-3})	5.8×10^{17}	5.8×10^{17}
2	T_{ox} (Å)	39.81	40.6
3	H_{tri} ($cm^{-2}eV^{-1}$)	1×10^{30}	4.6×10^{31}
4	L_{tri} (eV)	0.6	0.24
5	D_u ($cm^{-2}V^{-1}$)	10^{11}	10^{11}
6	D_{e0} ($cm^{-2}V^{-1}$)	10^{10}	1.35×10^{12}
7	Φ_m (V) (poly)	4.05	4.05

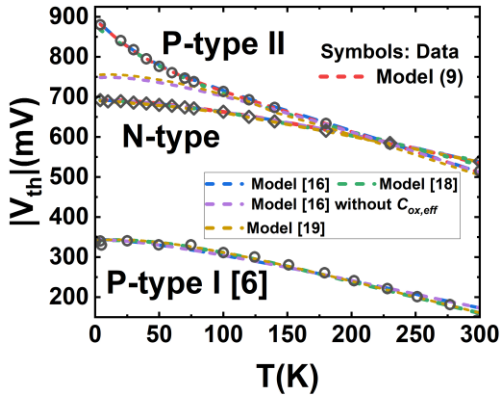

Fig. 15. A comparison between model (9) and model [16] (and model [16] without $C_{ox,eff}$), [18] and [19].

B. Analytical Model Calculation Speed and Accuracy

A comparison between model (9) and the newly developed model [16], [18], [19] with state-of-arts ones are shown in Fig. 15, with excellent agreement. However, the model in [16] without the $C_{ox,eff}$ item that has no physical meaning and the model in [19] will not be able to fit P-type II.

One of the major contributions of this paper is to transform the part of the model with error function (Gaussian distribution [16]) into an analytical model. This change greatly shortens the calculation time and improves the calculation efficiency without affecting the accuracy of the model. This is of great significance to the policy of VLSI circuits.

These two models are used to fit the measurement data and literature data [16], and the results are shown in Fig. 16, with excellent agreement. Using our measurement data for analysis, the mean error is only a few millivolts in Table IV. The results show that the fitting effect of the model (9) is also excellent.

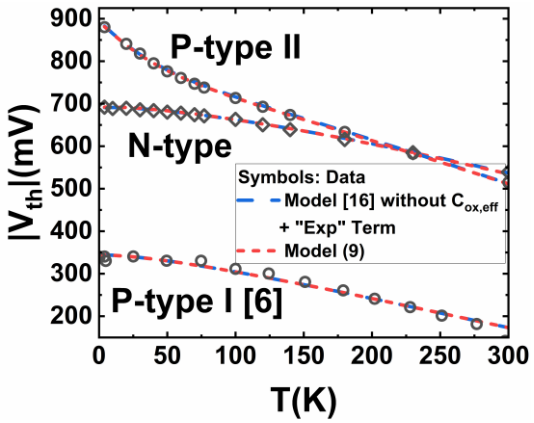

Fig. 16. The models use Gaussian distribution and triangle distribution, respectively, can both fit the measurement data and literature data [16] well.

Fig. 17 shows the fitting results of triangular model and Gaussian model with the measurement data. both models can control the error within ±3 mV (±0.4 %). Further comparing the average error of the two models (Table IV), the average error of the Gaussian model and data the average error of Triangle model and data are both less than ±3mV (±0.4%), showing the accuracy of the analytical cryogenic $V_{th}(T)$ model.

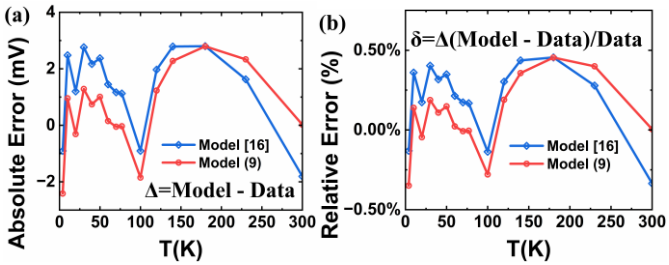

Fig. 17. (a) The absolute error and (b) the relative error between Gaussian distribution model and Triangular distribution model and measurement data.

In order to study the specific effect of this improvement, we calculate the $D_0(E)$ term of the two models, and the calculation is repeated 100 million times in order to avoid errors. The specific results are shown in Table V.

TABLE IV
AVERAGE ERROR OF MODEL AND MEASUREMENT DATA

Model	NMOS	PMOS
Model [16], Gaussian	1.84 mV (0.282%)	2.71 mV (0.379%)
Model (9), Triangle	1.16 mV (0.18%)	1.56 mV (0.217%)

TABLE V
CALCULATION TIME AND THE IMPROVEMENT OF EFFICIENCY

	$D_0(E)$, Error function	$D_0(E)$, Analytical
Calculation Time (100 million times)	19.93 s	11.44 s
The improvement in efficiency	(19.93 - 11.44) / 19.93 = 42.60 %	

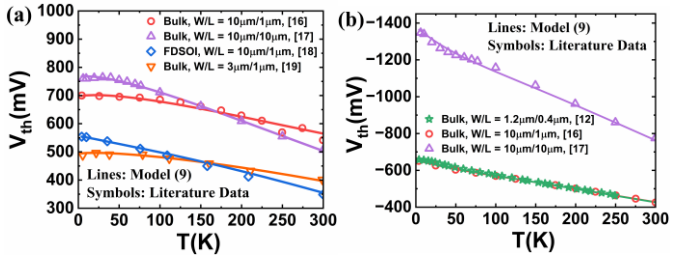

Fig. 18. The unified model (9) fits both (a) N- and (b) two types of P-MOSFETs $V_{th}(T)$ behaviors, either "saturating" or "kicking-up", respectively.

C. Fitting Literature Data

As shown in Fig. 18, excellent fit has been found between the proposed analytical model (9) and literature data in both N- and two types of P-MOSFETs $V_{th}(T)$ behaviors in Fig. 18(a) and (b), respectively. The parameters extracted for (9) are shown in Table VI.

TABLE VI
MODEL PARAMETERS EXTRACTED FOR (9) FROM LITERATURE DATA

Serial No.	[Ref]	MOSFET Type (N- / P-)	D_u ($cm^{-2}V^{-1}$)	D_{e0} ($cm^{-2}V^{-1}$)	H_{tri} ($cm^{-2}eV^{-1}$)	L_{tri} (eV)
1	[12]	P-type I	8×10^{11}	8×10^{11}	7×10^{31}	0.1
2	[17]	N-type	8×10^{12}	10^{10}	5×10^{31}	0.4
3	[17]	P-type II	8×10^{12}	2.1×10^{12}	1.1×10^{32}	0.4
4	[16]	N-type	10^{11}	10^{10}	3.5×10^{31}	0.1
5	[16]	P-type II	10^{11}	2.1×10^{12}	7.5×10^{31}	0.1
6	[18]	N-type	10^{11}	10^{10}	3×10^{31}	0.5
7	[19]	N-type	10^{11}	10^{10}	10^{30}	0.4

Recent studies have revisited band edge trap states in *SS* and $V_{th}(T)$ in deep cryogenic temperature[16], [18], [33], [39], [40]. From physical to closed-form analytical equations on subthreshold slope have been developed [33], [39], [40]. G. Pahwa *et al.* [18] proposed a different elaboration of Coulomb scattering on *SS* dependence on drain current I_{DS} at low temperatures. The model presented this paper comprehensively addresses trap states in threshold voltage modeling in low temperature by not only incorporating both the uniform and the Gaussian distribution components, but also adding an empirical exponential term to address different behaviors of N- and P-MOSFETs found in both literature [16], [17] and our own measurement data. The proposed model retains the standard definition of threshold voltage based on physical MOS capacitance, C_{ox}, would enable decoupling of physical effects such as Coulomb scattering [18] for future modeling development.

V. CONCLUSIONS

For the first time, this paper proposes a physical charge-based analytical threshold voltage model that covers different trending behaviors of both N- and P-MOSFETs while retaining standard threshold voltage definition based on the MOSFET capacitor C_{ox}. It is realized through adding an empirical term in explicitly including interface-trapped charges in the model. Such treatment provides a universal representation of the temperature-dependent behaviors of the $V_{th}(T)$ for both N-type and two types of P-MOSFETs while retaining physical C_{ox} in equation so that it both provides clear extraction strategy in design PDK generation and paves future way to framework modeling capable of dealing each key device parameter such as mobility and inversion charge in their respective physical meaning. Moreover, this analytical model can improve the computational efficiency for VLSI design of cryogenic CMOS technology. Excellent fit is shown between the proposed model and measurement data for both N- and P-MOSFETs from 300 K down to 4 K from this work.

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