Low temperature junction formation for EZ-FET

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***Abstract*—The EZ-FET is a device with simplified architecture and processing that enables fast electrical characterization of semiconductor films on insulators (SOI) with only two lithography levels and using regular process steps. For low temperature SOI substrates characterization, the EZ-FET must be processed at a low temperature, including the junctions formation i.e., the dopant activation process. Two EZ-FET dopant activation approaches using nanosecond laser annealing at low thermal budget are presented in this work. The first is the classical process of partial source and drain amorphization followed by their recrystallization. The second is a simplified process consisting of full source and drain amorphization followed by recrystallization. Both approaches are evaluated through the analysis of the electrical behaviors of the resulting structures.**

***Index Terms*—SOI, Nanosecond laser annealing, Dopants activation, Low temperature junctions**

I. INTRODUCTION

For some low temperature (LT) applications, like 3D sequential integration [1], silicon substrate layers must be fabricated at a low thermal budget (lower than 500°C during 2h) using different LT processing approaches. These LT substrates can be characterized using an electrical device that is fabricated on top of them. To avoid the process complexity and time consumption of a fully processed transistor, the EZ-FET (easy-FET) is a simple FDSOI-like (Fully Depleted Silicon On Insulator) device that can be used for the electrical characterization and benchmarking of Si layers fabricated with various types of LT approaches. Therefore, to ensure an efficient characterization of these LT films, the EZ-FET device itself should be fabricated at a low thermal budget. This includes all the device processing steps: active level lithography and etching, gate stack deposition, lithography and etching and finally dopants activation for source and drain (S/D) junctions formation. For the previous steps that are standardly performed at high temperature (above 500°C), low thermal budget processes were explored and are therefore available for the EZ-FET integration. However, the LT dopants activation is still challenging. To get past the limitations of this step, we proposed in [2] a junctionless EZ-FET where the S/D are left undoped, removing the dopants activation requirements. With an electrical model taking into account the access resistance in the undoped source and drain regions, LT films parameters can be extracted using a junctionless EZ-FET. However, front-channel parameters cannot be accurately obtained.

Besides, doped source and drain activation by nanosecond laser annealing (nLA) instead of furnace activation was also explored for LT processing [3]. This process can be achieved by first amorphizing the silicon layer by ion implantation then recrystallizing it in two different ways. The first consists in the melting of the partially amorphized Si followed by its recrystallization and is called Liquid Phase Epitaxial Regrowth (LPER) [4]. The second way can be achieved through Solid Phase Epitaxial Recrystallization (SPER) assisted by nLA [5]. In the current work, using nLA, these two methods are evaluated for LT EZ-FETs junction activation. Additionally, a simplified approach where the S/D are totally amorphized, leaving no crystalline seed for recrystallization, is explored. This allows to minimize the complexity of implantation depth tuning which is challenging for thin films and in this case, poly-crystalline S/D are obtained. The two approaches (with or without a crystalline seed) are evaluated and compared through electrical characterization (S/D resistances, drain current, and low-field mobility) and morphological characterization (Scanning Electron Microscopy SEM) for both n-type and p-type dopants.

II. EXPERIMENTAL METHODS

As previously said, a simplified architecture device called EZ-FET is used to evaluate the options for S/D processing. In Figure 1, a schematic of an EZ-FET device on an FD-SOI wafer with a 12-nm-thick top Si layer and a 145-nm-thick buried oxide (BOx) is presented. Since this device does not feature metallic contacts, the source, drain and gate probes are directly placed on the corresponding regions.

The active layer is defined by mesa etching. The gate stack is made of an Al_2O_3 layer obtained by atomic layer deposition (ALD) at 300°C (3 nm) and of a TiN layer (10 nm) formed by physical vapor deposition (PVD) at 350°C. Subsequent lithography and etching define a gate stack on top of the silicon film. Finally, the source and drain regions are implanted and annealed.

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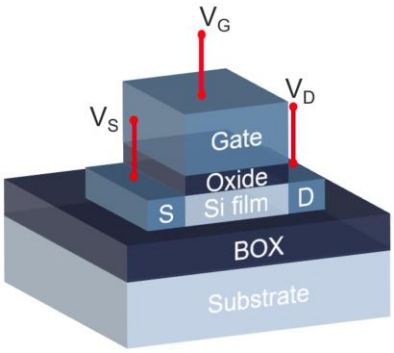

Figure 1. EZ-FET schematic displaying the different device layers and the placement of the probes used for electrical measurements.

Figure 2 schematically describes the dopant activation approaches that are tested here. The first consists in a partial amorphization of the source and drain regions that is obtained using an implantation energy that induces an amorphization depth of 7 nm, leaving a 5 nm crystalline seed. Then, using nLA, a recrystallization starting from this seed produces crystalline S/D with activated dopants. The second approach consists in a total S/D amorphization using an implantation energy high enough to get past the complexity of amorphization thickness control, particularly challenging in thin films. Then, after exposure to nLA, recrystallization starting from the BOX, since no crystalline seed is left, induces poly-crystalline S/D.

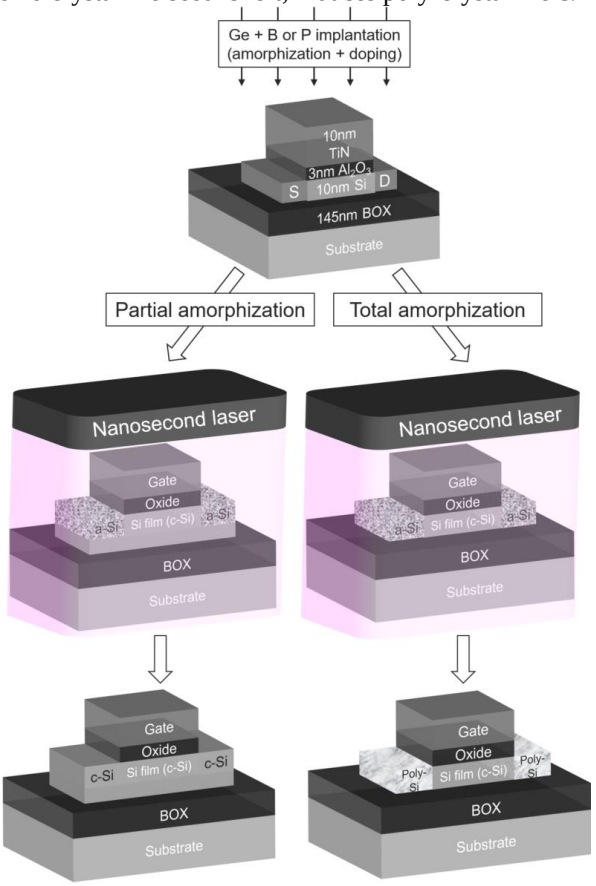

Figure 2. EZ-FET schematics before and after the two dopants activation approaches. The amorphized regions are presented in patterned colors in the S/D regions.

In the studied samples, all the implantation steps were performed in a VARIAN Viista HCP implanter. For p-EZFETs, Germanium ions were implanted at 0.3 keV with a dose of $5x10^{14}$ at.cm^{-2} for partial amorphization and at 1.25 keV with a $1x10^{15}$ at.cm^{-2} dose for total amorphization, followed by Boron ions implantation at 0.75 keV with a dose of $1x10^{15}$ at.cm^{-2} for doping. For n-EZFETs, Phosphorous ions were implanted at 0.75 keV with a dose of $5x10^{14}$ at.cm^{-2} for partial amorphization and doping, or at 2keV with a $2x10^{15}$ at.cm^{-2} for total amorphization and doping.

Afterwards, a SCREEN-LASSE LT3100 system based on a XeCl excimer laser (λ = 308 nm) and a pulse duration of approximately 160 ns was used to perform different nLA experiments. 10x10 mm^2 fields were irradiated with laser Energy Densities (ED) ranging from 300 to 600 mJ/cm² with an incremental step of 25 mJ/cm² using either a single pulse or multiple pulses. Additionally, a sample with dopants activated by high-temperature furnace annealing at 500°C for 2h was used as a reference for the activation level.

To evaluate dopants activation using both methods (partial or total amorphization), SEM observations were carried out to characterize the surface morphology of the studied samples. Moreover, S/D resistances were assessed by placing two probes on the source or the drain and measuring the electrical current induced by an applied voltage. Then, current-voltage I_D-V_G characteristics were used to evaluate the electrical performances at device level. For some graphs, the current is plotted as a function of the overdrive voltage V_G-V_T to compare the samples at a same inversion charge value. Finally, the low-field mobility μ_0 of the different samples was extracted by performing curve fits of the drain current on a current electrical model. The μ_0 values are used to compare the effectivity of the dopants activation approaches for LT substrates characterization.

III. Results and Discussion

A. Partial junctions amorphization

Measured S/D resistance values are plotted as a function of the laser energy density ED used for dopants activation in Figure 3 for a p-EZFET (a) and for an n-EZFET (b). In the single pulse experiment (black boxes), 3 resistance regimes are observed. (les nommer) First, as the laser ED increases from 300 mJ/cm² up to ED_1= 450 mJ/cm² for p-EZFET and 500 mJ/cm² for n-EZFET, the S/D resistance decreases. Then, from ED_1 up to 550 mJ/cm², the resistance reaches a minimum value comparable to the furnace-activated reference where it stabilizes. Finally, the resistance abruptly increases above ED = 550 mJ/cm² until it reaches the same level than that of a non-activated reference sample.

These three distinct resistance regimes can be explained by the morphological changes of the silicon in the S/D regions due to the exposure to laser at various ED [6]. Indeed, at ED lower than ED_1, the energy furnished by the laser beam is not high enough to melt the amorphous silicon (a-Si) in the S/D regions. It only induces a partial solid phase recrystallization decreasing the resistance to a value lower than the non-activated reference. As the crystalline thickness increases, the film resistance decreases, explaining the first resistance regime. Afterwards,

the entire a-Si layer melts from ED_1 to 550 mJ/cm². A liquid phase recrystallization is initiated then starting from the crystalline seed, which explains the minimum resistance value. The same a-Si melting + LPER cycle repeats in this ED range, explaining the resistance's stable value. Ultimately, as soon as the ED reaches 550 mJ/cm², the whole Si top layer melts (a-Si + crystalline seed) and LPER starting from the BOX is initiated. A poly-Si layer is then obtained, explaining the resistance degradation for 550 mJ/cm² and above. Although the same trend is observed for both p-type and n-type EZ-FETs, it is worth noticing that a-Si melting starts at a lower ED for p-EZFETs. That is due to the varying amorphised Si thickness induced by the difference of the ion implantation conditions of the two species (Germanium for p-EZFETs and Phosphorous for n-EZFETs) since a thinner a-Si layer requires less energy to reach the melt.

In the multiple pulses experiments, the same decreasing trend is observed in the first regime (from 300 mJ/cm² to ED_1) either using 10 (red diamonds) or 100 (blue circles) cumulative laser pulses. As for the single pulse case, a solid phase recrystallization takes place in this range of ED [4]. However, in the multiple laser pulses case, each pulse provides enough thermal energy to recrystallize a given amorphous portion (similar to the single pulse case). This cumulative effect of multiple pulses, results in a thicker recrystallized layer, which increase with the number of laser pulses, and therefore lower resistances are achieved. Consequently, at a same laser ED, multiple pulses ensure a better recrystallization of the Si layer.

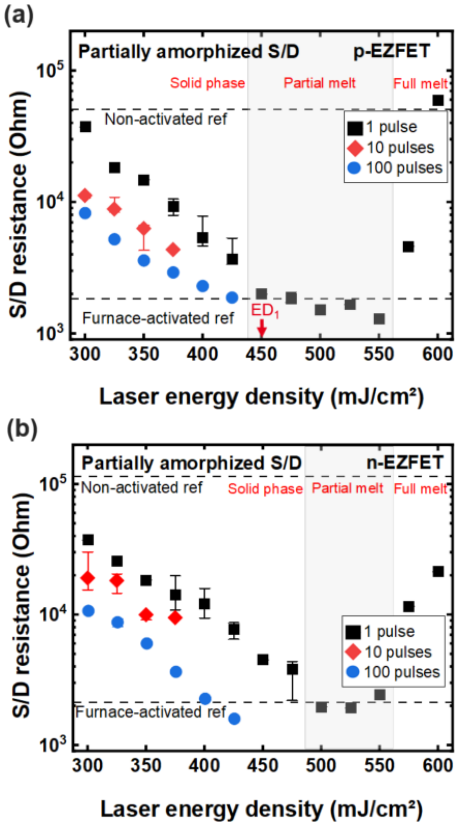

Figure 3. S/D resistance for laser energy densities ranging from 300 mJ/cm² up to 600 mJ/cm² using one pulse (black boxes), 10 pulses (red diamonds) or 100 pulses (blue circles) in a partially amorphized sample for a p-EZFET (a) and an n-EZFET (b).

The measured drain current I_D curves with a single laser pulse and for ED ranging from 300 to 400 mJ/cm² are plotted in Figure 4 for a p-EZFET (a) and for an n-EZFET (b). As previously explained, the recrystallization happens in solid phase in this ED range. It is worth noticing that at ED conditions corresponding to liquid recrystallization (higher than 400 mJ/cm²), the gate stack is damaged, inducing a current leakage as shown in the measured gate current I_G vs. gate voltage V_G inset of Figure 4. Furthermore, due to the thin TiN gate electrode used (10 nm), at the S/D implantation step, the ions could pass through the gate, inducing a channel doping of the same type as the junctions. This results in a threshold voltage shift. Therefore the I_D is plotted as a function of the overdrive voltage (difference between gate and threshold voltages) V_G-V_T for the sake of a better graph visibility. For both p-EZFETs and n-EZFETs, the current level increases with the laser energy density, in correlation with the measured resistances in Figure 3. Higher current levels are attained thanks to the better junctions activation.

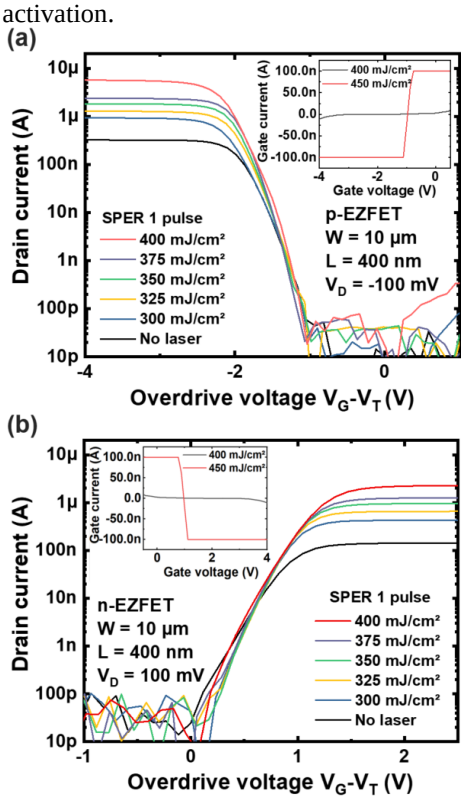

Figure 4. Measured drain currents vs. overdrive voltage V_G-V_T at V_D = 0.1 V at laser energy densities ranging from 300 to 400 mJ/cm² in a partially amorphized and recrystallized sample by single pulse SPER for a p-EZFET (a) and an n-EZFET (b).

To assess the number of laser pulses effect on drain current levels, we plot in Figure 5 the linear current, which is defined as: I_D at V_G = -3V and V_D = -0.1V for p-EZFETs, or I_D at V_G = 3V and V_D = 0.1V for n-EZFETs, for various laser ED and number of cumulated pulses. Again, in correlation with the resistance behavior previously described, the current level

increases with the laser ED using either 1, 10 or 100 pulses thanks to the better junction activation. Moreover, at a same ED, the current level increases with the number of pulses, which is consistent with the access resistance reduction. This can be particularly useful for LT device fabrication since a complete dopants activation is possible with a lower laser energy and multiple pulses, reducing the process's thermal budget.

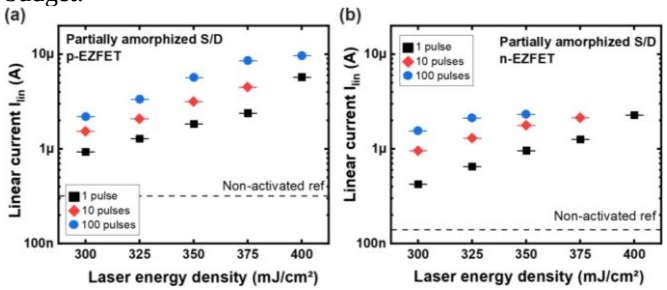

Figure 5. Measured linear currents at laser energy densities ranging from 300 to 400 mJ/cm² using 1 pulse (black boxes), 10 pulses (red diamonds) or 100 pulses (blue circles) in a partially amorphized and recrystallized sample by single pulse SPER for a p-EZFET (a) and an n-EZFET (b).

We can conclude from the results of this first approach that dopant activation in the S/D regions can be effectively performed using nLA with one or multiple laser pulses. However, an optimal junction formation with this method requires a compromise between dopant concentration and seed thickness. On one hand, the ion implantation energy should be tuned to leave the required thickness, and on the other hand, dopant concentration in S/D regions should be precisely tailored to benefit from optimal junctions. Nonetheless, the precise control of the crystalline seed thickness after ion implantation is challenging, especially for thin films. So, to avoid the complexity of such an implantation adjustment, another approach for dopants activation is explored. It consists of a total amorphization of the Si layer followed by LPER recrystallization of the S/D region, resulting in polycrystalline S/D terminals. Results are presented in the next section.

B. Total junctions amorphization

Measured S/D resistances are plotted as a function of the laser ED used for totally amorphized junctions activation in Figure 6. Similarly to the partial junctions amorphization case (Figure 3), the resistance features 3 regimes depending on the melting depth. Before a-Si melting (ED < ED_2 = 375 mJ/cm² for p-EZFET, whereas ED_2 = 400 mJ/cm² for n-EZFET), the resistance is high and constant. That is because S/Ds remain amorphous since SPER does not occur without a crystalline seed. Again, as for partially amorphized junctions, the a-Si layer melting starts at a lower ED for p-EZFETs due to the different amorphized thicknesses using two different dopant species. As soon as the a-Si layer starts melting at ED = ED_2, LPER recrystallization initiates from the a-Si and yields poly-crystalline junctions. This explains the resistance stabilization at a minimum value, which is comparable to a furnace-activated sample, for ED between ED_2 and 500 mJ/cm². Beyond ED = 525 mJ/cm², the resistance increases again. The reason is that the fully formed poly-Si layer melts and recrystallization starts from the BOX this time.

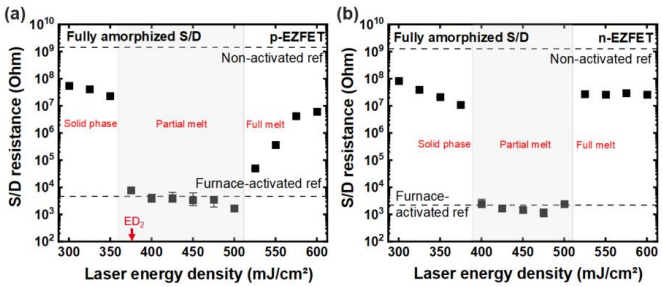

Figure 6. S/D resistance for various laser energy densities ranging from 300 mJ/cm² up to 600 mJ/cm² in a totally amorphized sample for a p-EZFET (a) and an n-EZFET (b).

In comparison with the partial amorphization experiment, the ED initiating a-Si melting is lower for totally amorphized junctions. ED_x refers to the lower energy density values for which the a-Si melting is achieved. This can be experimentally observed through the S/D resistance drop. Index 1 and 2 refer to the partial and the total amorphisation cases, respectively. For p-EZFET: ED_1 = 450 mJ/cm² > ED_2 = 375 mJ/cm², and for n-EZFET: ED_1 = 500 mJ/cm² > ED_2 = 400 mJ/cm². In fact, without a crystalline seed, a-Si melting starts sooner than in the presence of a crystalline seed due to the fact that the thermal conduction of crystalline silicon is higher compared to that of the amorphous silicon. So, heat is dissipated faster in samples with a crystalline seed [7]. Therefore, to reach the sample's melting temperature, a higher laser energy density is needed.

It is worth noting than the minimum resistance in the partial amorphization case, corresponding to a mono-crystalline silicon, is equivalent to that of the total amorphization one, corresponding to a poly-crystalline silicon (~ 2kΩ). This is because at high dopant concentration, the poly-crystalline and the mono-crystalline Si have comparable resistivity values [8]. For the phosphorous implantation for instance, the dopant concentration can be estimated by $\frac{2\,10^{15}\,at.cm^{-2}}{t_{Si}=10^{-6}cm} \sim 2\,10^{21} at\,cm^{-3}$. This value is consistent with the dopant concentration range where mono and poly crystalline Si resistivity values are similar.

Figure 7 displays the measured drain current I_D curves as a function of the overdrive voltage V_G-V_T for different laser energy densities lower than the gate damage condition (< 450 mJ/cm²). For both p-EZFETs and n-EZFETs the current levels are correlated with the measured resistances in Figure 6. Indeed, there is no measured current before ED = ED_2 since the S/D resistance remains high, as junctions are not activated yet. Then, above this threshold, a current is measured and its level remains almost constant with the laser energy density, as did the resistance. Ultimately, above 450 mJ/cm², a gate current leakage occurs due to the gate stack damage that will be visually demonstrated later, in Figure 8.

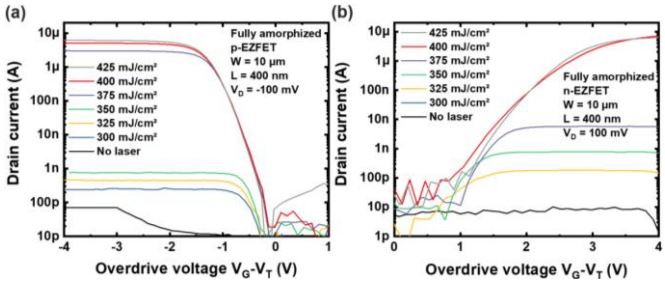

Figure 7. Measured drain currents vs. overdrive voltage V_G-V_T at V_D = 0.1 V at laser energy densities ranging from 300 to 425 mJ/cm² in a totally amorphized and recrystallized sample for a p-EZFET (a) and an n-EZFET (b).

The explanations of the electrical behaviors can also be supported by the morphological variations of the samples under test. In Figure 8, SEM top-view images at various laser energy densities are unveiled. First, at ED < ED_2, the samples are visually the same as before nLA; the silicon is still amorphous. At ED = ED_2 (375 mJ/cm² for p-EZFET and 400 mJ/cm² for n-EZFET), and above, poly-Si grains start to form in the S/D regions, which is consistent with the resistance drop in Figure 6 and the current measurements in Figure 7. Finally, beyond 450 mJ/cm², the gate damage that explains the measured current leakage is clearly observed.

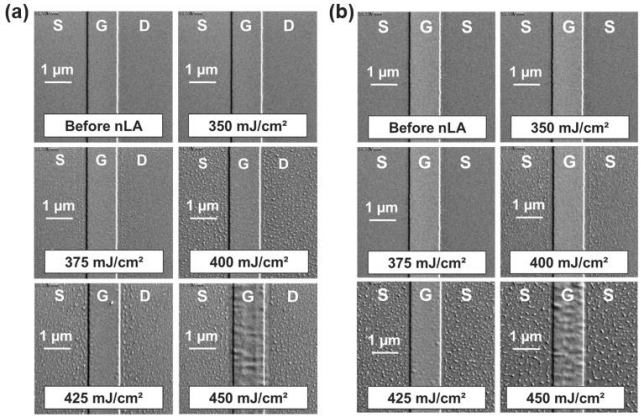

Figure 8. (a) p-EZFET and (b) n-EZFET top-view SEM images displaying the S/D and gate regions in a totally amorphized sample after exposure to nLA at various energy densities from 350 mJ/cm² to 475 mJ/cm².

We can conclude from the results of this second approach that poly-crystalline terminals activated by LPER without a crystalline seed can effectively be used for LT film characterization. This approach eliminates the complexity of ion implantation depth tuning, particularly for thin films. In the next section, the two EZFET junction activation approaches described above are compared.

C. Comparison of junction activation methods

The linear currents I_{lin} are plotted as a function of the laser ED in Figure 9 to compare the current levels obtained with the two dopants activation approaches (partial or total amorphization). By comparing the full and open symbols, it is clear that from 300 mJ/cm² to ED_1 (350 mJ/cm² for p-EZFET and 375 mJ/cm² for n-EZFET), SPER with either a single or multiple pulses initiates S/D recrystallization when a crystalline seed is left, while the S/D remain amorphous when there is no crystalline seed. This explains the measured current in the first case, and the low current (below 1 nA) in the second case. It is only above ED_1 that a significant current is measured for the totally amorphized samples. Consequently, appropriate current levels can be obtained for both approaches at a specific laser ED. Therefore, both approaches can be used for LT junctions activation.

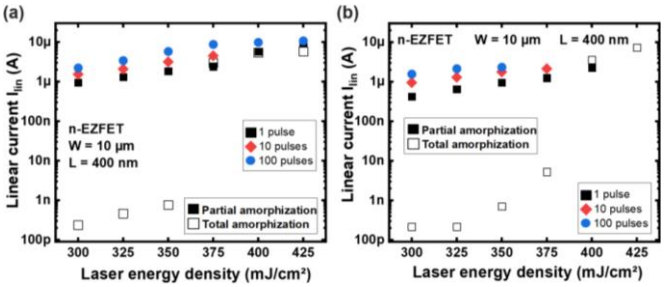

Figure 9. P-EZFET (a) and n-EZFET (b) linear currents for laser energy densities ranging from 300 to 425 mJ/cm² for SPER with partially amorphized S/D (full symbols, black boxes: 1 pulse, red diamonds: 10 pulses, and blue circles: 100 pulses) and LPER with totally amorphized S/D (open boxes).

The ultimate aim of this study is to validate an effective electrical characterization and comparison of LT substrates using a LT EZ-FET through the extraction of the low-field mobility μ_0, for instance. The previous results proved that the laser junctions activation approaches presented in this work can be used as LT processes during the device fabrication. In Figure 10, yielded μ_0 values for each electrical activation protocol are compared for a p-EZFET example using the Lambert function extraction methodology [9] that eliminates the contribution of access resistances in an EZ-FET. It is worth noticing that the samples do not have optimized gate stacks, but the aim here is the evaluation of options for S/D activation. Therefore, the comparative analysis of μ_0 is relevant rather than the actual extracted values. Optimized oxide types and S/D implantation conditions should yield definitely higher mobility values on par with that of Fig. 10 reference, e.g. for an EZ-FET with a SiO_2 gate oxide and furnace junctions activation [10].

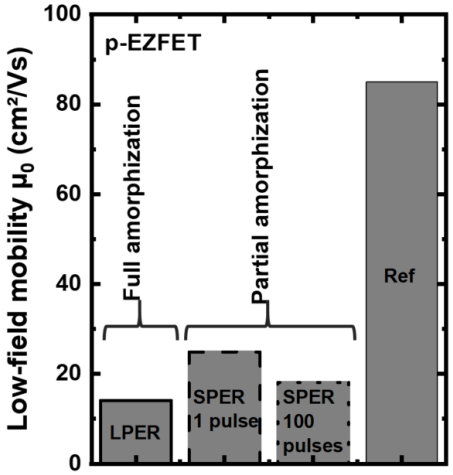

Figure 10. Extracted low-field mobility µ0 in a p-EZFET with junctions dopants activation at 400 mJ/cm² by LPER in a totally amorphized sample (line) or by SPER in a partially amorphized sample using either 1 laser pulse (dashes) or 100

pulses (points).

Disregarding the degraded mobility values, this graph proves that comparable Si film mobility values can be extracted from EZ-FET samples with junctions activated using either of the two approaches (with or without seed). Note that the used extraction methodology for μ_0 reduces the access resistances impact. Therefore, since the minor access resistance variation with the activation method does not impact the extracted μ_0, the criterion of choice of the activation method for process only depends on the desired application: SPER for standard crystalline junctions, multipulsed SPER for lower thermal budget requirements, and LPER with totally amorphized S/D for thin film process simplicity.

IV. Conclusions

In this work, nLA was explored as an alternative to furnace annealing for low temperature dopants activation for p-EZFETs and n-EZFETs junctions formation. Two approaches were presented: the first consisting in a partial amorphization by ion implantation of the Si in the S/D region followed by a classical recrystallization starting from the crystalline seed whereas the second consists in the total amorphization then the recrystallization of the S/D for implantation process simplification. For both doping types, and using both approaches, effective dopant activation was achieved as proved by the extracted S/D resistances that are comparable with a furnace-activated reference. Moreover, appropriate current levels were obtained. The multi-pulsed SPER provides however the best activation and the highest current levels.

Moreover, comparable low-field mobility values were extracted in EZ-FET samples activated with the two different dopants activation options. Therefore, the two dopant activation approaches can be used to characterize and compare technological splits, and particularly, various LT substrates fabrication methods. The method choice would only depend on the device integration conditions (e.g. multipulsed SPER for challenging thermal budget constraints, LPER without seed for thin films).

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