Carbon Nanotube FET Technology for Radio-Frequency Electronics: State-of-the-Art Overview

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***Abstract*—Carbon-based electronics is an emerging field. Its present progress is largely dominated by the materials science community due to the many still existing materials-related obstacles for realizing practically competitive transistors. Compared to graphene, carbon nanotubes provide better properties for building field-effect transistors, and thus, have higher chances for eventually becoming a production technology. This paper provides an overview on the state-of-the-art of CNTFET technology from an electrical engineering and radio frequency analog applications point of view. Important material properties, resulting device structures, their fabrication, and the most relevant modeling concepts are briefly reviewed. Furthermore, recent results on device and circuit performance and the future prospects are presented in the context of practical requirements and applications.**

***Index Terms*—Carbon electronics, carbon nanotube, CNTFET, emerging technology, radio frequency (RF) transistors.**

I. Introduction

The extraordinary electronic *intrinsic* material properties of carbon nanotubes (CNTs) and graphene (G) have spawned large waves of research activities for extending the silicon based CMOS technology roadmap. The first wave started with the CNT discovery in 1991 [1] while the second wave was triggered in 2004 by the first experimental realization of graphene [2] Field-effect transistors (FETs) built with these two materials have achieved extrinsic current gain cut-off frequencies (f_T) of around 10 GHz [3], [4], thus generating interest in their applications to, e.g., the low-GHz radio-frequency (RF) wireless market.

In graphene, the lack of a bandgap leads to an intrinsic voltage gain significantly lower than one and thus also very low power gain. It may be interesting to note the following comments in [5], which the authors of this paper believe to be an accurate and realistic assessment: "*The performance of GFETs has been hampered by graphene's metallic conductivity. ...These low [on/off] ratios ... present a fundamental problem for any realistic prospect of graphene-based integrated circuits*." A recent quantitative study [6] has demonstrated that CNTFETs achieve higher performance, such as power gain and cut-off frequencies, at lower power dissipation and are thus fundamentally more suitable for RF analog applications than GFETs. As a result, CNTFET based RF devices and circuits show superior performance to those built with GFETs, as discussed in [7]. Therefore, the focus of this paper is on RF CNTFET technology only and has the goal of providing an overview of its present status with respect to practical *engineering* RF analog applications.

Compared to conventional bulk semiconductors, CNTs possess a number of properties making CNTFETs fundamentally superior to Si/SiGe based MOSFETs for certain applications. While THz performance has been predicted for ideal CNTFET structures with sub-100 nm channel length [8], practical materials, equipment, and fabrication related constraints make it very unlikely to achieve these predictions and beat incumbent technologies on device speed alone in the foreseeable future. The same is true for digital applications due to issues with metallic tubes and the lack of methods for deliberate single-tube placement (despite the recent advances of single tube placement presented in [9]). Also, considering the many years of research and investment already spent, the pressure for demonstrating first commercial applications keeps increasing. Thus, based on existing RF performance, targeting low-GHz products as first market entry makes most sense. However, beating depreciated incumbent technologies at the same device speed but just on cost is virtually impossible, since circuit redesign typically also has to be factored in. Therefore, additional features, which are unavailable in existing devices, are required for CNTFET (and any other emerging) technology to become competitive. These features result in particular from the one-dimensional (1D)

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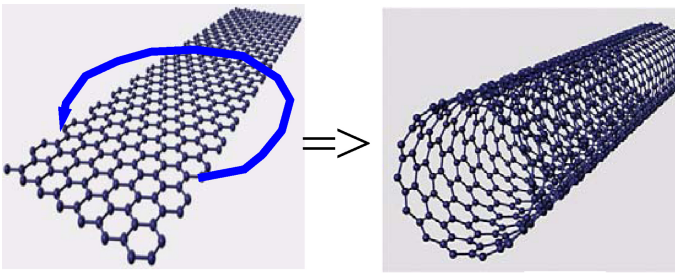


(a) (b)

Fig. 1. Sketch of (a) graphene nanoribbon and (b) carbon nanotube.

transport in CNTs, which leads to (i) higher mobility and current carrying capability, (ii) low distortion due to a linear relation between drain current and input (gate-source) voltage, and (iii) higher temperature stability and electrothermal ruggedness.

This paper provides an overview on the state-of-the-art of CNTFET technology and electronics from an *electrical engineering* and *RF applications* point of view. The relevant material properties are reviewed briefly in Section II. The various existing fabrication approaches are discussed in Section III with emphasis on manufacturability and integrated circuits for RF applications. Based on the resulting device structures, the most relevant modeling concepts are presented in Section IV in order to provide the basic understanding for the expected advantages of CNTFETs. Sections V and VI, respectively, then show selected device characterization results (with a model comparison) and circuit results, respectively, achieved so far. The necessary improvements for fabricating devices with competitive performance and the potential solutions in terms of device fabrication methods are discussed in Section VII. Finally, the most important conclusions are summarized in Section VIII.

II. Material Properties

Graphene is a single-atomic layer Carbon (C) sheet [see Fig. 1(a)], which does not have a bandgap (W_g) and thus shows (quasi-)metallic transport behavior [2]. Opening up a bandgap is possible by reducing the width of the sheet to a few nm, thus creating a graphene nanoribbon (GNR). However, this leads to not only a significant reduction in mobility [10] but also a large variability in threshold voltage and mobility [11] due to the uncontrollable random organization of atoms and their bindings with other materials at the edges.

Such effects can be circumvented by rolling up a GNR into a CNT, which occurs "naturally" under certain (process) conditions. This way, semiconducting CNTs with a bandgap of around 0.88 eVnm/diameter can be obtained. The conduction band has a double degeneracy compared to graphene nanoribbons, which only has a single degeneracy [11]. For practical transistor applications typical diameters are around 1.6 nm, yielding a bandgap of $\approx$0.55 eV. For the above diameter range, carrier transport is basically one-dimensional (1D) in the tube axis direction and occurs at the CNT surface. Such 1D transport significantly reduces the scattering probability. Low-field mobilities at room temperature of up to about 8.10^4 cm^2/Vs have in fact been measured [12], which corresponds to a mean free path of several hundred nm. The low phonon scattering resulting from 1D transport also is expected to lead to extremely low thermal noise, low self-heating, relatively high breakdown voltage, and a linear $I_D(V_{GS})$ relation above threshold. Finally, CNTs have a very robust mechanical structure. All these features, along with the high Fermi velocity of $8 \cdot 10^7$ cm/s and the very small quantum capacitance in a 1D conductor, make CNTFETs very attractive for future RF applications such as amplifiers, mixers and switches.

A detailed analysis reveals that one out of three possible ways of rolling up a graphene sheet yields a metallic (m-) tube while the other two yield a semiconducting (s-) tube (e.g. [13]). The current carrying capability of CNTs has been estimated to be as high as 10^4 mA/μm^2 [14], which is orders of magnitude higher than in metals presently used by the semiconductor industry and thus has been the focus of interconnect and contact via research [15]. For building transistors though metallic tubes need to be avoided. Detailed information on CNTs and related devices can be found in [16], [17].

Since CNTs possess only a single atomic layer interfacing with other materials, such as the integration in a transistor structure, typically changes the mobility and can also change the bandgap due to interactions between the materials at the interface (e.g. [18]). In order to avoid a negative impact on the electrical device characteristics, suitable materials have to be found and integrated into the process flow.

III. Device Fabrication

CNTs can be fabricated with a variety of methods such as arc discharge, laser ablation, CVD growth or cloning [19]–[22]. Fig. 2 shows a generic process flow for building CNTFETs. Variants of this flow will be discussed below along with their pros and cons.

An often employed approach is the dispersion of, e.g., commercially available CNTs from solution on a wafer [3], [23], [24]. The achievable tube density (i.e. number of tubes per μm) ranges from several CNTs per μm to 100/μm for multiple dispersions. The method has two advantages. First, the CNTs in the solution can be purified to up to 99% semiconducting (s-) tubes by ultracentrifugation (UCF). Second, the tubes can be fairly easily aligned in parallel by dielectrophoresis (DEP). The latter requires a voltage to be applied between the two electrodes (i.e. source (S) and drain (D)) the tubes are supposed to connect. As a consequence, the S/D patterning and metal already needs to be available. The latter is one of various disadvantages of this method. Applying DEP to many devices simultaneously requires connecting all devices on a wafer in parallel, which limits the wafer size and also adds a process step for removing these connections later. Secondly, UCF typically leads to broken and thus fairly short tubes in the range of not more than 1μm, which makes the fabrication of multi-finger RF devices difficult; UCF may also cause defects which increase carrier scattering. Third, exposing the CNTs to the solution contaminates the tube surface and causes hysteresis,

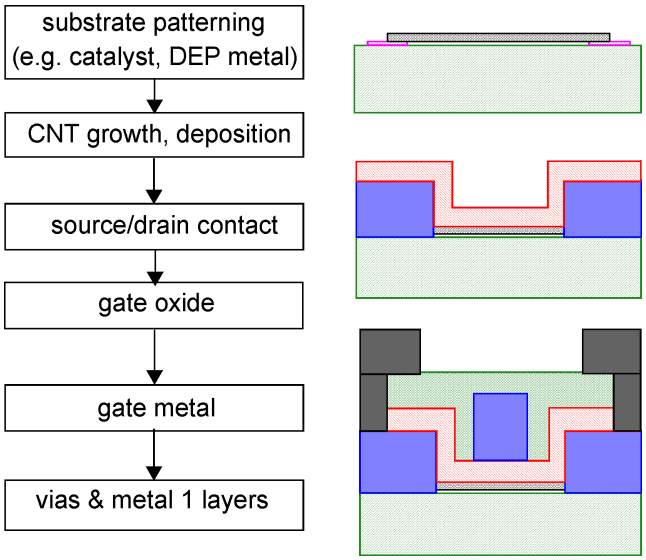
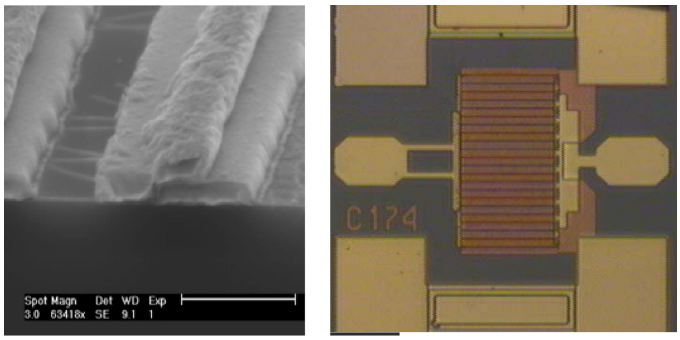


Fig. 2. Generic CNTFET process flow (for explanations see the text).



(a) (b)

Fig. 3. (a) TEM picture of the (open) channel region with CNTs visible. (b) Chip photo of a multifinger MT CNTFET in RF pads. Courtesy RFNano Corporation.

unless the surface is completely cleaned which appears to be still very difficult. Fourth, intentional wafer-scale device placement is still a challenge, making RF analog circuit fabrication difficult. This has resulted in the perception that deliberate placement of CNTFETs is impossible. While this is true for single-tube FETs it is not for RF FETs as discussed below.

CNTs can also be grown directly on-wafer using CVD [25], [26] and a suitable catalyst material. The growth result in terms of chirality, tube density, and alignment depends on not only the growth conditions (such as catalyst size and material, C feeding rate) [26] but also on the selected substrate. On quartz, CNTs with a density of up to 15/μm [27] and a s:m ratio of up to 19:1 [28] have been achieved. A perceived advantage of using quartz is the tube alignment due to the interaction between the van-der-Waals force of the quartz surface and the carbon atoms during growth. However, the corresponding phonon interaction between the quartz and charge carriers on the tube appears to cause a significant reduction in carrier mobility as indicated by electrical measurements in [27] and also at RFNano Corp. For this reason and also for integration with existing (CMOS) technology, the CNT arrays have been transferred from quartz to a SiO_2 substrate [27], [29], where an about three to five times higher mobility can be achieved. However, it is questionable whether this substrate transfer process is suitable for industrial wafer-scale production in terms of throughput and also process variability; e.g., the transfer introduces contamination of the CNTs, which will cause hysteresis and uncontrollable threshold voltage variations.

For direct growth of CNTs on SiO_2, a temperature around 900°C is often used [21], [25], which is too high for CMOS integration. However, a growth temperature as low as 600°C was shown in [30]. Although on-wafer CNT growth yields long tubes that are suitable for RF FETs and appears to be most attractive for large-scale integration, it presently still has a few drawbacks. First, the still unavoidable growth of metallic tubes has so far limited the electrically measured s:m ratio to about 3:1 to 4:1. Second, the random alignment (compared to quartz) causes not only the average length of the tubes to be larger than the lithography defined S/D spacing but also to crossings of m-tubes over s-tubes. These crossings cause Schottky (point) contacts and lead to potential barriers in the s-tubes, thus resulting in a deterioration of their transport characteristics. Third, the tube density is only in the range of 10/μm at maximum. Fourth, the gate oxide thickness varies from tube to tube since they can bend (upwards) during growth.

As an example, Fig. 3(a) shows the open channel region of a fabricated CNTFET [4]. The randomly aligned CNTs are clearly visible since electron microscopy enhances the visibility of the tubes by about a factor of 100. Raman spectroscopy and AFM data suggest the majority of the CNTs to have diameters around 1.6 to 1.8 nm. For RF purposes, it is important that the CNTs bridge the channel region directly, i.e. without crossings and forming a percolation network, since in the latter the carrier mobility is determined by the "point" contacts formed by the crossings and thus is much lower than in the tube itself.

Fig. 3(b) shows an example for a multi-tube (MT) RF CNTFET with 20 gate fingers of 0.4μm length and 40μm width. The S to D distance is 0.8μm, and the SiO_2 thickness is $> 1.5\mu$m for providing sufficient electrical (RF) isolation. The relaxed dimensions are a consequence of the fact that for an emerging technology like this one, investment for production-type equipment (such as advanced lithography) is still limited.

The in-place CNT growth allows the deliberate placement of devices with arbitrary size on a wafer, thus enabling RF analog circuit design. Fig. 4(a) shows an example of a typical test chip for process development and modeling. It contains special DC structures and large arrays of RF FETs, ordered as regularly as on test chips for incumbent technologies. CNTFETs are fabricated here along with passive devices and simple cascode stages on a 4" wafer. The process requires just three masks for building the transistor structure itself as well as two more masks for the formation of vias and a second (Au) metallization layer [4].

Device uniformity and yield are critical issues for emerging technologies, and are impossible to evaluate for research-lab type processes on small (2") wafers and dies fabricated using E-beam lithography. However, as was shown for the 4"

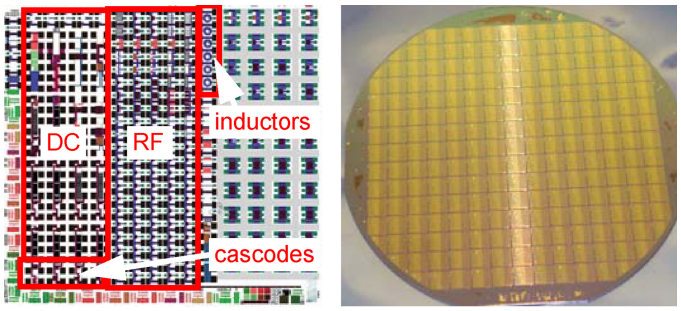


Fig. 4. (a) Magnified view of a typical CNTFET test chip layout ($6 \times 6\text{mm}^2$ reticle size). (b) 4" wafer with fabricated dies. Courtesy RFNano Corporation.

stepper process displayed in Figs. 3 and 4, a quite reasonable uniformity has already been obtained for both DC parameters and RF figures of merit (such as g_m, f_T, power gain) [4], [31].

IV. Device Modeling

A wide range of simulation approaches have been utilized for analyzing the properties and performance of CNTFETs, ranging from atomistic first-principles methods [32], [33] over Schrödinger-Poisson (SP) [34]–[36] and Boltzmann transport equation (BTE) [37]–[40] solvers to compact models [41]–[43]. Common to the existing numerical device simulation methods is their focus on just single-tube devices. Moreover, most approaches assume ohmic S/D contacts and an ideal cylindrical device structure with needle-like contacts. Atomistic methods are capable of detailed investigations on, e.g., contact resistance and functionalization effects [1], but are unsuitable for simulating a practically useful device structure. SP based solution methods are limited to device structures with short channels up to a maximum of about 200 nm due to the computational effort. Especially (time dependent) simulations for the determination of the frequency-dependent two-port admittance parameters are very challenging. For an overview on these methods the reader is referred to the literature [36]. Generally, the often extremely long simulation times of numerical tools limit their suitability for the device design of practically feasible MT transistors fabricated with depreciated lithography tools.

A serious difficulty is the calibration of physical models to measurements, since hysteresis and the high-impedance of single tubes prevent the acquisition of consistent and accurate DC and AC data. There is a sufficient number of adjustable (i.e. unknown) parameters though in the simulators mentioned above that enable obtaining reasonable agreement with experimental results. For the latter, mostly those of the single-tube device in [44] have been used which, unfortunately, provide only (i) a very limited set of DC data without small-signal variables such as the transconductance g_m and (ii) data for a very short channel (50 nm). For practically more feasible devices with longer channels and higher scattering probability,

[1]Functionalization generally means a chemical treatment of the tube surface. For the electronics applications considered here, only the effect of doping is of interest and will therefore be used throughout the rest of the paper.

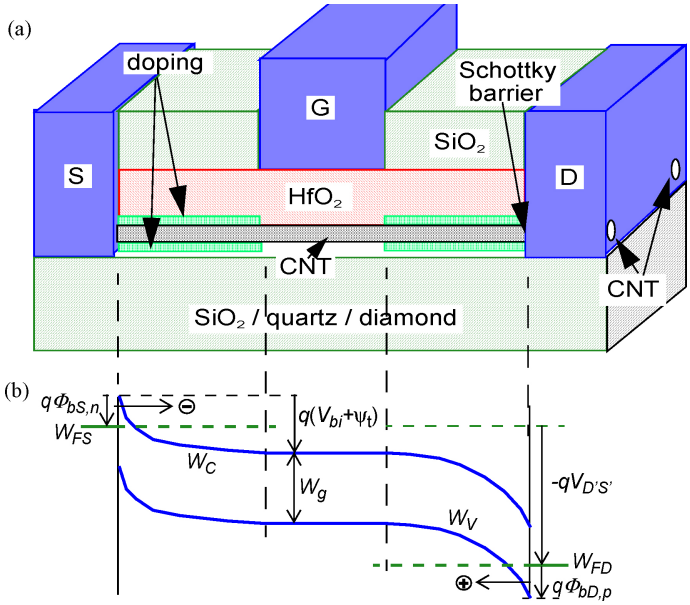


Fig. 5. (a) Schematic cross-section of a top-gate multitube CNTFET. (b) Band diagram for $V_{DS} > V_{GS} > 0$. W_F is the Fermi level of the S or D contact reservoir. $V_{bi} = \Phi_{bS,n} - W_g/(2q)$ is the built-in voltage at the S contact.

the use of a BTE solver appears to be more appropriate. The BTE can be solved either directly [37] or by a Monte-Carlo method [38]. Common to all simulation approaches is the difficulty to find suitable contact models. The approaches range from a simple Schottky barrier model (e.g. [45]) to more elaborated heterojunction based models (e.g. [46]). An excellent survey is given in [47]. In the following the generic term„ Schottky barrier" is used to describe a bias-dependent potential barrier at the ends of the channel.

For designing circuits, compact models are required. Fig. 5(a) shows the schematic structure of a planar multi-tube (MT) RF CNTFET to be modeled. The middle region of the tubes is electrically controlled by the top gate (G) through a thin high-k gate oxide. The S/D contact metal covers or wraps around the CNTs in order to minimize the contact resistance. Since typically a Schottky-barrier is formed at the tube ends leaving the S/D metal (see Fig. 5(b)), the corresponding (channel) access regions between S/D and gate ("spacers") should be doped as highly as possible. However, the tube region underneath the gate should be left intrinsic for minimizing scattering and maximizing carrier modulation by the gate.

Various attempts at deriving compact expressions for current and charge as well as for building a suitable equivalent circuit have been published [41]–[43], [48], [49]–[53] and critically reviewed in [54]. For discussing both the advantages of CNTFET technology and the issues encountered in compact modeling, the most important basic relations are recapitulated below.

A general approach for calculating the electron transport related drain current component of, e.g, a single-tube CNTFET is based on the Landauer equation [55]

$$I_D = \frac{4q}{h} \int_{-\infty}^{\infty} T_n(w)[f_n(W, W_{FS}) - f_n(W, W_{FD})]\, dW \qquad (1)$$

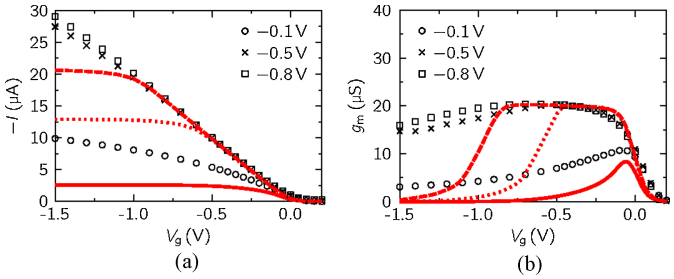


Fig. 6. Comparison of a SP solution (symbols) with equation (2) (lines) as discussed in the text. (a) Drain current versus GS voltage for several V_{DS}. (b) Corresponding transconductance g_m. The SP simulation was adjusted to the experimental results of an 50-nm-long CNTFET [44].

with f_n as the electron Fermi function and h as the Planck constant. T_n (≤ 1) is the electron transmission factor between the bulk S and D contact, which generally includes tunneling through the Schottky-barriers and scattering along the tube. For an energy independent average transmission factor $T_{n,av}$ the remaining integral can be evaluated analytically, leading to the closed-form solution

$$I_D = T_{n,av} G_q V_T \left(\ln\left[1 + \exp\left(\frac{\psi_t^*}{V_T}\right)\right] - \ln\left[1 + \exp\left(\frac{\Psi_t^* - V_{D'S'}}{V_T}\right)\right]\right) \quad (2)$$

with the thermal voltage V_T, the quantum conductance (per tube)

$$G_q = 4q^2/h = 155\mu S \quad (3)$$

and $\psi_t^* = \psi_t - (W_{g1}/2q)$, where Ψ_t is the tube surface potential and W_{g1} is the conduction band edge of the first subband. Fig. 6 shows the results of (1) for a single-tube FET with 50 nm gate length. In order to maximize the accuracy, the tube potential was taken directly from the SP simulation. A reasonable approximation of I_D and g_m can only be obtained for a small V_{GS} range and at higher V_{DS}. Therefore, a bias dependent modeling of $T_{n,av}$ or even an energy dependent expression for T_n is required to describe experimental results [54]. However, approaches such as those in [49], in which a more or less sophisticated analytical expression for $T_n(W)$ is assumed and then is evaluated numerically, require too large a computational effort and are thus not suitable for circuit design.

Assuming the ideal case, i.e., (i) negligible impact of S and D contact as well as of possible doping and oxide charge on the electrostatic potential, and (ii) the same work function for CNT and gate material, the surface potential under the gate is related to the gate voltage through the charge balance,

$$Q_t' = C_{ox}'(V_{G'S'} - \psi_t) \quad (4)$$

with C_{ox}' as gate oxide capacitance per tube length. For a realistic structure, the above relation also needs to include all parasitic capacitances between the gate and the other electrodes.

According to a quasi-ballistic approach, the charge associated with the forward (from S to D) moving carrier density on the tube for the subband v is generally given by

$$Q_{tv}^+(x) = \frac{4q}{2\pi}\int g_v^+(W)dW, \quad (5)$$

where $g_v^+(W)$ is the position and energy dependent non-equilibrium carrier distribution of the right injected carriers. A similar relation can be written for the backwards moving electrons and also for holes. Ignoring all quantum ballistic mechanisms such as tunneling and quantum reflections, an often found approximation (known as "pseudo-bulk approximation") for the forward charge density component is

$$Q_{tv}^+ \approx \frac{4}{3}\frac{q}{\pi a_{cc} W_{tb}}\int_{W_{C,v}} D(W,\psi) f_n(W, W_{FS}) dW, \quad (6)$$

with a_{cc} as the distance between two nearest carbon atoms (0.142 nm), W_{tb} as tight-binding energy ($\approx$3 eV), Ψ as the location dependent tube potential, and $W_{F,S}$ as the source Fermi level. Furthermore, $W_{c,v} = W_{gv}/2 - q\Psi$ is the subband dependent conduction band edge, $W_{g,v}$ is the energy gap of the v^{th} subband, and

$$D(W,\Psi) = \frac{2}{3 a_{cc} W_{tb}} \frac{W + q\Psi}{\sqrt{(W+q\Psi)^2 - (W_{g,v}/2)^2}} \quad (7)$$

is the density of states of the CNT. The tube electron charge in (4) is then given by the sum over the subband contributions.

In the compact modeling literature, the tube charge is obtained either by further simplifications of (6) (e.g. [43]) or by simply using an empirical relation (e.g. [41]). With a compact expression for $Q_t'(\Psi_t)$, (4) typically becomes a nonlinear equation for Ψ_t. As was shown in [54], all these approximations lead to significant errors in Ψ_t, $Q_t'(\Psi_t)$ and I_D. Unfortunately, for realistic transistor operating conditions, there appear to be no experimental data presently available for the bias-dependent tube charge and capacitances, which can be used for verifying the simulation results.

In the absence of suitable physics-based compact analytical expressions for both I_D and Q_t', the best option for enabling analog RF circuit design and CNTFET technology evaluation appears to be the use of empirical formulations such as those in [53]. Corresponding results for RF CNTFETs will be shown later.

As (3) shows, assuming $T_{n,av} = 1$ would yield as the lowest possible impedance of a single tube the quantum resistance $R_q = 1/G_q = 6.45\,\text{k}\Omega$. So far, in fabricated devices, the on resistance has been significantly higher, and the resulting maximum drain current of a single tube FET is at best in the tens of μA. Hence, for RF applications, which typically work in a 50Ω system and where an output power in the mW to W range is required, many tubes need to be connected in parallel. The resulting multi-tube FET can then in principle be scaled toward meeting the desired RF specifications.

Generally, an MT FET consists of an ensemble of s- and m-tubes with (at least) varying diameter and contact resistance per tube. For CVD growth the misalignment also leads to a length variation and possible crossings. Detailed circuit simulator based investigations [56] of MT FET structures employing a compact model for a single s- and m-tube device and taking into account random variations in tube diameter, contact resistance, threshold voltage, misalignment, and crossings led to the equivalent circuit for the internal transistor shown in Fig. 7. It consists of two parallel networks representing the nonlinear behavior of the s- and m-tubes. The

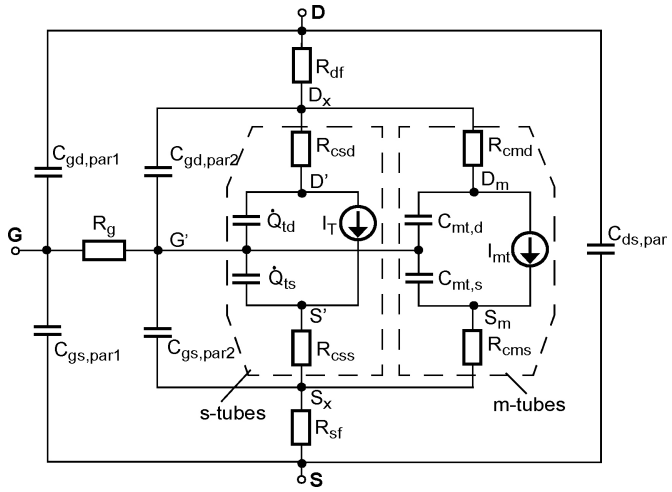


Fig. 7. Large-signal MT CNTFET equivalent circuit, including s-tubes, m-tubes, and parasitic elements. Nodes G', S', D' represent the internal s-tube transistor. Self-heating and hysteresis adjunct networks also exist, but are not shown here.

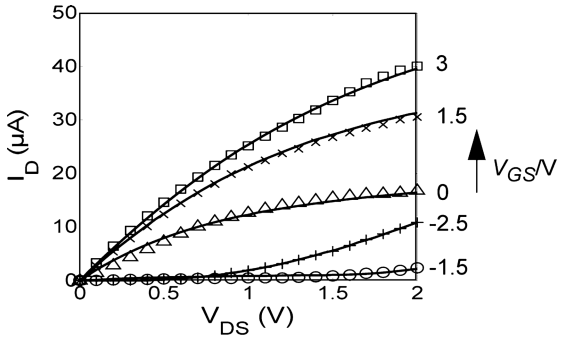


Fig. 8. Output characteristics (V_{GS}/V = −2.5, −1.5, 0, 1.5, 3) of a CNTFET with only two semiconducting tubes. Comparison between measured data (symbols) and compact model (solid lines).

average transfer current I_T and charge portions Q_{ts}, Q_{td} of the s-tubes are modeled by smooth and nonlinear functions of both $V_{G'S'}$ and $V_{G'D'}$ [53], while the *average* current through the m-tubes is a nonlinear function of V_{DmSm}. A bias independent capacitance is assumed for the m-tubes. A separate contact resistance $R_{c(s/m)(s/d)}$ is included for each the s- and the m-tube path. The outer shell of the equivalent circuit contains the parasitic resistances and capacitances from the finger metallization, vias, and connections. Adding temperature dependent formulations and noise calculations as well as thermal and hysteresis adjunct networks completes this geometry scalable large-signal model, which has been implemented in Verilog-A and has already been employed successfully for RF analog circuit design (e.g. [57]).

The model formulation for the DC characteristics has been verified for top-gate transistors with a single or a few tubes. Fig. 8 shows an example for a CNTFET with just two semiconducting tubes. The saturation toward larger V_{DS} values and corresponding high output conductance desired for practical applications is clearly visible, resulting in an intrinsic voltage gain that is typically larger then 15 and increases with decreasing channel length. The increase of I_D for large negative V_{GS} is caused by hole injection, which leads to ambipolar transport.

V. Experimental Results

This section focuses on practically relevant RF CNTFETs. The top-gate processes discussed earlier have yielded devices with varying performance. Reports in the research literature and business news on multi-10 GHz CNTFETs (and even multi-100 GHz GFETs) have led to widespread confusion among the circuit design community regarding the practical suitability of these technologies. It is important to understand that such high frequencies apply to the *intrinsic* device only, where the complete metallization (i.e. every metal visible in Fig. 3(b)) was deembedded and just the CNTs or graphene sheet is left. As a consequence, the reported intrinsic transit frequencies (f_{Ti}) can be up to two orders of magnitude higher than the actual (extrinsic) cut-off frequencies (e.g. [58]). The latter are obtained from deembedding only the pads and thus still include all metal interconnect related parasitics that are required for designing a functional circuit. Therefore, only *extrinsic* HF results are of practical interest and are reported in this paper.

Typical transfer and output characteristics of a state-of-the-art MT CNTFET (fabricated at RFNano Corp.) with 8 gate fingers of 0.4 μm gate length and 50 μm width are shown in Fig. 9. At negative V_{GS}, i.e. below the threshold voltage, a non-zero (off-state) drain current is observed in Fig. 9(a), which is caused by the m-tubes. Above a certain (in this case negative) threshold voltage V_{th} the s-tubes turn on and I_D increases. The sign and value of V_{th} depends on the materials interfacing the tube surface in the channel. For the device shown in Fig. 9, the spacer region was slightly doped and the gate oxide was HfO_2. There is presently only a narrow linear range since the curves start bending most likely due to the following reasons. First, the Schottky barrier at the S end is too wide due to the lack of sufficient tube doping and can thus not be controlled very well by the gate, which is too far away (0.2μm). Second, the tubes are in average even longer than the S to D distance of 0.8μm, giving rise to carrier scattering, especially at high V_{DS}. For non-pulsed measurements, hysteresis also tends to stretch the curve during a positive V_{GS} sweep. Self-heating does not appear to have an impact on I_D though due to the very weak experimentally observed temperature dependence [59], [60].

Note that I_D saturates to a value lower than three times the off-state value that is expected from an s:m ratio of 2:1. In fact, Raman spectroscopy measurements on those wafers showed s:m ratios up to 4:1. The reason for this discrepancy appears to be the lower average maximum current through the s-CNTs compared to that of the m-CNTs. Hence, Raman data, which are often used in the materials science community to characterize the s:m ratio, cannot be used to infer the actual electrical on/off ratio in fabricated transistors.

The output characteristics in Fig. 9(b) exhibit a significant leakage at negative V_{GS} (below V_{th}), which is caused by the m-tubes. Nevertheless, compared to GFETs, a significant modulation of I_D can be observed. The current from the s-tubes increases at low V_{DS} almost linearly (ohmic-like behavior)

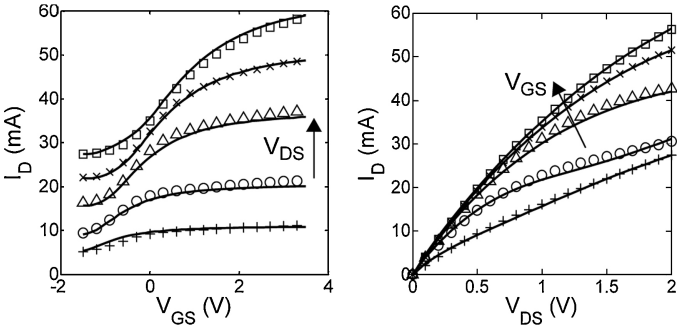


Fig. 9. (a) Transfer characteristics (V_{DS}/V = 0.25, 0.5, 1, 1.5, 2)) and (b) output characteristics (V_{GS}/V = −1.5, −0.5, 0.5, 1.5, 2.5) of a 8*0.4*50μm^2 MT CNTFET. Comparison between measurements (symbols) and compact model (solid lines).

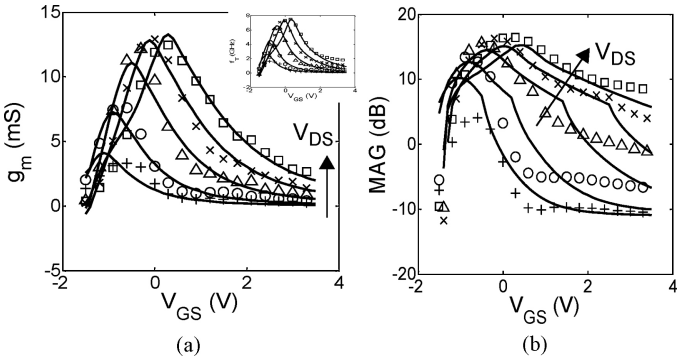


Fig. 10. (a) Transconductance and (b) maximum available power gain (at 0.5 GHz) of a 8*0.4*50μm^2 MT CNTFET at V_{DS}/V = 0.25, 0.5, 1, 1.5, 2). Comparison between measured data (symbols) and compact model (solid lines). The inset in (a) shows the corresponding f_T curves.

but starts to saturate toward higher V_{DS}. This has various causes: (i) Injection of carriers from the drain above V_{GS} - $V_{DS} > V_{th}$. (ii) Carrier scattering at high fields [61]. (iii) The Schottky "point" contact from crossings of m- over s-tubes creates a potential barrier in the s-tubes that, according to our simulations [56], has a detrimental effect on their current if the crossing is located within the G-S spacer or the gate region. (iv) For non-pulsed data, hysteresis [64] may occur from filling more traps.

Fig. 10(a) shows the extrinsic transconductance g_m (i.e. measured at the device terminals). Its peak value initially increases with V_{DS} but saturates toward higher V_{DS}, most likely due to increased carrier scattering. The corresponding maximum available power gain is shown in Fig. 10(b). The peak value of 16 dB at 0.5 GHz, along with 14 dB at 1 GHz [4], is among the best values achieved so far for Carbon-based devices. The curve shape at lower V_{DS} values is again similar to that of g_m, while at higher V_{DS} a somewhat more flat behavior is observed, most likely caused by hysteresis.

In all cases, the compact model mentioned in the previous section yields a reasonable accuracy, thus allowing an evaluation of the impact of certain physical effects and different device designs on circuit performance.

The existence of m-tubes also has a negative impact on the transistor small-signal parameters. Estimating from growth, the total number of tubes in the measured device is about 2400, with about 1900 s-tubes. Thus, the maximum theoretical g_m peak value would be 290 mS, which is much larger than the actually observed value. The causes for this discrepancy are: (i) The Schottky-barrier limits the injection of carriers into the tube. (ii) The large S contact resistance R_{cS} acts as a negative feedback resistor. (iii) The large internal output conductance g_{dsi} from the m-tubes along with R_{cS} and the drain contact resistance R_{cD} further decrease g_m according to

$$g_m = \frac{g_{mi}}{1 + g_{mi}R_{cS} + g_{dsi}(R_{cS} + R_{cD}) + g_{mi}R_{cS}g_{dsi}(R_{cS} + R_{cD})}, \tag{8}$$

where g_{mi} is the internal transconductance.

The presently fastest MT CNTFETs exhibit an *extrinsic* transit frequency of around 10 GHz ([3], [4]). The curve shape is very similar to that of g_m, as can be observed from the inset in Fig. 10(a), indicating an almost bias independent capacitance at the gate node. Beyond the peak of f_T the gate node related capacitance increases significantly due to the onset of optical phonon scattering. Note that similar to existing FET technologies still a rather peaky behavior is observed. Possible causes are the same as those already discussed earlier for g_m. In addition, the charge on the longer tubes in the present devices very likely consists of carriers that experience multiple reflections at both the S and D contacts before leaving the tube. This leads to a more classical Maxwellian velocity distribution and a charge built-up on the tubes.

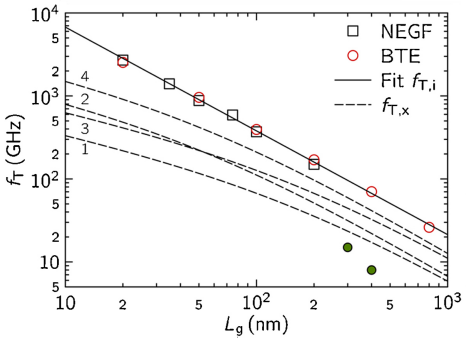
HF noise measurements performed over the past three process development cycles resulted in a drop in noise figure from initially 8 dB to about 3 dB at 1 GHz [62]. This still relatively high value is attributed to the m-tubes and contacts.

Carbon-based devices typically exhibit more or less large hysteresis effects of the order of at least several 100 mV, sometimes even up to several volts, which is often not mentioned in the literature. Such hysteresis effects make the physical understanding and modeling very difficult. It can be shown that hysteresis effects can cause "apparent" linearity [63], i.e. bias independent f_T and g_m characteristics above the threshold voltage, which has not been confirmed by load-pull measurements. Hysteresis is mainly caused by traps located both at the tube interface with the gate oxide and the substrate as well as in the bulk [64], [65]. Eliminating hysteresis requires not only "matched" and defect-free materials but also effective cleaning of the tubes from resist and other electrically undesired materials.

VI. RF Analog Circuits

A fairly limited effort on designing CNTFET based RF circuits has been spent so far since the technology is still in an emerging state. As the best fabricated devices achieve peak operating frequencies of about 10 GHz, it seems appropriate to target RF circuit applications in the range up to about 3 GHz.

Although CVD grown single-tube FETs on SiO_2 show intrinsic voltage gains well above 10 [60], the value decreases to slightly above 1 in corresponding MT FETs due to the metallic tubes (e.g. [4]). Discrete amplifiers built with those CNTFETs showed 11 dB power gain at 1.3 GHz [66] and at



$$f_{Ti} = \frac{21GHz}{(L_g/\mu m)^{1.25}}$$

	8/um	20/um
10 kΩ	3	4
40 kΩ	1	2

Fig. 11. Intrinsic transit frequency projections versus channel length calculated from NEGF [77] and BTE [40] (at V_{GS} = V_{DS} = 0.5 V). The additional extrinsic projections are based on a scalable compact model. For the calculation of the extrinsic transit frequency f_{Tx} (with s:m = 8:1), the tube density and the contact resistance were changed according to the table (curve number). The filled points correspond to experimental data [3, 4].

least 6 dB power gain at 2 GHz [4]. Mixer circuits designed with such CNTFETs achieved 8 dB conversion gain with an LO power of just -2 dBm at 2.4 GHz [57]. These results, which are partially expected from the intrinsic voltage gain, are orders of magnitude better than those of a GFET mixer [67].

VII. Future Prospects

The existing analog RF performance of CNTFETs is still lagging behind the predictions. Achieving the latter, especially accessing the desired intrinsic device features, requires various technological obstacles related to material growth and overall device fabrication to be overcome. A first version of a competitive production-type CNTFET process technology for fabricating integrated RF circuits most likely needs to offer in-place tube growth on 4" wafers with sufficiently thick SiO_2 for RF isolation. From the projections, which will be discussed in more detail below, sub-μm lithography is also required in order to address an RF market up to about 3 GHz. So far though, major factors limiting the RF performance of existing CNTFETs are: (i) low s:m ratio, (ii) high contact resistance, and (iii) S/D Schottky barriers.

For RF analog applications, an s:m ratio of at least 8 is required to achieve an intrinsic voltage gain A_v above 10. Since finding recipes for increasing the s:m ratio during CVD growth on SiO_2 has been slow, with best values of about 4:1 achieved so far, various alternative methods have been pursued. Inexpensive wafer-scale reduction of the number of m-tubes has been shown by, e.g., post-growth removal [68] and chemical decoration making m-tubes less or not conducting [26]. One often cited option is burning m-tubes by self-heating in air [69], which is difficult though to apply across wafer and especially in circuits. Moreover, the m-tube is burned just at a single spot with their stubs still connected to S/D and thus not only contributing to the capacitance but also causing Schottky-barriers when crossing s-tubes in the channel. Other methods proposed in the literature involve heating and burning the m-tubes via microwave [70], UV [71], or laser irradiation [72]. For production, however, the best option still seems to be better growth control.

Contact resistances are still typically in the order of several tens to hundreds of kΩ per tube contact. Recent studies using a graphitic interface layer [73] have demonstrated a significant reduction to about 17 kΩ/contact. Optimizing materials and layer thickness, partially resulting also from investigations on graphene, is expected to bring the contact resistance down further to a range that is comparable to values expected for other types of nanowires [74].

The impact of the Schottky barrier can be significantly reduced by doping the S/D access region or by moving the metal coating close to the gate. Although chemical doping has been demonstrated, its uniformity and thermal stability for production is still questionable. A viable alternative is a thin (few nm) thick metallic or graphitic layer on top of the tubes in the spacer region, preferably self-aligned to the gate (e.g. [75]). This approach comes close to the theoretically investigated ideal structures with "needle" contacts and should enable better access to the intrinsic tube properties such as linearity. While it also leads to shorter channel lengths it introduces though an additional contribution to the parasitic G to S/D capacitance. The impact of the latter can be minimized by significantly increasing the tube density toward the limit of 300 to 400/μm. Shorter channel and gate lengths as well as better tube alignment during growth, using e.g. a buried ferroelectric layer [76], reduce both tube crossing and carrier scattering and thus improve the device performance.

Hysteresis can be significantly reduced and even eliminated by carefully cleaning the CNTs from undesired materials [65]. Any remaining hysteresis may come from lower quality substrate material and gate oxide and, possibly, from *severe* self-heating.

Initial simulations of CNTFETs, based on ideal cylindrical structures and ballistic transport, predicted cut-off frequency values of about 100 GHz/(L_g/μm), resulting in up to several THz for very short channel lengths [8]. However, realistic device structures differ significantly from ideal ones, which are planar, have contacts stacks of finite height, and do not contain highly doped tubes in the access regions. Also, practical constraints for bringing an emerging technology to the market limit, among others, the investment in processing equipment, such as steppers. A re-evaluation of the expected RF performance under realistic conditions is therefore necessary.

As a first step, the intrinsic transit frequency f_{Ti} was extracted from the results of a SP solver using NEGF [77] and of a BTE solver using a Monte-Carlo approach [40] that is based on [38]. The same device structure was simulated employing the same scattering parameters. The only difference was that the NEGF approach in [77] includes Schottky contacts, while the implementation in [40] presently only allows ohmic contacts. The latter lead for low V_{GS} to an overestimation of the transconductance. But for higher V_{GS}, where f_{Ti} was determined, the Schottky barrier thickness is negligible and the current level is determined by the scattering within the channel. Therefore, both approaches give nearly the same results as shown in Fig. 11. The resulting 21 GHz/$(L_g/\mu\text{m})^{1.25}$ is much lower than the initially predicted value of 100 GHz/(L_g/μm) and confirms an earlier analytical estimate [80].

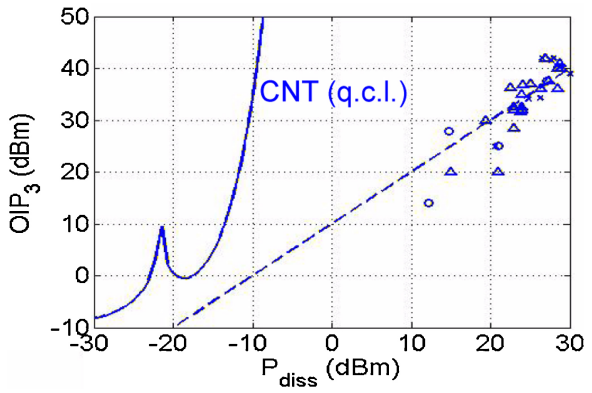


Fig. 12. Low-frequency third-order output intermodulation product (OIP_3) versus power dissipation (P_{diss}) for an ideal CNTFET (solid line) and for various commercial products (symbols) around the dashed line.

In a second step, these f_{Ti} results were combined with parasitics of a realistic structure for calculating the extrinsic value

$$f_{T,x} = f_{T,i} \frac{1}{1 + \dfrac{\overline{C}_{m,t}}{\overline{C}_{s,t}} \Big/ \left(\dfrac{s}{m}\right) + \dfrac{1}{\delta_t} \dfrac{1 + s/m}{s/m} \dfrac{\overline{C}_{gp}}{\overline{C}_{s,t} L_g}} \frac{g_m}{g_{mi}} \quad (9)$$

with δ_t as the tube density, $\bar{C}_{m,t}$ and $\bar{C}_{s,t}$ as the capacitances per gate length L_g of a single metallic and semiconducting tube, respectively, and $\bar{C}_{gp}$ (= 0.28 aF/μm at L_g = 0.25μm) as the parasitic capacitance per gate width. The latter was calculated by a Poisson solver. The intrinsic values $g_{mi} \approx 30$ μS, $g_{di} \approx 2$ μS, and $\bar{C}_{s,t} \approx 0.2$ aF/μm were determined from the BTE simulations.

For evaluating (9), the following assumptions were made: (i) the s:m ratio is 8:1; (ii) a reduction of contact resistance from the present 40 kΩ to 10 kΩ per contact; (iii) an increase of tube density from 6 to 20 tubes per μm gate width. The results are shown in Fig. 11. For a moderate gate length of 0.25 μm, f_{Tx} values between 20 to 80 GHz are predicted, which are comparable to incumbent technologies employed for the 2 to 5 GHz RF market. Therefore, since intentional placement is only possible for MT CNTFETs, the main focus for developing a production-type technology should be on analog and RF rather than on digital applications with single-tube FETs. However, access to better than 1μm lithography is required for competitive performance. The experimental values in Fig. 11 are lower than the predicted ones due to, e.g., the undoped spacer region and random alignment, both leading to a much longer overall channel length than just L_g.

High linearity, which is extremely important for many RF applications, is expected from 1D carrier transport. At the quantum capacitance limit (q.c.l), i.e. for $C_t^{'} = dQ_t^{'}/d\Psi_t \ll C_{ox}^{'}$, Ψ_t follows closely the internal voltage $V_{G'S'}$. Thus, for $V_{G'S'}$ above V_{th} and for sufficiently large $V_{D'S'}$ the drain current from (2) reads

$$I_D = T_{n,av} G_q (\Psi_t - V_{th}). \quad (10)$$

Hence, for bias independent $T_{n,av}$ (e.g. in the ballistic regime and for ohmic contacts), I_D follows $V_{G'S'}$ linearly. Evaluating (2) under these assumptions leads to the curve displayed in Fig. 12. For a given power dissipation, determined by the required 1 dB output power and associated transistor bias point, the OIP_3 of a CNTFET is expected to be much larger than that in bulk technologies. For comparison, the data of a variety of amplifiers fabricated in GaAs and Si/SiGe technology have been inserted. This expected linearity combined with high current carrying capability and weak impact of temperature effects on device performance has made CNTFETs very interesting for analog RF electronic applications. A similar curve had been shown in [78], but without the local peak, which results from the inflection point of g_m, and with a smaller slope for the increase toward higher P_{diss}. So far, this superior linearity has not been demonstrated experimentally though. Major reasons for this are the Schottky barriers and the optical phonon scattering at higher $V_{D'S'}$. The removal of the metallic tubes has only a minor effect as it would shift the curve by about 3 dBm to the left. Note that during operation as a large-signal amplifier the dynamic reduction of the internal drain-source voltage would lead to some reduction in OIP_3.

VIII. Conclusion

An overview on the state of the art of CNTFET technology has been provided with emphasis on production issues and RF analog applications. It was shown that multi-tube multi-finger FETs, which are suitable for 50 Ω RF systems, can be fabricated on 4" wafers employing conventional masks and lithography, and with a yield of around 50%. This along with an accurate compact model enables the design and fabrication of integrated RF CNTFET circuits. Therefore, the authors disagree with the assessment in [74] stating that graphene technology is closer to production than CNTFET technology. This is especially not the case for GNRFETs, which are needed for achieving competitive RF performance, including power gain.

The best fabricated CNTFETs so far show *extrinsic* transit and maximum oscillation frequencies of around 10 GHz as well as a maximum available power gain of slightly above 10 dB at 2 GHz. However, the overall RF performance of fabricated CNTFETs and circuits is still far behind that of both comparable incumbent technologies and predictions based on material properties [8]. This is due to the significant challenges faced in fabrication. The most important issues are the reduction of (i) the number of metallic tubes, (ii) the Schottky barrier width, (iii) contact resistances, and (iv) hysteresis. Possible approaches for better accessing the intrinsic tube properties and achieving competitive RF performance have been discussed in Section VII.

If the presently existing materials and fabrication challenges can be overcome, the electrical performance of CNTFETs is expected to surpass that of graphene FETs [6] and also of Si nanowire FETs [79]. Whether this will also be true for III-V nanowire FETs is difficult to say at this time since that field is still very much in flux. Based on the present development trajectory, the first promising market for CNTFET technology may be RF applications requiring high linearity, such as amplifiers, mixers, and switches, operating up to about 3 GHz.

Finally, if the semiconductor industry is as serious about accessing the superior transport features of CNTs in transistors and circuits as it has been about, e.g., GaAs and GaN based electronics in the past, then it needs to significantly increase the investment into CNTFET process engineering and development of a *manufacturable* technology. Otherwise, the development will remain dominated by research institutes which often do not have the facilities for building practically relevant demonstrators.

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