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Bulk Carrier Contaminations and Their Effects on MOSFETs Under Energy Harvesting Systems

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ABSTRACT Energy harvesters, such as photovoltaic cells, generate carriers in the deep substrate regions; these carriers can affect MOSFETs and deteriorate their performance or even cause malfunctioning. In this study, we discussed the effects of bulk carrier contamination on integrated MOSFETs in the context of energy-harvesting devices. We confirmed that the close integration of MOSFET circuits in a photovoltaic cell causes malfunctioning under strong light illumination. Moreover, numerical simulations revealed that PMOS is highly sensitive to carrier contamination as a forward pn-junction from the bulk-side storage carriers into the NWell region. Furthermore, increasing the distance from the illumination window was not an effective countermeasure, and alternative methods, such as the silicon-on-insulator substrate, n^--substrate, or NMOS logic, should be implemented for such large-scale integration.

INDEX TERMS Analog LSI, energy harvesting, Internet of Things, reliability, silicon-on-insulator.

I. INTRODUCTION

The integration of energy harvesters with large-scale-integration (LSI) chips for standalone operation is essential in the field of Internet of Things [1]. Energy harvesters, such as photovoltaic cells, thermoelectric devices, and piezoelectric resonators, are potential candidates for this integration. In particular, photovoltaic cells are widely used for the development of these devices because of their simplicity over other methods, such as pn-junctions with illumination windows. Moreover, the power density from sunlight is high at 1 kW/m^2, and light illumination is available regardless of the chip location [2].

Currently, standard complementary metal-oxide-semiconductor (CMOS) technologies are used in LSI chips system design. In LSI chips, the element separation technique is crucial for ensuring the intended operation of transistors of NMOS and PMOS, diodes, and other electronic devices. Generally, a p^--substrate is used for CMOS LSIs, and various methods are used to form compatible NMOS and PMOS transistors. One technique involves triple-well technology, which is applied to NMOS to separate its substrate from the surrounding light-doped n^--region [3]. PMOS formation occurs within the NWell region on the p^--substrate to separate the PMOS from other components. Their separation occurs because of reversed pn-junctions from the transistor regions to prevent carriers from escaping to the substrate [4].

However, in these techniques, the carrier concentration in the substrate is assumed to be sufficiently small, as carrier transport from the substrate to the transistors is possible using a forward pn-junction. Therefore, when energy harvesters are integrated and carriers are generated at the substrate, these generated carriers can negatively affect transistor performance [5]. For photovoltaic cells, the concentration of excess carriers depends on the light intensity, and its effect differs depending on the environment, situation, or location of LSI chips. Thus, this carrier generation represents bulk carrier contamination (BCC).

This study discussed BCC effects on CMOS transistors. Experiments were conducted to evaluate the effect of high-intensity light on the CMOS logic. Moreover, a numerical simulation was performed to reveal the BCC effects of various MOS devices and distances from the illumination window to determine the safe operating conditions of this system.

II. BCC EFFECT

BCC occurs when excess carriers are generated in the substrate region. Subsequently, the generated carriers could penetrate the MOSFET regions before recombination, which is facilitated by a long carrier lifetime. As silicon is an indirect bandgap semiconductor, its lifetime can be of the order of milliseconds, and avoiding this problem is challenging. In particular, the diffusion length of the minority carrier L can be expressed as follows:

$$L = \sqrt{D\tau}, \tag{1}$$

where D is the minority carrier diffusivity and τ is the minority carrier lifetime. Given that $\tau = 1$ ms and $D = 27$ cm^2/s, $L = 1643$ μm [6]. Because one side of a general silicon LSI chip is 2–5 mm, this large L value can be critical. Furthermore, D is determined as follows:

$$D = \mu \frac{kT}{q}, \tag{2}$$

where μ is the mobility, k is the Boltzmann constant, and T is the temperature.

The diffusion length differs between the electron and the hole, and semiconductor type especially the direct or indirect bandgap influences it. For example, the hole diffusion length of the direct bandgap semiconductor $GaAs_{1-x}P_x$ was reported as a value of approximately 1.5 μm, which is considerably shorter than that of silicon [7]. Ge nanowires (NWs) have been reported to exhibit diffusion lengths of $4 \sim 5$ μm, and Ge is known to be an indirect bandgap semiconductor [8]. A previous study on gallium nitride (GaN) nanorods revealed that the diffusion length is sub-nm, indicating that GaN is a direct bandgap semiconductor [9]. The diffusion length of an n-GaN film is sub-nm, and the nanorod structure of this system can be independent of this value [10]. The minority carrier in a p-type semiconductor is an electron, which exhibits a considerably larger μ value than that of a hole [11]. Generally, silicon LSI chips are sensitive to BCC effects. A novel diffusion length measurement method based on electron-beam induced current (EBIC) acquisition was reported, and the diffusion length of an electron on silicon LSI was reported to be 10–200 μm [12].

Generally, this BCC effect is crucial for power ICs or RF devices [13], and countermeasures such as substrate thinning [14] have been proposed. Large-power operations generate numerous excessive carriers through impact ionization [15], and such generated carriers can cause latch-up. Furthermore, temperature affects impact ionization [16]. However, when a silicon substrate is illuminated with light, several carriers can be directly generated, which is another mechanism causing latch-up.

Fig. 1 details an example of an energy-harvester-compatible system designed using a 0.18 μm CMOS process LSI. The system detects the light intensity using a photovoltaic cell and a comparator circuit by detecting the open-circuit voltage (V_{OC}) of the photovoltaic cell. Because the input impedance of the MOSFET is sufficiently

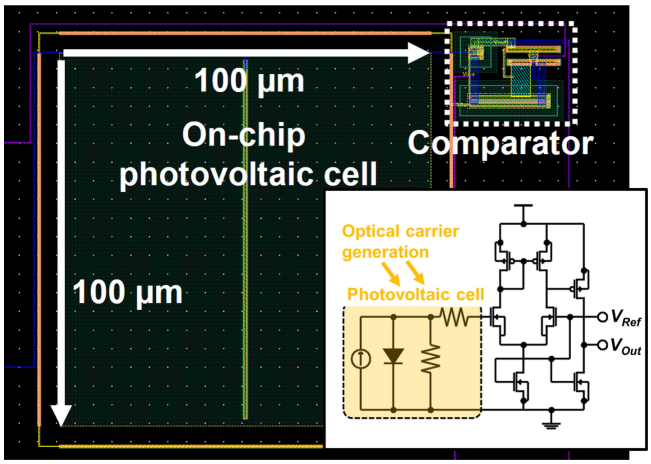

FIGURE 1. Example of an energy-harvester-compatible system involving a photovoltaic cell and a comparator integration [17].

large, the photovoltaic cell is always open [17]. Fig. 2 displays the experimental validation of the BCC problem for the comparator. We tested two conditions, namely, a one-chip system that includes both an on-chip PV cell and a comparator and a two-chips system that separates an on-chip PV cell and a comparator into various chips. This experiment investigates how light illumination affects the surrounding transistors with various intensities. The one-chip configuration is negatively affected by the illumination, whereas the two-chip configuration is unaffected. In the one-chip system, an unintentional output was observed under solar light illumination, and a higher comparator switching voltage V_{th} was observed compared with the two-chip configuration for all illumination conditions. Under solar light illumination, a strong intensity was generated by many carriers such that a larger switching voltage appeared. Considering previously obtained experimental results for these systems [17], the two-chip system exhibits a performance similar to the estimated system operation for an on-chip PV cell, and the mixed comparator system exhibits a potential defect. Fig. 1 displays that the distance between an on-chip photovoltaic cell and a comparator is on the order of μm. Therefore, these results indicate that the optically generated carriers caused a transistor malfunction in the off-state. Optically generated carriers contaminate chip substrate and if those carriers penetrate into transistors, the transistors malfunction, as observed in Fig. 2(a). Placement of the PV cell on a different chip (see Fig. 2(b)) successfully eliminated the BCC effect, and expected operations of the system. Therefore, the BCC originating from optically generated carriers becomes a critical problem in IoT-oriented chip designing.

III. SIMULATION MODELING

The BCC effect on each NMOS transistor (with and without triple wells) and PMOS at various distances from the illumination window were evaluated through simulations, as illustrated in Fig. 3. As mentioned in Fig. 3, the simulation emulates transistors' operations at 1-chip configuration to

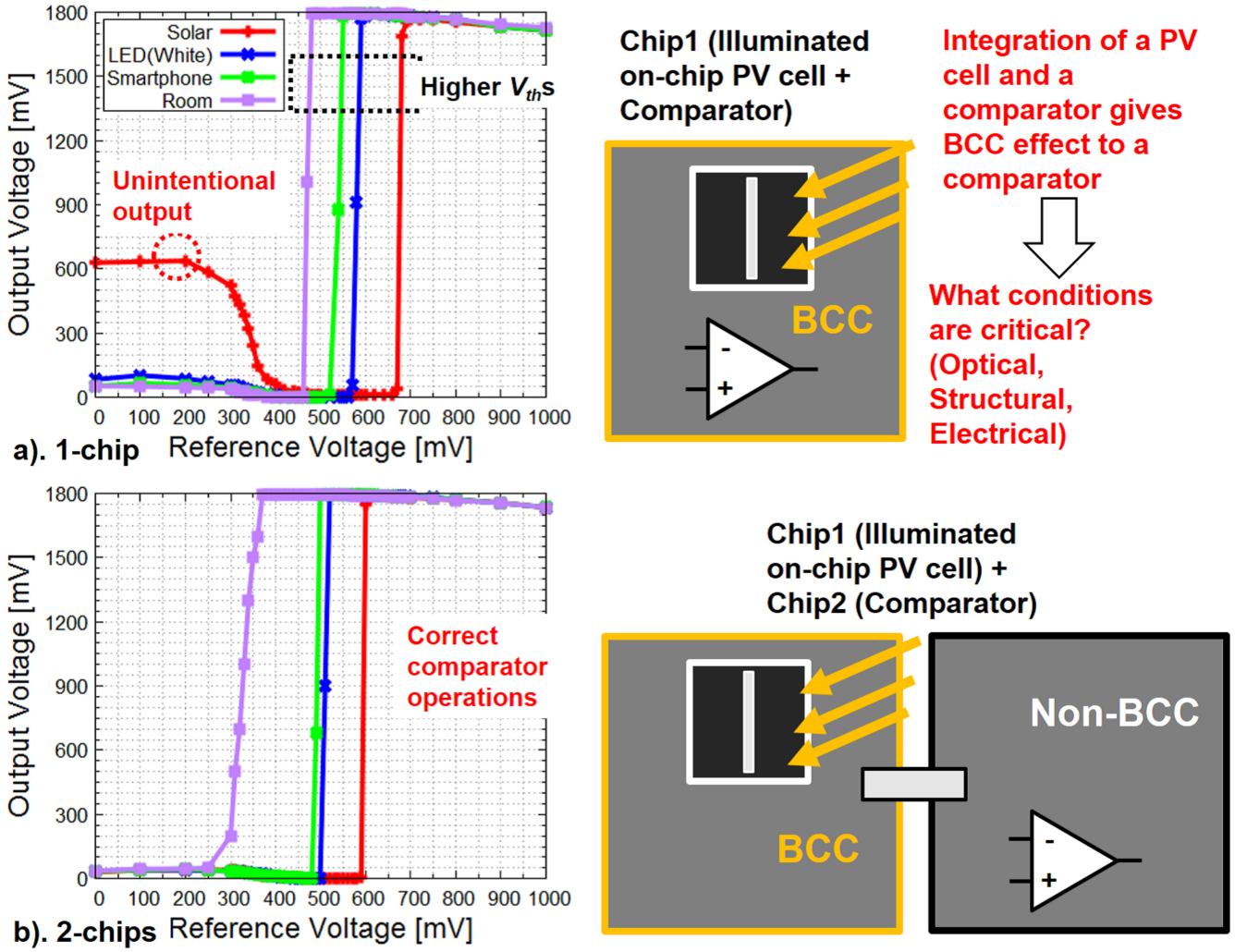

FIGURE 2. Experimental demonstration of example of the BCC problem on a comparator with an unintentional output at off-state, a) a one-chip configuration, b) a two-chip configuration; a one-chip configuration is displayed in the upper graph with higher V_{th}s and a two-chip configuration is depicted in the lower graph.

TABLE 1. Simulation model parameters.

Physics	Value
CMOS gate length	0.18 μm
Bulk doping concentration	1×10^{16} cm^{-3}
Bulk thickness	180 μm
N(P)SD doping concentration	1×10^{20} cm^{-3}
N(P)SD thickness	0.1 μm
NWell doping concentration	5×10^{16} cm^{-3}
NWell thickness	1 μm
DeepNWell doping concentration	5×10^{16} cm^{-3}
DeepNWell thickness	1.5 μm
Bulk lifetime	1 ms
Temperature	300 K
Carrier recombination	SRH, Auger
Silicon/Oxide SRV	10 cm/s
Silicon/Metal SRV	10^6 cm/s

see the BCC effects. The Sentaurus technology computer-aided-design (TCAD, Synopsys, Inc.) system was used for these simulations [18]. Table 1 summarizes the simulation modeling parameters used in this study. The illumination spectrum was AM1.5G sunlight [19]. Moreover, the illumination window had a 10-μm width. We defined d as the horizontal length between the illumination window and the transistor device location, and the generated carriers reached the transistor after undergoing d-length carrier transport. Quasi-stationary DC analysis of the transistor performance was simulated by solving Poisson's equation and the current continuity equations of electrons and holes with self-consistency.

The standard CMOS process parameters are not the same as those of previous studies [20], [21]; however, this study reveals the effects of BCC on transistors, and therefore, these variations do not affect our evaluation. Additionally, the standard CMOS process parameters completely differ among various fabrication processes.

The objective of the simulation is to understand which parameters of the transistor is responsible for malfunction in Section II. Evaluations of transistors with the nearby illumination emulate each transistor's operations on a 1-chip

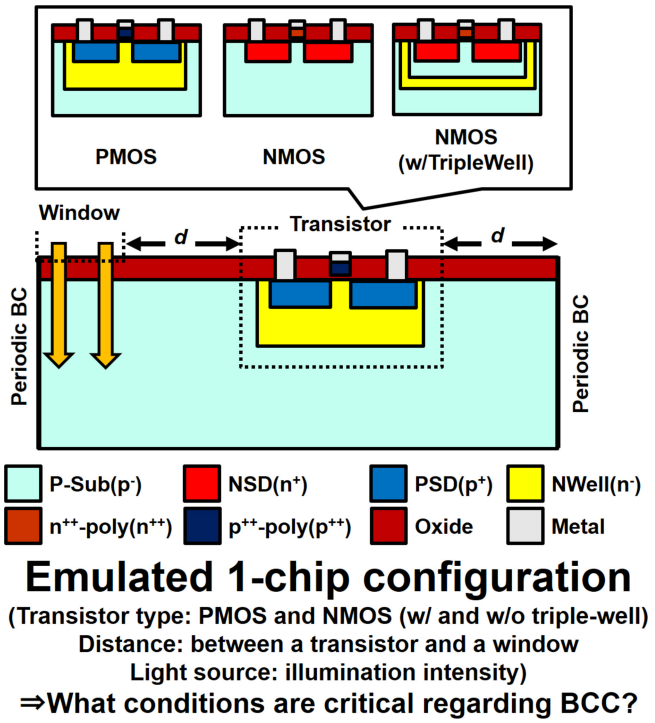

FIGURE 3. Simulation model evaluated in this study: three transistors with various *d* values.

configuration; therefore, finding malfunctions on this analysis is useful to address a BCC problem. The analysis aims to reveal the optical (illumination intensity), structural (the distance between the window and the transistor) and electrical (transistor type) conditions for the BCC to become critical.

IV. RESULTS AND DISCUSSION

A. EVALUATIONS OF BCC

First, the effect of distance d between the illumination window and transistor, as discussed, was evaluated under 100,000 lux illumination. Fig. 4 displays the NMOS performance of the systems with and without triple wells with various d values. Comparing these systems, the triple-well structure prevented the BCC effect, as few dependencies toward d in the off-state were present. By contrast, the system without triple-well NMOS exhibited some off-current increases under small d values. However, the off-current increases were not severe, even for the system without triple-well NMOS, which implied that the NMOS was robust against the BCC effect.

Fig. 5 displays the PMOS performance for various values of d. Although similar off-current increases were present, they were considerably larger than those in NMOS, and an approximately ten-times larger off-current was observed at $d = 0$ μm compared with that at $d = 1$ mm.

The results in Figs. 4 and 5 demonstrate two critical problems; the increased I_{Off}s and then the varied threshold voltages V_{th}s of transistors. The increased I_{Off} provides the closed circuits to unintentional on-current as observed in

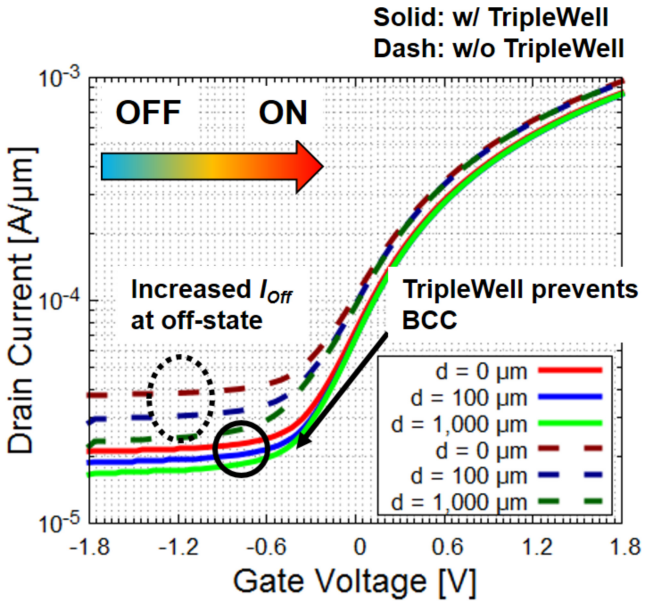

FIGURE 4. Drain current as a function of gate voltage on NMOS with and without a triple well system for various *d* values.

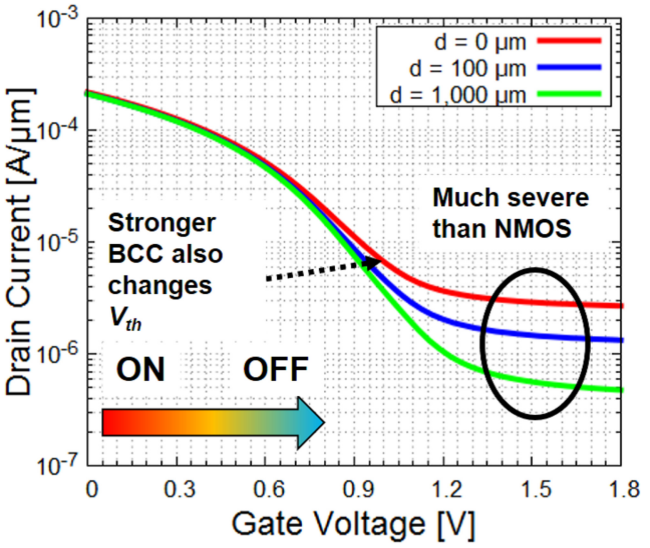

FIGURE 5. Drain current as a function of the gate voltage on PMOS for various *d* values.

Fig. 2(a), and this pushed-up I_{Off} worked to decrease V_{th}. Therefore, the lower switching voltage of a comparator was observed in Fig. 2(a). The effect appears critical on a PMOS transistor.

Fig. 6 displays a comparison of the off currents of three MOSFETs for various d values. PMOS becomes sensitive to d with the increase in d, which indicates that PMOS is severely affected by BCC. For NMOS, the BCC effect is less severe, especially for the NMOS with a triple-well, where the transistor is electrically protected.

B. OPTICAL FACTOR

Figs. 7 and 8 display the effects of the illumination intensity on the performances of systems with $d = 0$ μm. For NMOS

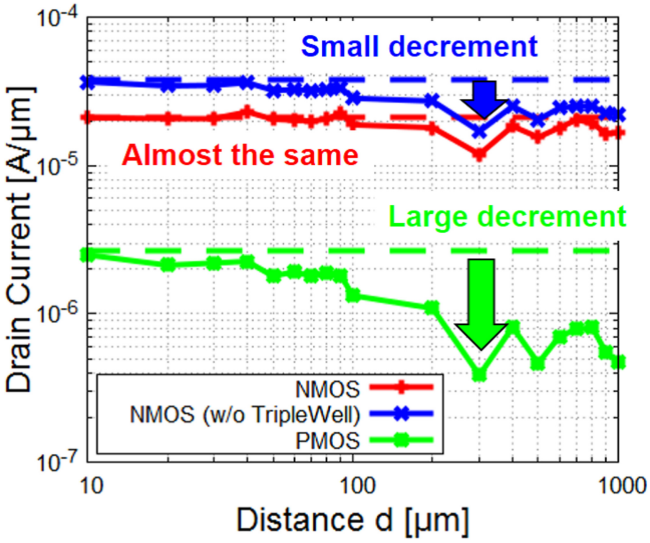

FIGURE 6. Off currents of transistors as a function of distance d (the dash lines express the off currents at $d = 0$).

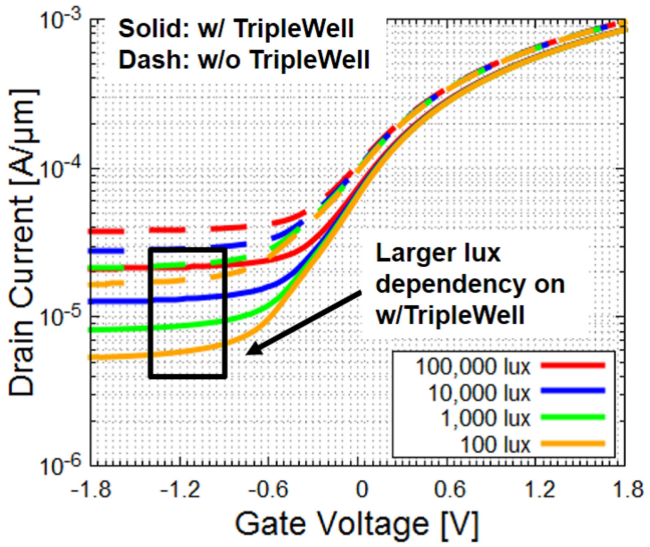

FIGURE 7. Drain current as a function of the gate voltage on NMOS with and without a triple well for various illumination intensities of 100–100,000 lux.

(Fig. 7), the structure with the triple-well exhibited a larger dependency on the illumination intensity than the structure without the triple well. Considering the PMOS results (Fig. 8), a 100-lux illumination is adequate for avoiding affecting transistor operations, as the same off-current was obtained. In the simulation, no thermal carrier generation at the substrate was considered (and thermal carrier generation is considerably smaller than optical carrier generation. Thus, its effect is negligible.) Therefore, an extremely small off-current can be obtained when illumination is not applied to this system.

C. COUNTERMEASURES

The simulation results indicate that the BCC effect is strongly present in PMOS operations. The light illumination generates

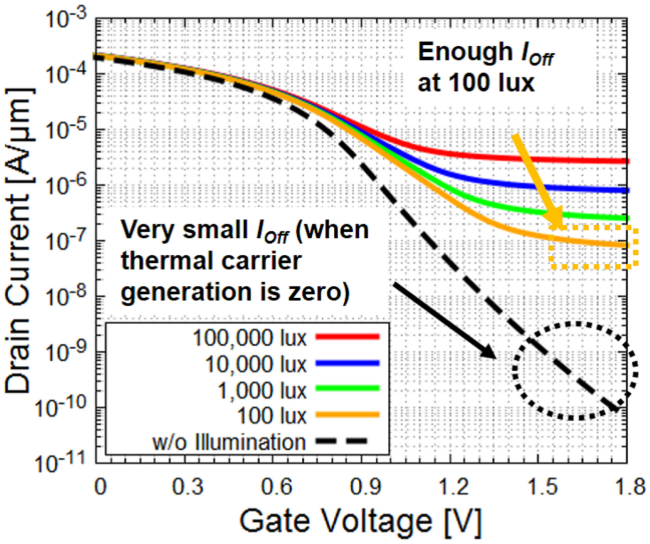

FIGURE 8. Drain current as a function of the gate voltage on PMOS for various illumination intensities of 100–100,000 lux.

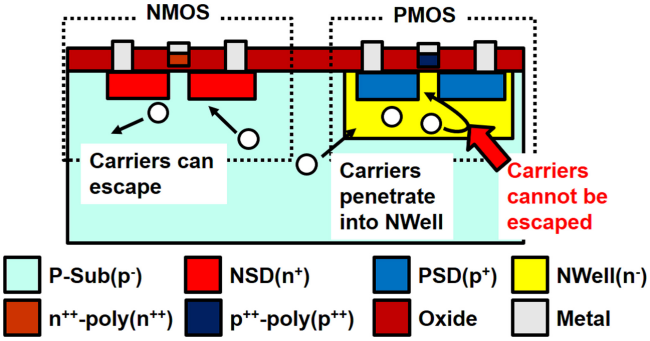

FIGURE 9. Various BCC effects on NMOS and PMOS systems.

both the electrons and holes simultaneously, and most of the substrates are p-type systems such that the electrons are minority carriers. Considering the diffusion length defined by Eq. (1), the presence of both electron- and hole-type carriers can negatively affect transistors. A reason for this phenomenon is that the NWell system forms a reversed pn-junction (NWell/P-Sub), which stores the penetrated carriers as the carriers cannot escape from the NWell region to P-Sub, increasing the off-current. The NMOS without the triple well also exhibits BCC; however, the penetrated carriers can escape from the NMOS region because this region is continuous with the substrate such that the BCC effect can be minimized (see Fig. 9). These NWell kept carriers cause a stronger BCC effect on PMOS. Fig. 7 displays a larger dependence on the illumination intensity for the triple-well structure, which indicates that the triple well system functions as a carrier keeper.

The obtained results indicate that increasing the distance from the illumination window is not an effective method of avoiding BCC effects as the diffusion length in silicon is long (on the order of millimeters, as evidenced by Eq. (1)). A silicon-on-insulator (SOI) substrate can be used

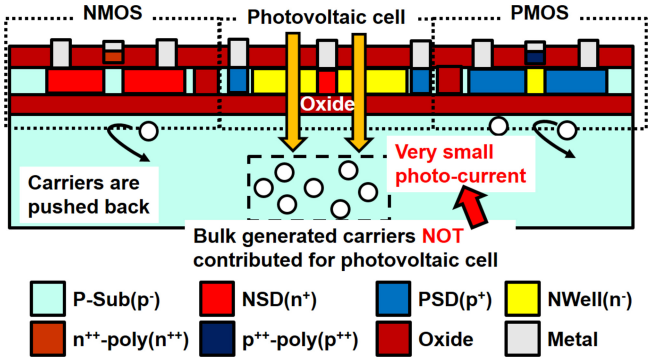

FIGURE 10. Advantages and disadvantages of using a silicon-on-insulator (SOI) substrate.

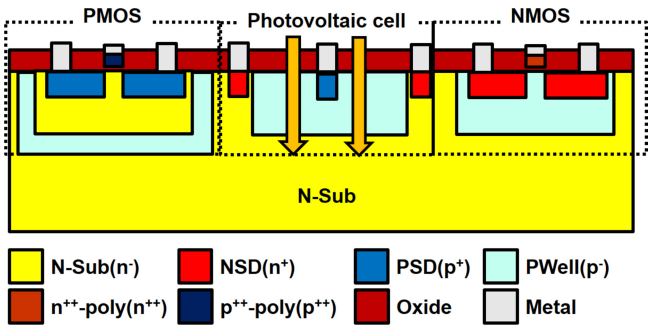

FIGURE 11. n-substrate usage with NMOS, PMOS, and on-chip photovoltaic cells.

to overcome this limitation, and a fully depleted SOI (FD-SOI) can be used to completely isolate the transistors from the substrate to prevent carrier penetration. However, SOI substrates have several limitations because they are expensive and the use of an SOI reduces the optical path length (i.e., the absorber) in a photovoltaic cell, and its output performance can drastically decrease. Fig. 10 illustrates this concept, where the effects of BCC are nullified, but the photocurrent of the photovoltaic cell deteriorates. Another countermeasure is to use an n-substrate because PMOS is severely affected by BCC, and applying a triple well system to PMOS can suppress BCC [22]. Moreover, n-substrates are more expensive than the p-substrate, and the n-substrate CMOS process requires specialized techniques. Therefore, selecting the correct CMOS process is challenging. Fig. 11 illustrates an integrated NMOS, PMOS, and photovoltaic cell on an n-substrate. Alternatively, separating photovoltaic devices from LSI blocks and creating a system with dual chips can be used to overcome the aforementioned limitation of these systems. However, this solution requires large costs and areas, and connecting chips should be used. A final countermeasure is to design using "NMOS logic" and avoid using PMOS transistors. However, NMOS logic has numerous limitations in the design of LSI systems. Table 2 summarizes the advantages and disadvantages of each countermeasure to guide the selection between these systems.

TABLE 2. Comparisons of countermeasures against BCC.

Method	Advantage	Disadvantage
SOI substrate	Strong element separations	Expensive cost Shorten optical path
n-substrate	Stronger PMOS protection	Reduced choice of processes
Multi chips	Complete separation	Large costs Connection is required
NMOS logic	Avoiding PMOS usages	Design restrictions

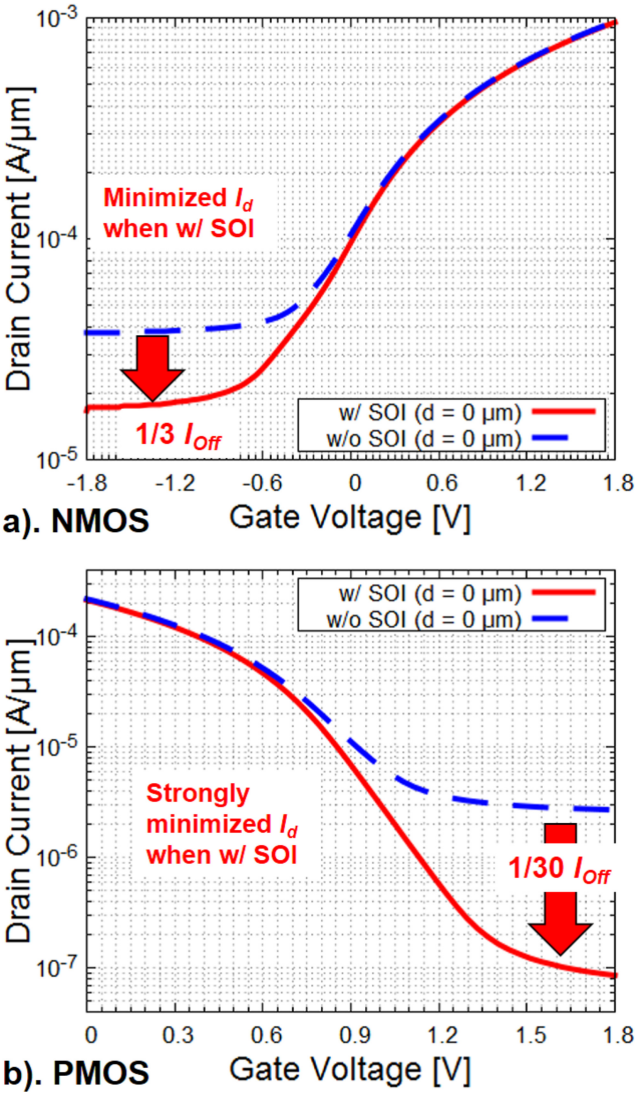

FIGURE 12. Drain currents as a function of the gate voltage on NMOS and PMOS systems with and without an SOI layer; a) NMOS b) PMOS.

To evaluate the effect of the SOI layer, we conducted simulations using an SOI layer thickness of 0.1 μm. These simulations targeted NMOS (without triple-well) and PMOS systems with $d = 0$ μm. Fig. 12 displays the drain currents of the NMOS and PMOS systems with and without an SOI layer. Both in the NMOS and PMOS systems, the presence of the SOI layer resulted in decreases in the off-current, especially in PMOS system of 1/30 I_{Off} and 1/3 I_{Off} even in NMOS system. The results ensured that using SOI can completely eliminate the BCC effect even when $d = 0$ μm.

V. CONCLUSION

BCC effects on energy-harvester-integrated LSI chips were investigated. The results indicated that PMOS was highly sensitive to BBC effects because NWell retained the penetrated carriers. Countermeasures to reduce these unwanted effects were considered, advantages and limitations of various methods were highlighted. Designers should select an appropriate method to avoid or minimize the effects of BCC.

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