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Physics-Based Compact Model of Independent Dual-Gate BEOL-Transistors for Reliable Capacitorless Memory

LIHUA XU[1,2], KAIFEI CHEN[2,3], ZHI LI[2,3], YUE ZHAO[2,3], LINGFEI WANG[2,3] (Member, IEEE), AND LING LI[2,3] (Senior Member, IEEE)

1 School of Microelectronics, University of Science and Technology of China, Hefei 230026, China
2 State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, China
3 School of Integrated Circuits, University of Chinese Academy of Sciences, Beijing 100049, China

CORRESPONDING AUTHOR: L. WANG (e-mail: wanglingfei@ime.ac.cn)

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ABSTRACT Capacitorless DRAM architectures based on Back-End-of-Line (BEOL)-transistors are promising for long-retention, high-density and low-power 3D DRAM solutions due to its low leakage, operational flexibility, and monolithic integration capability. Different from classical silicon-based devices, in-depth studies on the performances of nanoscale multi-gate transistors (e.g., a-InGaZnO-FET) are still barely conducted for physical description, due to the complicated multi-gating principle, finite-size effects on transport, increased variation sources and enlarged parasitic effect. Hence, high-performance multi-nanoscale (down to $\sim$ 50 nm) dual-gate a-IGZO transistors are fabricated, and a physical compact model is developed based on the surface potential for dual-gated coupling and the disordered transport with finite-size-correction. The short channel behaviors on sub-threshold swing, mobility and threshold voltage are investigated, and contact effects are validated by the transfer-line method (TLM). Regarding the specific challenge of dual-gate alignment, possible misalignment and parasitic effects on multi-device fluctuations are important of large-scale circuit design and analyzed by TCAD simulations. Besides, the bias-temperature instability (BTI) has been comprehensively investigated. In awareness of the above effects, this model bridges fabrication-based material properties and structural parameters, assisting in a threshold fluctuation-resistant operation scheme for capacitorless multi-bit memory, showing a great potential in future monolithic integration circuit design using BEOL-transistor.

INDEX TERMS BTI, compact model, contact effects, DRAM, independent dual gate a-IGZO-FET, disorder semiconductor, hopping, transfer-line method.

I. INTRODUCTION

Amorphous In-Ga-Zn-O (a-IGZO) exhibits promising attributes for Monolithic 3D integration (M3D), primarily owing to its compatibility with the Back-End-of-Line (BEOL) process [1]. The a-IGZO field-electric-transistors (FETs) take advantage of moderate mobility and ultra-low leakage current due to the disordered transport mechanism and ultra-wide energy band [2], [3], [4]. This presents a promising solution to circumvent the limitations associated with memory capacitance and cell coupling prevalent in conventional 1T1C dynamic random access memory (DRAM) technology [5]. By utilizing the gate dielectric layer of the transistor as a storage node capacitor, it offers higher storage density and longer data retention time in capacitorless memory design [6]. Due to the increasing demand for dense memory design, the scaling down of BEOL-transistors is highly required. However, the sub-threshold property and reliability issues of a-IGZO-FET arise with the scaling-down due to the inferior gate controllability [7], [8], [9]. Variations in material composition and fabrication process

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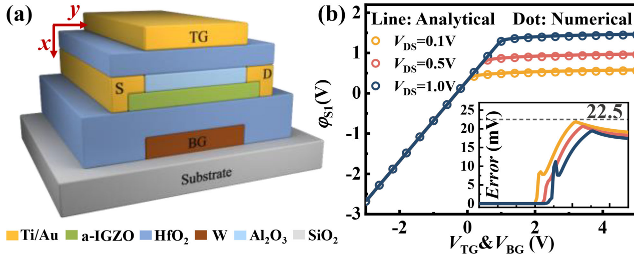

FIGURE 1. **(a) Schematic illustration of the IDG a-IGZO FETs with a thickness of ∼5 nm. (b) Agreement between analytical and numerical results of back gate surface potentials at different V_{DS} with errors in the inset. V_{TG} & V_{BG} denotes DG-synchronized-sweep with the same voltage.**

contribute to the changes in density of states, and further induce reliability issues in sub-threshold region. It hindered advanced large-scale applications, especially in multi-bit data processing, which is sensitive to device instability [10].

Recently, independent dual-gate (IDG) technology has exhibited the potential to overcome the limitations [11], [12], which are attributable to operational flexibility, adaptive threshold and excellent gate controllability. Nevertheless, when considering complicated effects of dual-gate coupling, disordered transport and sub-threshold degradation at the nanoscale, the compact modeling of BEOL-devices is still incomplete to satisfy future reliable M3D circuit design [13]. To tackle with this issue, the high-performance dual-gated a-IGZO-FET is fabricated and modeled to enable cross-layer co-design. On the basis of Newton correction method and dual-gate coupling effects, an accurate surface potential (SP)-based physically compact model is developed to support three operation modes. Particularly, the percolation-theory-based transport mechanisms have been corrected considering the finite-size effects on the amorphous channel [14]. With this model, the critical effects of short channel effects, top gate misalignment, multi-device fabrication variability, bias-temperature instability (BTI), and parasitic effects are investigated. Based on the above effects, this model enables compensation for the attenuation of voltage at the charge storage node (V_{SN}) resulting from fabrication process variations, thereby facilitating accurate and tolerant multi-bit programming. Thus, robust design metrics of monolithic integration circuits can be explored by considering the fabrication-related material and structural parameters.

II. DEVICE FABRICATION AND MODELING

A. DEVICE FABRICATION

Fig. 1(a) shows the schematic illustration of the fabricated IDG-IGZO FET with a channel width of 200 nm and a channel length of 50 nm. Firstly, layers of 20 nm W (bottom gate), 4.5 nm HfO_2, and 5 nm a-IGZO were deposited and patterned. The S/D patterns were lithographed by electron beam lithography (EBL), then 10/30 nm Ti/Au was deposited by the E-beam evaporator and lifted off. Next, dual stacks of 2/5 nm Al_2O_3/HfO_2 were deposited as the passivation layer and top-gate dielectric. Finally, the top gate was patterned and lifted off. Fabrication process details can be found in our previous publication [11].

B. NANOSCALE SURFACE POTENTIAL CALCULATION

Due to the conduction band-edge fluctuations in the a-IGZO material [15], disorders (e.g., localized states, etc.) are generally present near or below the conduction band-edge. Therefore, the amorphous channel carrier density is dominated by the density of localized and extended states, closely related to changes in IGZO composition [16]. Based on the Fermi-Dirac distribution, the Poisson equation is given as Eq. (1), shown at the bottom of the page where $\Phi_{TA}=k_0T/q$, $\Phi_{TA}=k_0T_A/q$. And φ is the potential in the channel layer, ε_S is the dielectric constant of semiconductor, q is the elementary charge, N_T is the total concentration of localized states, τ_0 is the lifetime of carriers, v_0 is the attempt-to-escape frequency, k_0 is the Boltzmann's constant, and T_A is the characteristic temperature of the exponential DOS. The first and second terms in the right of Eq. (1) represent the localized state and the extended state carrier concentrations, respectively. The defect-related carrier concentration dominates the subthreshold region [17].

Referring to the mathematic manipulation in [17], based on boundary conditions of bottom/top channel surfaces (Eqs. (2), (3)), the original transcendental equation for IDG-FETs can be obtained in Eq. (4). shown at the bottom of the page

$$Q_{BG} = C_{OXB}(V_{BG} - V_{BF} - \varphi_{BG}) = - \left.\varepsilon_s \frac{\partial \varphi}{\partial y}\right|_{y=0} \quad (2)$$

$$Q_{TG} = C_{OXT}(V_{TG} - V_{TF} - \varphi_{TG}) = \left.\varepsilon_s \frac{\partial \varphi}{\partial y}\right|_{y=t_s} \quad (3)$$

where $q_1 = Q_{TG}/(C_{OXT} \cdot \Phi_{TA})$, $q_2 = Q_{BG}/(C_{OXB} \cdot \Phi_{TA})$, $A_0 = 2 \quad qN_T\varepsilon_S \cdot ((\pi T/T_A)/sin(\pi T/T_A)) \quad \Phi_{TA}$,

$$\frac{\partial^2\varphi(x,y)}{\partial x^2} = \frac{q}{\varepsilon_S}\left[\left(\frac{\frac{\pi T}{T_A}}{\sin\left(\frac{\pi T}{T_A}\right)}\right)\cdot N_T e^{\frac{(\varphi-V)}{\Phi_{TA}}} + N_T v_0 \tau_0 e^{\frac{(\varphi-V)}{\Phi_T}}\right] \quad (1)$$

$$FF(\varphi_{S1}) = \left[k_1q_1 + \alpha\cdot\coth\left(\frac{\alpha}{2} + t_s\cdot\delta\right)\right](k_1q_1 + k_2q_2) - A_0 exp\left(\frac{V_{G1} - \varphi_{S1}}{\Phi_T}\right) - B_0 exp\left(\frac{V_{G1} - \varphi_{S1}}{\Phi_{TA}}\right) \quad (4)$$

$B_0 = 2\ qN_T\varepsilon_S v_0\tau_0/\ \Phi_{TA}$, t_s is the active layer thickness, Q_{BG} and Q_{TG} are charge densities, C_{OXT} and C_{OXB} are gate capacitances, V_{BF} and V_{TF} correspond to the flat-band voltages of the top and bottom gates, respectively, and α is closely related to the interfacial coupled electric field.

The segmentation method is employed in the sub-threshold and above-threshold regions to simplify the *Coth*/*Csch* functions and decouple transcendental equations for the analytical solution of surface potential at the nanoscale. In the subthreshold region, the free charge density is approximately zero, according to this equivalent capacitance model, and φ_{ss} can be obtained by

$$k_{eq} = 1/(1 + 1/k_1 + 1/k_2) \tag{5}$$

$$\varphi_{ss} = \left(k_2(k_1V_{G1} + V_{G2}) + k_{eq}(V_{G1} - V_{G2})\right)/k_2(1 + k_1) \tag{6}$$

where k_1=C_{OXT}/C_S, k_2=C_{OXB}/C_S, V_{G1}=V_{TG}-V_{TF}, and V_{G2}=V_{BG}-V_{BF}. In the above-threshold voltage region, *Coth/Csch* functions are approximated by zero, the transcendence equation is transformed into Eq. (7), shown at the bottom of the page and φ_{sn} is easily obtained as Eq. (8), shown at the bottom of the page here, q_2 can be expressed as a function of φ_{S1}, $q_2 = (V_{G2}$-$\varphi_{S1})/\Phi_{TA} + 2ln(k_1q_1)$. By connecting φ_{sn} and φ_{ss}, an initial analytic solution is given by a smoothing function and its accuracy is further improved by the 1st-order Newton's correction series in

$$\begin{cases} \Delta F = -FF/FF^{(1)} \\ \varphi_{S1} = smothf\{\varphi_{SS}, \varphi_{Sn}\} + \Delta F \end{cases} \tag{9}$$

where *smothf(x)* is the smoothing function that connects piecewise surface potentials. Finally, the analytical solutions of the channel surface potential φ_{S1} at different V_{DS} agree with numerical results, as described in Fig. 1(b), and the error is less than 22.5 mV. And the numerical results were obtained by iterative calculations of Eq. (1) using Wolfram Mathematica numerical computation software.

C. MOBILITY WITH CONTACT EFFECTS AND CURRENT MODEL

The fluctuation of the mobility edge in the amorphous state of a-IGZO leads to localized states in the band gap and potential barriers in the extended state [3]. As for the intrinsic transistor properties, carrier density and T-dependent transport in an amorphous channel have been reported in [18]. As the size of TFTs scales down to the nanoscale, the effects of the extended-state potential barrier, localized-state characteristic temperature, and gate coupling become increasingly significant and can no longer be ignored. On the classical percolation and hopping mechanisms, the mobility model (Eq. (12), (13), (14)) includes finite-size effects while also considering the coupled carrier density for dual-gate modulation [12]. Due to the obvious contact resistance (R_C) effect in the ultra-scaled device [19], [20], the applied voltage drop in the contact area is much larger than that in the channel, which causes mobility degradation. The mobility considering R_C is incorporated into Eq. (13).

$$\mu_P = \mu_b A_P(V_{G1} - V_{P1} + V_{G2} - V_{P2})^{4(D-W/D)} \tag{10}$$

$$\mu_V = \mu_0 A_v(V_{G1} + V_{G2})^a \tag{11}$$

$$1/\mu_{EF} = 1/\mu_P + 1/\mu_V + 1/\mu_{coup} \tag{12}$$

$$\mu_{EF_{CON}} = \mu_{EF}/(1 + \theta\mu_{EF}R_C(V_{GS} - V_T)) \tag{13}$$

where μ_b and μ_0 are constant mobility terms for percolation and hopping, W/D is the spatial coherence ratio of the potential barriers, $V_{P1,2}$ is the transition voltage, A_P and A_V are related to N_T and T_A, and θ is related to the electrode contact length. Moreover, based on Pierret and Shields' theory [21], combined with μ_{EFCON}, the Pao-Sah current integral equation is solved to obtain

$$I_D = \frac{\mu_{EFCON}}{L/W}\left\{\begin{array}{c} C_{OX1}\left[V_{Gf}(\varphi_{D,1} - \varphi_{S,1}) + \frac{1}{2}\left(\varphi_{D,1}^2 - \varphi_{S,1}^2\right)\right] + \\ C_{OX2}\left[V_{Gf}(\varphi_{D,2} - \varphi_{S,2}) + \frac{1}{2}\left(\varphi_{D,2}^2 - \varphi_{S,2}^2\right)\right] + \\ 2\Phi_{TA}\left[\begin{array}{c} C_{OX1}(\varphi_{D,1} - \varphi_{S,1}) + C_{OX2}(\varphi_{D,2} - \varphi_{S,2}) \\ +AF \cdot N_T t_s e^{\Phi_{TA}V_{Geff}} \end{array}\right] \end{array}\right\} \tag{14}$$

III. RESULTS AND DISCUSSION

A. MODEL VALIDATION

Transfer curves on a logarithmic and linear scale at different V_{TG} are simulated in Fig. 2(a), which shows the great potential of threshold modulation. For IDG devices, under the influence of the bottom gate, electrons accumulate at the bottom interface of the a-IGZO and form the main channel [22]. Due to the dual-gate coupling effect, the top gate can flexibly control the energy band and current density distribution of the channel, as shown in Fig. 2(b). The output and transfer curves for DG-synchronized-sweep are shown in Figs. 2(c, d). An excellent agreement between the model and experimental data has been demonstrated. Due to the dual-gate coupling effect, the carrier scattering induced by the interface defects can be mitigated, resulting in a weakened interfacial effect and better *SS* performance.

In order to explore the L-dependent device characteristics at nanometer size, the model reproduces the IV characteristics of IDG-FETs at different L (e.g., Fig. 3(a)). As shown in Fig. 3(c), as L decreases (300 nm∼50 nm), the *SS* decays to 92.49 mV/Dec, the mobility decreases by 70%,

$$FF(\varphi_{S1}) = k_1q_1(k_1q_1 + k_2q_2) - A_0 exp\left(\frac{V_{G1} - \varphi_{S1}}{\Phi_T}\right) - B_0 exp\left(\frac{V_{G1} - \varphi_{S1}}{\Phi_{TA}}\right) \tag{7}$$

$$\varphi_{sn} = \frac{k_1V_{G1} + k_2V_{G2}}{k_1 + k_2} - \Phi_T \cdot Lam\left(\frac{B_0\Phi_{TA}t}{k_1V_{G1}(k_1 + k_2)} exp\left(\frac{k_1(V - V_{Gf}) + k_2(V - V_{Gb})}{\Phi_T(k_1 + k_2)}\right)\right) \tag{8}$$

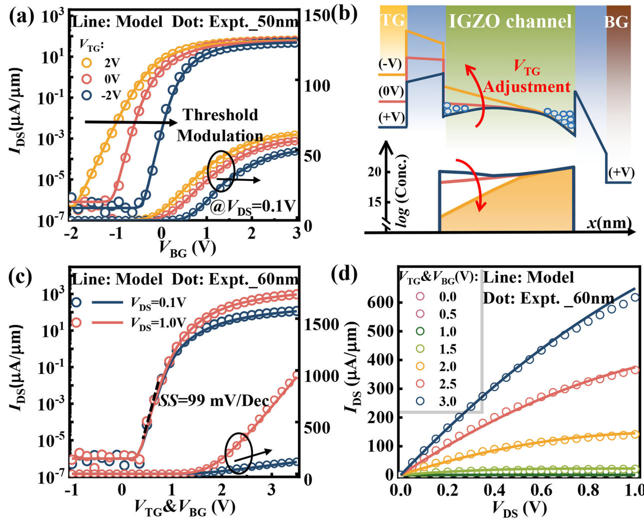

FIGURE 2. (a) Comparison of model and experimental transfer curves and trans-conductance at different V_{TG}. (b) Energy band diagrams and carrier concentration distributions under different top-voltage conditions. Agreement between our model and experimental data of the (c) transfer curves, (d) output curves under the DG&BG synchronized sweep.

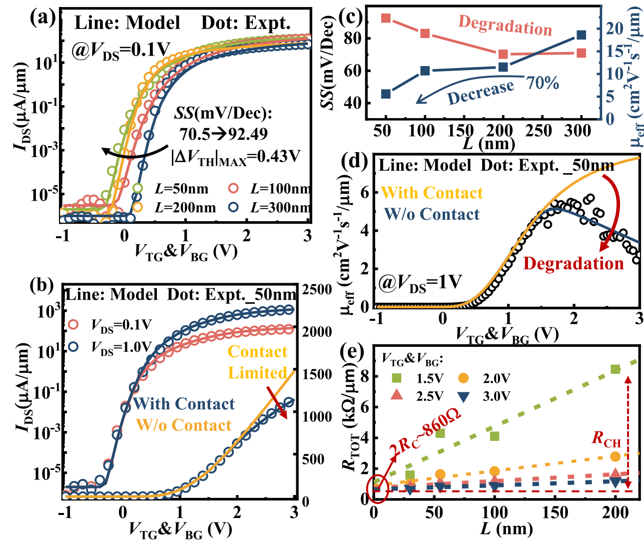

FIGURE 3. (a)Agreement between model and measured results for transfer curves for L from 300 to 50nm. (b) Comparison of model (w/o contact effects) and experimental transfer curves in linear scale at L =50 nm. (c) SS increases and u_{eff} decreases with L. (d) Mobility with and w/o contact effects. (e) Total device resistance vs. L measured by transfer-line method under different V_G conditions.

and the V_{TH} is significantly shifted. The DIBL effect is also not significant for the DG-FET as L decreases to 50 nm compared to the single-gate device [23], as shown in Fig. 3(b). An extreme point of the channel potential may shift and indicate short channel effects at small L and large V_{DS}. The SS performance of the short-channel device is defined as $\Phi_T(\ln 10)(1/\delta+C_D/C_{OX})$, where δ is related to the minimum value of the channel potential [12]. The SS degradation leads to an increase in the leakage current, which in turn affects the DRAM retention. There are non-ideal

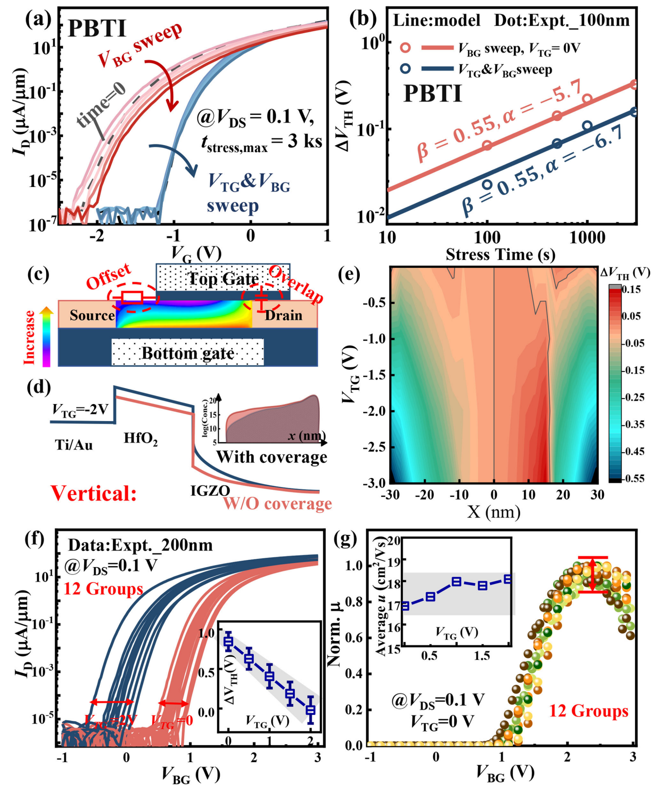

FIGURE 4. I V curves of BG single-sweep and TG&BG synchronized-sweep of BG stress measured under (a) PBTI for L_{CH}=100nm IDG-FET. Degradation of ΔV_{TH} at (b) PBTI was investigated using various sweeping methods ΔV_{TH} was subjected to fitting using a semi-classical model. (c) Schematic of top gate misalignment and the potential distribution diagram. (d) Band diagrams and carrier conc. corresponding to the surface un- covered and covered by the top gate. (e) TCAD simulated ΔV_{TH} matrix for different V_{TG} and misalignment distances, with 30 nm-channel length and 5 nm-thickness. (f) Distribution characteristics of 12 groups of devices under different V_{TH} and insert the variations of V_{TH}. (g) Normalized mobility properties extracted from I-V curves and average μ is inserted.

ohmic contacts in short-channel devices, the effect of contact resistance increases as the channel length decreases, and the channel resistance (R_{CH}) divider decreases, resulting in lower mobility and lower current. Furthermore, a comparison of different mobility models (classical and contact-limited) and experimental data is depicted in Fig. 3(d), where the contact resistance leads to a significant decrease in mobility and current when L=50 nm. Based on the TLM, the total resistance (R_{TOT}) was calculated for different L corresponding to different V_{GS} and the $2R_C$ was extracted from the intercept of the linear fit to the R_{TOT} as shown in Fig. 3(e) with $2R_C = 860\Omega \cdot \mu$m.

B. RELIABILITY ASSESSMENT

The continuous scaling improves metrics of efficiency, density, and area in circuits and architectures. However, continued miniaturization leads to increasingly serious BTI effects and non-uniformity of the manufacturing process.

Since a-IGZO FETs are inherently n-channel devices, the reliability of positive bias temperature instability (PBTI)

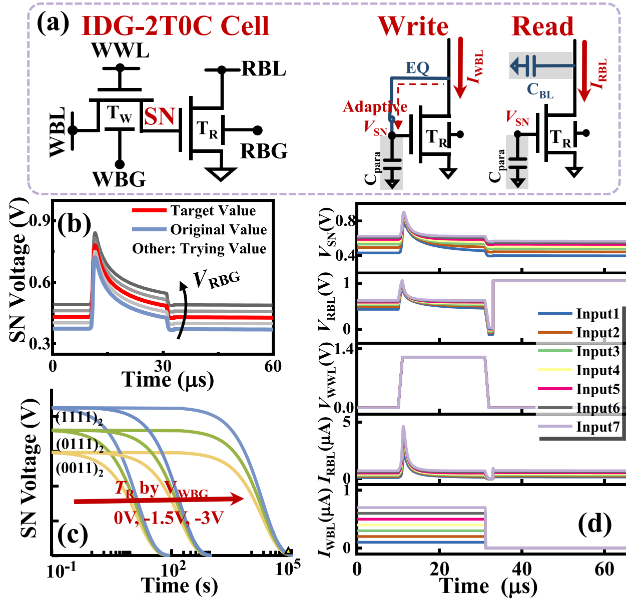

FIGURE 5. (a) Description of write operation and read mode in a 2T0C cell. (b) V_{SN} compensation values corresponding to different V_{RBG}. (c) Simulated V_{SN} development over time for different storage states and different V_{WBG}, where $(1111)_2$, $(0111)_2$ and $(0011)_2$ are different binary-based input values. (d) 2T0C cell multi-bit operation waveforms, and Input1 to Input7 correspond to I_{WBL} input values of 0.1 μA to 0.7 μA in steps of 0.1 μA, respectively. WWL: write word line, WBL: write bit line, WBG: write back gate, RBL: read bit line, RBG: read back gate.

is very important. Here, Fig. 4(a) shows the PBTI with measured IV curves (V_{DS}=100 mV) for BG-sweep and DG-synchronized-sweep. PBTI leads to a positive V_{TH} shift, and during synchronized-sweep, the BTI effect is mitigated due to the dual-gate coupling effect, which leads to the bulk accumulation of carriers away from the interface [24], thus exhibiting more reliable threshold characteristics. PBTI in IGZO is mainly due to charge trapping or relaxation kinetics, which have different time kinetics, voltage acceleration factors and activation energies. As reported in [7], [25], a physics-based model is employed to reproduce stress and relaxation traces recorded under various test conditions. Here, we simplify the complex physics-based model to a unified empirical BTI degradation model that can be expressed as

$$\Delta V_{TH} = A_E t^{\beta} V_{ov}^{\alpha} e^{-\frac{E_a}{\Phi_T}} \tag{15}$$

where, ΔV_{TH} is the threshold voltage offset due to BTI, t is the stress time, Vov is the stress voltage, E_a is the activation energy, A_E, α and β are degradation fitting parameters. The degradation fitting parameters are extracted by fitting the ΔV_{TH} measured from the experiment, as shown in Fig. 4(b). Then, the above ΔV_{TH} is embedded into the compact model via the effective gate voltage V_{GEFF}=V_{GS}-ΔV_{TH}, further capturing DRAM cell retention degradation induced by stressing.

The source/drain asymmetry effect due to top gate misalignment in an advanced process node is investigated using TCAD simulation. For poorly aligned IDG-FET, the offset area induces additional series resistance and weakens controllability for the channel potential, and the increased overlapping area aggravates the effects of overlap capacitance and gate leakage, as shown in Fig. 4(c), which results in degradation of the data integrity of the 2T0C DRAM cell. The threshold adjustment feature based on IDG-FETs compensates the data integrity by adjusting the V_{TH} to alleviate leakage current through the top-gate voltage. It facilitates accurate and tolerant multi-bit programming. When applied a negative top-gate voltage, conduction band decreases at surface, which is not covered by top-gate. Correspondingly, carrier concentration will increase, as shown in Fig. 4(d). Moreover, Fig. 4(e) exhibits a relationship between top gate offset distance and ΔV_{TH} at different V_{TG}.

We further investigated the device-to-device variations of the nanoscale IDG-FETs, Fig. 4(f) shows the variation of measured IV curves for 12 groups of devices using the same process steps. The average V_{TH} decreases as V_{TG} increases, accompanied by an increase in V_{TH} variation. Additionally, the intrinsic parameters of the transistor are extracted from transfer characteristics, demonstrating mobility fluctuations among different devices, as shown in Fig. 4(g). These fluctuations primarily originate from variations in material composition and fabrication process of a-IGZO, which lead to changes in density of states, thereby affecting the extended-state potential barrier and localized-state characteristic temperature. It will result in fluctuations of retention time among cells, challenging multi-bit computing.

C. NOVEL 2T0C CELL SIMULATION

This model is written in Verilog-A and compiled to commercial circuit design simulator as new active components. For the design of a high-density storage DRAM architecture, a multi-bit storage current read/write operation scheme based on IDG-2T0C was verified [26], and the novel capacitorless circuit unit is shown in Fig. 5(a). This is mainly gate voltage modulation that alters the DG coupling effect to change the channel potential and carrier concentration, which in turn stabilizes the threshold voltage of the read/write transistor in the read, write and hold cases of the 2T0C cell. During write operation, the write bit line (WBL) is shorted to read bit line (RBL), the write transistor (T_W) and the read transistor (T_R) forms a diode connection to charge the storage node (SN) through WBL, the V_{SN} can be adaptively changed to compensate for the V_{TH} variations of T_W. During read operation, different current values are obtained at RBL depending on the V_{SN} nodes, as shown in Fig. 5(a). Based on the T_R threshold regulation capability, the V_{RBG} is adjusted so that the V_{SN} rises to a high level after the write word line (WWL) is turned on and stabilizes at the target value after the WWL is turned off, as shown

in Fig. 5(b). This method effectively mitigates the current degradation as well as compensates for the degradation of the V_{SN} due to the coupling effect of the WWL turned-off device. For the T_W, adjusting V_{WBG} increases the V_{TH} value, thereby reducing its leakage current and improving data retention, as shown in Fig. 5(c). Flexible operation based on the IDG-2T0C can be used to balance device fluctuations due to short-channel effects. Fig. 5(d) demonstrates the timing diagram for the multi-bit operation of the 2T0C memory cell, where I_{WBL} is the write current, I_{RBL} is the read current.

IV. CONCLUSION

In summary, a surface potential-based compact physical model of ultra-scaled independent dual gate a-IGZO-FET was successfully developed, which can be applied to three modes of operation: single gate sweep, dual gate synchronized sweep, and independent gate modulation. This model considers gate coupling and finite-size disordered transport from device physics, and characterizes the short channel effect and contact resistance. The reliability issues due to variations in material composition and manufacturing processes have been addressed. It serves as a novel methodology for evaluating device-to-circuit reliability, thus accelerating the design-technology co-optimization flow in ultra-large-scale integrated circuits using BEOL-transistors.

REFERENCES

[1] Z. Zheng et al., "First demonstration of work function-engineered BEOL-compatible IGZO non-volatile MFMIS AFeFETs and their co-integration with volatile-AFeFETs," in *Proc. IEEE Symp. VLSI Technol. Circuits*, Kyoto, Japan, 2023, pp. 1–2, doi: 10.23919/VLSITechnologyandCir57934.2023.10185355.

[2] I. I. Fishchuk et al., "Random band-edge model description of thermoelectricity in high-mobility disordered semiconductors: Application to the amorphous oxide In-Ga-Zn-O," *Phys. Rev. B, Condens. Matter*, vol. 105, no. 24, Jun. 2022, Art. no. 245201, doi: 10.1103/PhysRevB.105.245201.

[3] A. V. Nenashev, J. O. Oelerich, S. H. M. Greiner, A. V. Dvurechenskii, F. Gebhard, and S. D. Baranovskii, "Percolation description of charge transport in amorphous oxide semiconductors," *Phys. Rev. B, Condens. Matter*, vol. 100, no. 12, Sep. 2019, Art. no. 125202, doi: 10.1103/PhysRevB.100.125202.

[4] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, Nov. 2004, doi: 10.1038/nature03090.

[5] A. Spessot and H. Oh, "1T-1C dynamic random access memory status, challenges, and prospects," *IEEE Trans. Electron Devices*, vol. 67, no. 4, pp. 1382–1393, Apr. 2020, doi: 10.1109/TED.2020.2963911.

[6] A. Belmonte et al., "Capacitor-less, long-retention (>400s) DRAM cell paving the way towards low-power and high-density monolithic 3D DRAM," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2020, pp. 28.2.1–28.2.4, doi: 10.1109/IEDM13553.2020.9371900.

[7] A. Chasin et al., "Understanding and modelling the PBTI reliability of thin-film IGZO transistors," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2021, pp. 31.1.1–31.1.4, doi: 10.1109/IEDM19574.2021.9720666.

[8] H.-Y. Chang et al., "Channel migration of dual channel a-InGaZnO TFTs under negative bias illumination stress," *Appl. Phys. Lett.*, vol. 122, no. 12, Mar. 2023, Art. no. 123504, doi: 10.1063/5.0135302.

[9] Z. Luo et al., "5.1 Å EOT and low leakage TiN/Al2O3/Hf0.5Zr0.5O2/Al2O3/TiN heterostructure for DRAM capacitor," *Appl. Phys. Lett.*, vol. 122, no. 19, May 2023, Art. no. 192903, doi: 10.1063/5.0145824.

[10] R. Islam, P. Li, M. Beg, M. Sachdev, and G.-X. Miao, "Helimagnet-based nonvolatile multi-bit memory units," *Appl. Phys. Lett.*, vol. 122, no. 15, Apr. 2023, Art. no. 152407, doi: 10.1063/5.0147066.

[11] K. Chen et al., "Scaling dual-gate ultra-thin a-IGZO FET to 30 nm channel length with record-high Gm,max of 559 μS/μm at VDS=1 V, record-low DIBL of 10 mV/V and nearly Ideal SS of 63 mV/dec," in *Proc. IEEE Symp. VLSI Technol. Circuits*, 2022, pp. 298–299, doi: 10.1109/VLSITechnologyandCir46769.2022.9830389.

[12] J. Guo et al., "A new surface potential and physics based compact model for a-IGZO TFTs at multinanoscale for high retention and low-power DRAM application," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2021, pp. 8.5.1–8.5.4, doi: 10.1109/IEDM19574.2021.9720700.

[13] M. Caselli, D. Bhattacharjee, A. Mallik, P. Debacker, and D. Verkest, "Tiny ci-SAR A/D converter for deep neural networks in analog in-memory computation," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Austin, TX, USA, 2022, pp. 1823–1827, doi: 10.1109/ISCAS48785.2022.9937613.

[14] A. S. Rodin and M. M. Fogler, "Hopping transport in systems of finite thickness or length," *Phys. Rev. B, Condens. Matter*, vol. 84, no. 12, Sep. 2011, Art. no. 125447, doi: 10.1103/PhysRevB.84.125447.

[15] S. Lee et al., "Temperature dependent electron transport in amorphous oxide semiconductor thin film transistors," in *Proc. Int. Electron Devices Meeting*, Washington, DC, USA, 2011, pp. 14.6.1–14.6.4, doi: 10.1109/IEDM.2011.6131554.

[16] L. Xu et al., "A surface potential based compact model for ferroelectric a-InGaZnO-TFTs toward temperature dependent device characterization," *IEEE Electron Device Lett.*, vol. 44, no. 3, pp. 412–415, Mar. 2023, doi: 10.1109/LED.2022.3233824.

[17] J. Guo et al., "A new surface potential based compact model for independent dual gate a-IGZO TFT: Experimental verification and circuit demonstration," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2020, pp. 22.6.1–22.6.4, doi: 10.1109/IEDM13553.2020.9371951.

[18] Z. Bai et al., "High mobility achieved in InGaZnO TFT with vacuum-gap as insulating layer," *Appl. Phys. Lett.*, vol. 121, no. 26, Dec. 2022, Art. no. 263502, doi: 10.1063/5.0127613.

[19] E. N. Cho, J. H. Kang, and I. Yun, "Contact resistance dependent scaling-down behavior of amorphous InGaZnO thin-film transistors," *Curr. Appl. Phys.*, vol. 11, no. 4, pp. 1015–1019, Jul. 2011, doi: 10.1016/j.cap.2011.01.017.

[20] S. Lee et al., "Modeling and characterization of metal-semiconductor-metal-based source-drain contacts in amorphous InGaZnO thin film transistors," *Appl. Phys. Lett.*, vol. 96, no. 11, Mar. 2010, Art. no. 113506, doi: 10.1063/1.3364134.

[21] P. Dutta, B. Syamal, N. Mohankumar, and C. K. Sarkar, "A surface potential based drain current model for asymmetric double gate MOSFETs," *Solid-State Electron.*, vol. 56, no. 1, pp. 148–154, Feb. 2011, doi: 10.1016/j.sse.2010.10.025.

[22] M. Mativenga, S. An, and J. Jang, "Bulk accumulation a-IGZO TFT for high current and turn-on voltage uniformity," *IEEE Electron Device Lett.*, vol. 34, no. 12, pp. 1533–1535, Dec. 2013, doi: 10.1109/LED.2013.2284599.

[23] Z.-H. Liu et al., "Threshold voltage model for deep-submicrometer MOSFET's," *IEEE Trans. Electron Devices*, vol. 40, no. 1, pp. 86–95, Jan. 1993.

[24] S. Hong, S. Lee, M. Mativenga, and J. Jang, "Reduction of negative bias and light instability of a-IGZO TFTs by dual-gate driving," *IEEE Electron Device Lett.*, vol. 35, no. 1, pp. 93–95, Jan. 2014, doi: 10.1109/LED.2013.2290740.

[25] J. Guo et al., "Compact modeling of IGZO-based CAA-FETs with time-zero-instability and BTI impact on device and capacitor-less DRAM retention reliability," in *Proc. IEEE Symp. VLSI Technol. Circuits*, Honolulu, HI, USA, 2022, pp. 300–301, doi: 10.1109/VLSITechnologyandCir46769.2022.9830482.

[26] X. Duan et al., "Novel vertical channel-all-around (CAA) In-Ga-Zn-O FET for 2T0C-DRAM with high density beyond $4F^2$ by monolithic stacking," *IEEE Trans. Electron Devices*, vol. 69, no. 4, pp. 2196–2202, Apr. 2022, doi: 10.1109/TED.2022.3154693.