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A Comparative Study on the Effects of Planarity of Access Region on the Low-Frequency Noise Performance of InAlN/GaN HFETs

YATEXU PATEL AND POUYA VALIZADEH (Senior Member, IEEE)

Department of Electrical and Computer Engineering, Concordia University, Montreal, QC H3G 1M8, Canada

CORRESPONDING AUTHOR: P. VALIZADEH (e-mail: p.valizadeh@ieee.org)

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ABSTRACT The low frequency drain noise-current characteristics of metallic-face InAlN/AlN/GaN heterostructure field effect transistors (HFETs) having fin structures only under the gate, while maintaining a planar structure in the access regions, are compared to those of the HFETs having fin structures stretched from source to drain. Evidence indicates that both device types follow the trends of carrier number fluctuation (CNF) with correlated mobility fluctuation (CMF) model of 1/f noise. Accordingly, the noise of the gated channel has been identified as the dominant noise source for both device types. Devices from the former category exhibit improved 1/f noise performance with lower drain noise-current spectral density. This observation could be due to presence of a higher two-dimensional electron gas (2DEG) concentration under the gated-channel overshadowing the carrier number and mobility fluctuations.

INDEX TERMS InAlN/GaN, heterostructure field effect transistor (HFET), lattice-matched, low frequency noise (LFN).

I. INTRODUCTION

GaN has excellent electronic properties such as wide bandgap (E_g=3.4 eV) [1], high two-dimensional electron gas (2DEG) room temperature low-field mobility (1500 $cm^2/V{\cdot}s$) [1], high electron saturation velocity (V_{sat} = 2.5 × 10^7 cm/s) [2], and high critical electric field ($E_{critical}$ > 3 MV/cm) [3]. As a result of these properties, GaN-channel heterostructure field-effect transistors (HFETs) have been deemed suitable for high power (> 100 W), high voltage (≥ 600 V), high temperature (> 300 °C) [4], and high frequency (f_T/f_{MAX} of 454/444 GHz) [5] operation. Realization of these HFETs on narrow fins, instead of large mesas, has been proven to be of interest in not only improving the chance of realizing a positive threshold-voltage (V_T) [6], but at the same time offering a superior breakdown voltage [7].

The novel lattice-matched HFETs realized on an epilayer consisting of a thin $In_{0.17}Al_{0.83}N$ barrier layer grown on top of an undoped GaN channel have been demonstrated over the past decade to enjoy improved stable high-frequency power characteristics compared to their famous AlGaN/GaN counterparts [8]. This is specially thanks to employing a lattice-matched barrier enjoying substantial spontaneous polarization-induced sheet charge density. Since a good gate-transconductance (G_m) linearity, specially at high gate over-drives, is essential to linear high-frequency amplifiers intended for use in modern telecommunication system (such as 5G networks), enhancing the linearity of the deeply scaled HFETs implemented on such epilayers is very much in demand.

Whereas, resistance of the gate-source access region serving as a negative feedback loop is expected to have a positive impact on the device linearity in common source measurement configuration, if not of a constant value its dynamic variation affects the overall linearity of the device negatively [9]. In the HFETs having fin-shaped structures in the drain and source access regions, dynamically increasing source-access resistance at higher drain currents (I_D) decreases the effective voltage difference between the gate and the gated channel [10]. The result of which is the

loss in the drain current density and gate-transconductance. Lee et al. reported a fin-like nanowire channel InAlN/GaN HFET with an improved G_m linearity by partially etching InAlN barrier and GaN channel layer into fins only under the gate electrode [11]. By forming fin structures just under the gate, while retaining a planar structure in the access regions, the dynamic increase of the source access resistance can be maintained well below that of the gated channel. This has been reported to facilitate improved device linearity, higher drain current density, and gate transconductance.

An extensive body of research implies a significant correlation to exist between electronic device technology, the level of 1/f noise, and the manifestation of generation–recombination (G-R) bulge signatures [12], [13], [14], [15]. In addition to suitability of 1/f noise in reliability and material studies, for the special case of HFETs, despite their exceptional high frequency noise performance, in many nonlinear applications such as mixers and oscillators, low frequency noise acts as a limiting factor [16]. A decrease in LFN has a significant impact on oscillator phase noise and the performance of intermediate frequency (IF) amplifiers and mixers [17].

In light of the importance of these characteristics, in this study, we present a thorough analysis of the LFN characteristics of lattice-matched InAlN/GaN HFETs having fin structures only under the gate (Type-I) and those having fin structures stretched from source to drain (Type-II). Figure 1 illustrates the schematics of these two device types.

Device fabrication details and specifications are briefly presented in Section II. Section III provides details on the measurement setup. Section IV provides the analysis on the experimental results. The conclusion is provided in section V.

II. DEVICE FABRICATION AND SPECIFICATION

The devices studied in this manuscript were fabricated on a Ga-face Wurtzite $In_{0.17}Al_{0.83}N$/AlN/GaN heterostructure composed of 9 nm unintentionally doped (UID) barrier, a 1 nm thick spacer layer, a 1700 nm thick GaN channel, and a 1.45 μm Fe-doped GaN buffer layer grown on a 4-in 4-H-SiC substrate.

The device fabrication process started with spin coating of the sample with ma-N 2403 negative resist to define the isolation features using electron beam lithography (EBL) of beam energy 20 keV. Mesa isolation to 100-nm depth was performed post developing the sample in ma-D 525, employing magnetically enhanced reactive ion etching (MERIE) using Cl_2/Ar plasma. Then, followed the second EBL conducted with the same beam energy as step one, after the sample was coated with MMA(8.5)MAA-EL11/PMMA-A4 co-polymer positive resist for the registration of the Ohmic contacts. After developing the co-polymer photoresist in MIBK/IPA 1/3 solution for 1 min, the sample underwent immersion in HCl solution to eradicate the native oxide layer. Subsequently, Ohmic metallization was carried out using NEXDEP e-beam evaporation, followed by lift-off in

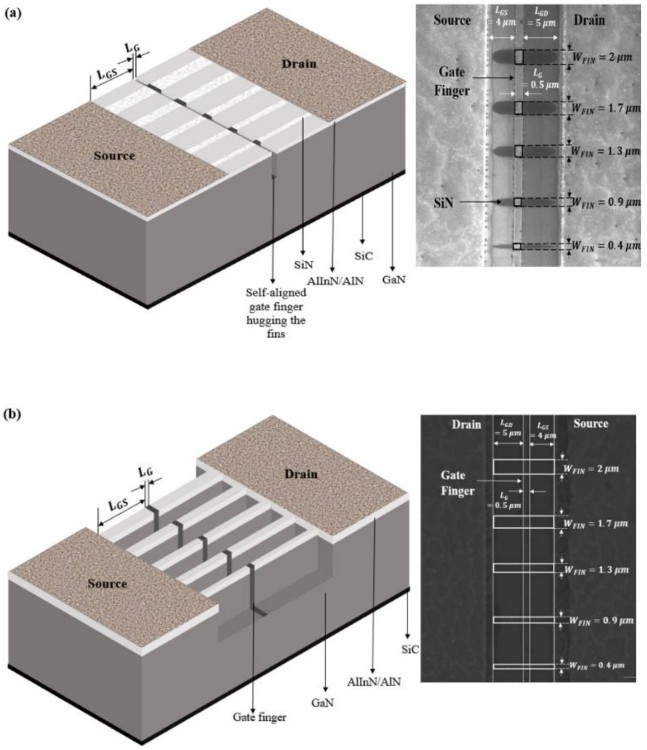

FIGURE 1. 3D schematic illustration of the (a) Type-I and (b) Type-II HFET. Inset: Top view SEM images of the fabricated devices.

acetone using ultrasonication. After depositing Ti/Al/Ni/Au (20/120/40/50 nm) ohmic metal stack, the sample underwent rapid thermal annealing (RTA) at 765 °C for 60 s in nitrogen ambient to form the alloyed Ohmic contact to the 2DEG. The fabricated Ohmic contacts exhibit high quality, as evidenced by the consistently low values of contact resistance (R_c) and sheet resistance (R_{sh}) obtained through transfer length measurement (TLM), which are approximately 0.67 Ω·mm and 243 Ω/□, respectively. The third EBL step was performed for the realization of the gate contacts for Type-II devices. For Type-I devices, after the realization of the ohmic contacts, a 120 nm thick SiN was deposited by plasma-enhanced chemical vapor deposition and fin structures were formed in SiN through the EBL with ma-N 2403 negative resist and subsequent dry etching of SiN in CF_4/O_2 plasma. By using MMA(8.5)MAA-EL11/PMMA-A4 co-polymer positive resist as a mask following the pattern of the gate finger, the dry etching of the top InAlN barrier and AlN spacer layers, as well as about 90 nanometers of the GaN channel layer was done in Cl_2/Ar plasma using the MERIE. During the etching process SiN served as the hard mask and protected fin areas. Succeeding this step, SiN was dry etched to expose channel area whereas the protected SiN by the co-polymer positive resist in the access regions serves the purpose of surface passivation. This way fin-like structures were formed in the gate opening region without conducting an additional EBL step and as a result of this, the fins have the same length as the gate electrode. DisCharge H_2OX_2 anti-charging agent was employed to

eliminate electron beam divergence from its designated path caused by the accumulation of electrons at the surface of the sample due to the existence of the insulating SiC substrate. Finally, Schottky gate-stack of Ni/Au (20/20 nm) was evaporated followed by the standard lift-off process in acetone using ultrasonic bath.

Evidently, the remaining SiN in the access regions only provides surface passivation to the parts of the access region aligned with the gated fins of the Type-I devices. Such a manner of implementation allows a simpler way of implementing the needed small fins. Following the deposition of contact pads, Keithley 4200-SCS semiconductor characterization system was used for room-temperature on-chip characterization of the fabricated HFETs.

Both device types are consisting of five fin structures of 400, 900, 1300, 1700, and 2000 nm width along the gate width direction. The broad range of threshold voltage (V_T) from –4 V for 2 μm wide fin to –1 V for 0.4 μm wide fin gives privilege to realize a linear multichannel device, comprised of sets of individual channels each possessing a specific V_T. These sets of individual channels turn on sequentially and the sum of the transconductances attributed to the parallel channels can effectively reduce the drop in the G_m at high gate-source over-drives (V_{GS}), essentially yielding a broader G_m-V_{GS} characteristics [18]. This way the choice of the fin structures was made with improvement of linearity in mind. According to the given dimensions, the fabricated devices have overall gate width of 6.3 μm with unless reported otherwise gate length (L_G) of 0.5 μm, gate-source spacing (L_{GS}) of 4 μm, and gate-drain spacing (L_{GD}) of 5 μm.

Tested among a large number of devices, consistently the threshold voltage of the Type-I HFETs is around –4 V, while that of Type-II is about –3.7 V. Since the two device types have been realized on pieces cut from different positions on the surface of the wafer, the relatively minor difference between the threshold voltage values defined ideally by the fin of the largest width is deemed acceptable. Nonetheless, for the sake of accuracy, effective gate-source voltage ($V_{GS,Eff}$) defined as the difference between the applied extrinsic gate-source voltage and the threshold-voltage of each device has been employed in our analysis.

Maximum drain-current density of the Type-I HFETs at $V_{GS,Eff} = 4$ V is about 1307 mA/mm and this value is about 1185 mA/mm for the Type-II HFETs, whereas the peak transconductance values of Type-I and Type-II HFET at drain-source voltage (V_{DS}) of 4 V are about 318 mS/mm and 240 mS/mm, respectively. The figure of merit of gate voltage swing (GVS) can be used to quantitively assess the linearity performance of various types of devices. GVS is defined as the gate voltage range across which the value of the transconductance remains at least 80% of its peak value. The GVS of the Type-I HFETs at the said V_{DS} is 4.5 V, while this metric equals 2.8 V for Type-II devices. As anticipated [11], it is very evident that by keeping the width of the access-region greater than the width of the gated channel, channel-charge density can rise closer to an ideal linear characteristic with an extrinsic gate bias (i.e., through maintaining the source-access region resistance well below that of the gated channel resistance).

III. EXPERIMENTAL SETUP

On-wafer LFN characterization was conducted utilizing a measurement setup developed in-house [19]. Noise measurements at room temperature were conducted in the linear and early saturation regime to prevent any uncertainties caused by factors arising in the saturation mode of device operation, such as pinch off, carrier velocity saturation, and self-heating which might make the noise analysis gratuitously complex and unreliable [19].

At least four devices of each type were selected for characterization on each die. A total of two dies were utilized for this evaluation. The DC characteristics of the devices of each type at room temperature were identical (with a variation of less than two percent). The noise data presented reflects the observed trends among these devices.

IV. EXPERIMENTAL RESULTS AND ANALYSIS

Fig. 2 shows the comparison of drain noise-current spectral density for the devices studied in this manuscript biased in the early linear regime ($V_{DS} = 0.25$, 0.5, and 0.75 V). As shown here, in the frequency range of 1 Hz to 10 KHz a $1/f^{\gamma}$ characteristics, with a frequency exponent (i.e., γ) varying within the range of 0.98–1.11, is observed on the drain noise-current of both device types. Type-II devices consistently show higher levels of drain noise-current density than Type-I devices at the same effective gate-source voltage and applied drain voltage.

Low frequency noise is a complicated issue and still theories are being developed to describe the origin of it in electronic devices. The most acknowledged 1/f noise theories named “carrier-number fluctuation” [20], “mobility fluctuation” [21], and a certain variation of these two old theories referred to as “carrier-number fluctuations with correlated mobility fluctuation” [22] proposed by McWhorter, Hooge, and Ghibaudo, respectively, strive to explain the origin of 1/f noise. Carrier-number fluctuation theory is based on the fluctuation of the number of charge carriers in the channel, trap sites and along the interface. Accordingly, in presence of a sufficient range of energy levels associated with these traps, the integral effect of the Lorentzian spectral densities defined by the generation-recombination of the carriers through these traps, offers a 1/f spectrum.

Where sufficient range of traps are deemed absent, representation of the mobility fluctuation noise theory is provided in terms of an empirical relationship, in which the normalized drain-noise power is evaluated according to [21],

$$\frac{S_{I_D}}{{I_D}^2} = \frac{\alpha_H}{f \cdot N} \tag{1}$$

where N is the total number of carriers in the transport channel and α_H is the dimensionless constant referred as Hooge’s

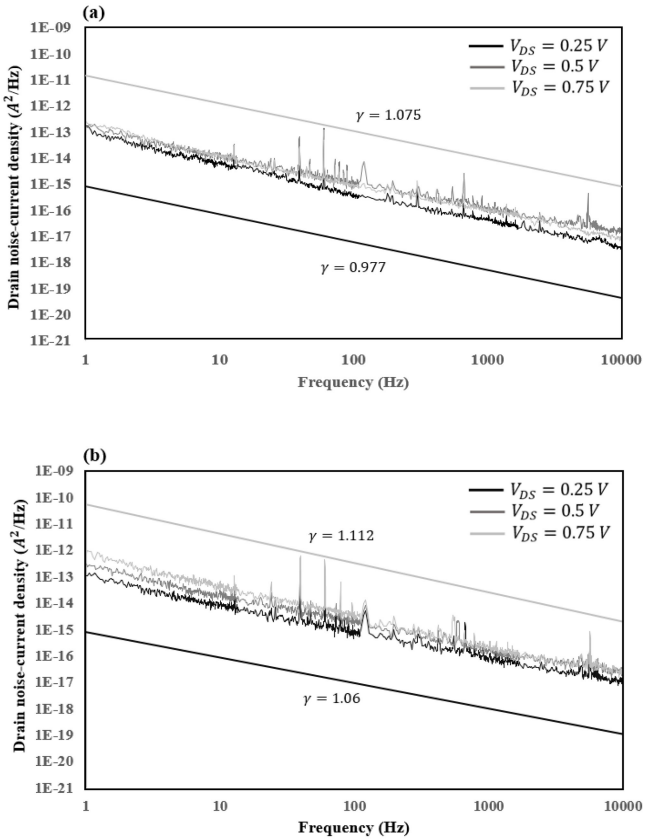

FIGURE 2. A comparison of room temperature drain noise-current spectral density as a function of frequency of (a) Type-I and (b) Type-II devices at $V_{GS,Eff} = 3$ V and $V_{DS} = 0.25$, 0.5, and 0.75 V.

parameter. The theoretical idea behind the aforementioned relationship is to assert that, when the electrons produce 1/f noise, regardless of the physical mechanism the electrons are involved in, they do it autonomously. It has been observed α_H varies with crystalline quality of the semiconductor and factors affecting the electron mobility [16]. The latter has mainly been related to the mobility fluctuation of the charge carriers due to the fluctuations in their scattering rate [23]. The "carrier number fluctuation with correlated mobility fluctuation" theory considers both the fluctuation of the number of carriers as a result of their trapping/de-trapping and the correlated mobility fluctuation of the charge carriers.

Considering the latter two theories, we leave the description of the method conducted to speculate on the applicability of these noise theories to a more appropriate place toward the latter part of this section.

In this study, in order to determine the dominant noise source, the models proposed by Peransin et al. [24] and Kammeugne et al. [25] have been explored. For a long time Hooge's empirical formulation has been used based on which Peransin et al. [24] by studying the gate-bias dependence of the normalized drain noise-current formulated a strategy to find out where in the channel the noise is dominant. The latter model disagreeing with this strategy suggests that in order to discriminate between the LFN from the access

TABLE 1. Summary of the criteria developed in [24] for the determination of the dominant noise and resistance along the channel.

		Dominant Noise Source	Dominant Resistance
$\frac{S_I}{I^2}\alpha$	$(V_{GS}-V_T)^{-3}$	S_{Ch}	R_{Access}
	$(V_{GS}-V_T)^{-1}$	S_{Ch}	R_{Ch}
	$(V_{GS}-V_T)^{0}$	S_{Access}	R_{Access}
	$(V_{GS}-V_T)^{2}$	S_{Access}	R_{Ch}

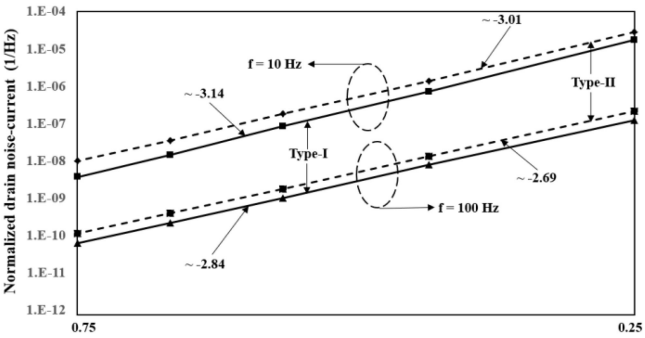

FIGURE 3. Variation of the normalized drain noise-current level at 10 and 100 Hz vs. effective gate-source voltage at room temperature, for $V_{GS,Eff} = 1$, 1.5, 2, 2.5, and 3 V and $V_{DS} = 0.25$ V. The presented number on each linear section indicate the slope of the characteristics.

regions and the gated-channel, the impact of access resistance on the recorded LFN must be studied by varying the gate length [25].

A. CARRIER MOBILITY FLUCTUATION-BASED MODEL FOR THE DETERMINATION OF THE DOMINANT NOISE SOURCE

As summarized in Table 1, variation of the normalized 1/f noise level with the normalized effective gate-source voltage (defined as $(V_{GS}-V_T)/|V_T|$), has been suggested to have the possibility of identifying the dominant noise source and resistance along the channel [24]. In this framework, S_{Access} represents the noise spectral density of the access-resistance, while S_{Ch} represents the noise spectral density of the gated-channel. Furthermore, R_{Access} denotes the resistance of the access-channel, and R_{Ch} denotes the resistance of the gated-channel.

At room temperature, the normalized drain noise-current vs the normalized effective gate-source voltage of both types of devices is demonstrating the existence of an exponential dependence with an exponent of about -3 (as shown in Figure 3). This observation suggests that, at room temperature, and in the studied range of bias, for both types of devices if the carrier mobility fluctuation theory prevails [24], the dominant resistance is the access-resistance and the dominant noise source is that of the gated channel.

B. CARRIER NUMBER FLUCTUATION WITH CORRELATED MOBILITY FLUCTUATION-BASED MODEL FOR THE DETERMINATION OF THE DOMINANT NOISE SOURCE

The gate length has been varied for Type-I and Type-II devices, while maintaining the L_{GS} and L_{GD} the same, to see

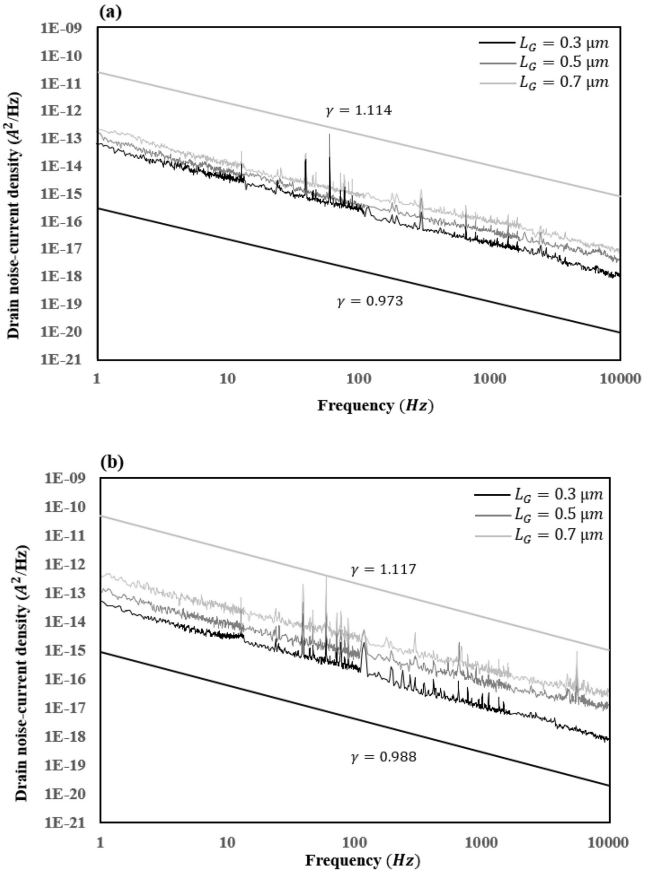

FIGURE 4. Comparison of room temperature drain noise-current spectral density as a function of frequency of (a) Type-I and (b) Type-II devices having L_G of 300, 500, and 700 nm at $V_{GS,Eff}$ = 3 V and V_{DS} = 0.25.

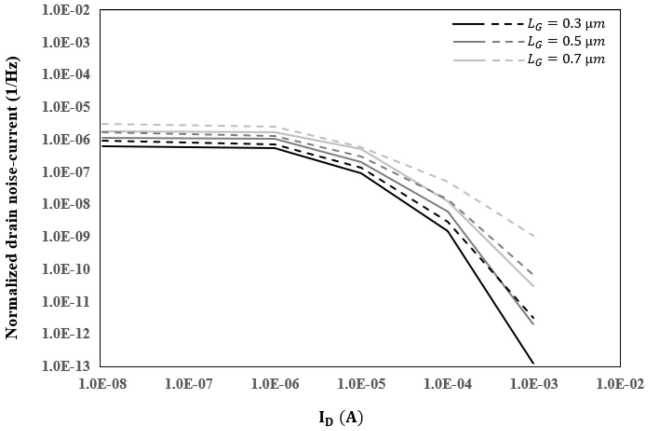

FIGURE 5. Normalized drain noise-current spectral density as a function of I_D of Type-I (solid line) and Type-II (dashed line) HFETs at V_{DS} = 0.25 and f = 10 Hz.

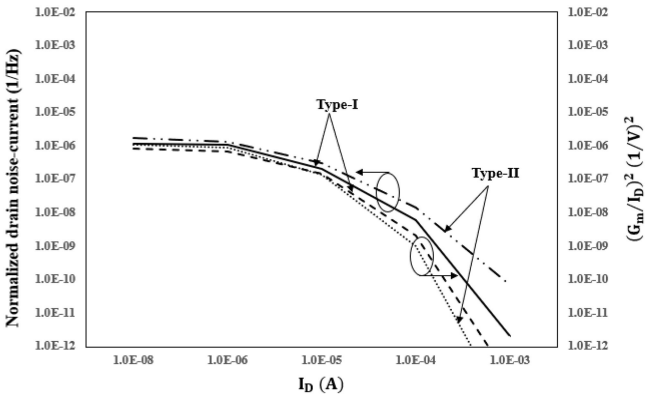

FIGURE 6. Comparison of normalized drain noise-current spectral density and $(G_m/I_D)^2$ versus I_D at V_{DS} = 0.25 and f = 10 Hz.

the impact of access resistance on LFN analysis. As alluded in [25], this is supposed to be more evident for devices having shorter L_G. Among these devices, Fig. 4 presents the drain noise-current density as a function of frequency while Fig. 5 illustrates the variation of the normalized drain noise-current as a function of drain current for the Type-I and Type-II devices having L_G = 300, 500, and 700 nm and in the early linear regime of operation (V_{DS} = 0.25). The impact of series resistance on LFN can simply be obtained by adding to the channel drain noise-current the contribution of the excess noise stemming from the access region. For instance, in the linear region, the total drain noise-current becomes [26]:

$$\frac{S_{I_D}}{{I_D}^2} = \left(\frac{S_{I_D}}{{I_D}^2}\right)_{channel} + \left(\frac{I_D}{V_D}\right)^2 \times S_{RD} \tag{2}$$

where $S_{RD} = {R_{ON}}^2 \times \frac{S_{I_D}}{{I_D}^2}$ is the spectral density of source-drain series resistance and R_{ON} is the ON resistance.

From Eq. (2) we can say that if the normalized drain noise-current tends to increase at high drain currents, this is indicative of an enhanced LFN contribution of the access resistance [25]. Based on Fig. 5, since there is a drop in the normalized drain noise-current at the higher drain currents (i.e., even for devices having shorter L_G), data suggests that the LFN from access regions is negligible and the dominant noise source is more likely to be the gated channel for all of the studied devices.

The study of the variation of $\frac{S_{I_D}}{{I_D}^2}$ and $\left(\frac{G_m}{I_D}\right)^2$ with the drain current has been conducted to determine the applicability of the appropriate noise theory for the studied devices in this manuscript. As can be seen in Fig. 6, $\frac{S_{I_D}}{{I_D}^2}$ and $\left(\frac{G_m}{I_D}\right)^2$ both tend to saturate to a plateau at low drain currents. Additionally, they both exhibit a reduction with increasing the drain current. As suggested in [22], these results satisfy the carrier number fluctuations (CNF) with correlated mobility fluctuations (CNF/CMF) theory, which considers both the change of the flat-band voltage (V_{FB}) following the trapping/de-trapping of carriers and the mobility fluctuation of the charge carriers:

$$\frac{S_{I_D}}{{I_D}^2} = \left(1 + \Omega\ \frac{I_D}{G_m}\right)^2 \left(\frac{G_m}{I_D}\right)^2 S_{V_{FB}} \tag{3}$$

where $S_{V_{FB}}$ is the flat-band voltage power spectral density, which depends on the volume trap density, the effective

channel area, the frequency and the tunneling constant between channel and traps and Ω is the CMF coefficient given by:

$$\Omega = \alpha_{sc}\mu_{eff} \tag{4}$$

where μ_{eff} is the effective mobility and α_{sc} is the Coulomb scattering coefficient.

At low drain currents, where $\frac{S_{I_D}}{I_D{}^2}$ and $\left(\frac{G_m}{I_D}\right)^2$ are varying similarly with I_D, and where there is no significant difference in noise performance between the two studied device types, the model presented in [22] suggests that the dominant noise source is the CNF. At higher drain currents, where there is a substantial difference between $\frac{S_{I_D}}{I_D{}^2}$ and $\left(\frac{G_m}{I_D}\right)^2$, and where Type-II HFETs are showing higher normalized drain noise-current than Type-I HFETs, the model presented in [22] suggests the dominant noise source to be the CMF.

Considering the applicability of the CNF/CMF theory for a wide range of I_D, the model proposed by Kammeugne et al. [25] has been determined more convincingly adoptable for the determination of the dominant noise source among the reported devices.

Having made the observation of the dominance of the noise of the gated channel, studying the variation of the normalized drain noise-current versus the drain current has been observed to provide an interesting link between the LFN performance of the two device types and their earlier-mentioned differences in terms of dynamic variation of source access region resistance [11]. According to what has been reported in the work of Lee et al. [11], dynamically increasing source-access resistance of Type-II devices decreases the effective drive between gate electrode and the gated channel at higher drain currents, whereas due to the wider source-access region of Type-I HFETs, the source access resistance stays well below that of the gated channel for this latter group of devices. As a result, for this device type a large supply of the carriers from the source-access region to the gated-channel takes place. Considering the noted significance of mobility-fluctuations at high drain currents, the resulting presence of higher sheet carrier density under the gated channel for the Type-I HFETs at relatively higher values of I_D likely results in screening of the Coulomb interactions between channel carriers and scattering centers present in the channel or in the barrier layer [27]. Owing to this screening effect, both the mean value of the Coulomb scattering rate and the mobility fluctuations are expected to reduce, resulting in a reduced noise level of Type-I devices in comparison to Type-II HFETs. Also, the presence of relatively higher carrier density in Type-I HFETs at high drain currents overshadows the fluctuation of the number of charge carrier under the gated-channel, resulting in lower value of CNF term $S_{V_{FB}}$ compared to that of the Type-II HFETs for which the impact of CNF contribution is more evident. However, close to the threshold voltage the current supply from the source-access region to the gated channel stays at the same level. As a result of which, there can not be any substantial difference in the screening effect and/or carrier number fluctuation due to trapping/de-trapping of the carriers among the two device types, yielding the noise level to remain the same at relatively low drain currents.

V. CONCLUSION

The InAlN/GaN HFETs having fin structures present only in the gated channel exhibited not only the expected much better direct current (DC) performance, but at the same token a better 1/f LFN performance compared to the device having fins stretched from source to drain. These improvements are believed to have originated from the wider source-access region of the HFETs having fin structures present only under the gate which facilitates in maintaining the source access resistance well below of the gated channel. LFN in both types of HFETs is representable by the carrier number fluctuations with correlated mobility fluctuation, whereas the noise of the gated channel has been deemed likely to be as the dominant noise source. The presence of higher sheet charge density under the gated channel for devices having fins only under the gate can be explained by reducing the chances of mobility fluctuation owing to the carrier screening effect and the overshadowing of the carrier number fluctuation which is the result of trapping/de-trapping and/or tunneling of the carriers.

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