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Increased Threshold Voltage of Amorphous InGaZnO Thin-Film Transistors After Negative Bias Illumination Stress

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ABSTRACT Degradation phenomena featured with positive shift of the on-state transfer curve are reported for the amorphous InGaZnO (a-IGZO) thin-film transistors (TFTs) under negative bias illumination stress (NBIS). Such a positive shift is absent when the gate bias or the illumination is independently applied. With the assistance of TCAD simulation, the positive shift of the transfer curve is attributed to the generation of acceptor-like trap states, which is proposed to be due to oxygen interstitials produced as a consequence of electron generation by the illumination, acceleration under the effect of negative gate bias, and breaking weakly bonded oxygen. The proposed degradation mechanism is consistent with the low frequency noise characteristics and the degradation behavior under bipolar gate bias stress of the TFTs after NBIS. The whole degradation phenomena for the a-IGZO TFT under the NBIS are then consistently explained.

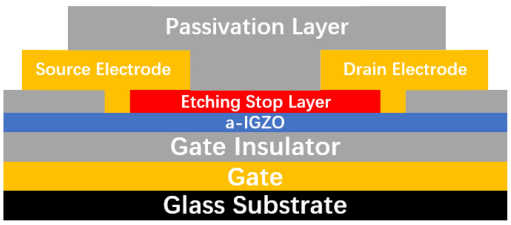
INDEX TERMS a-IGZO, thin-film transistor, negative bias illumination stress, acceptor-like trap states.

I. INTRODUCTION

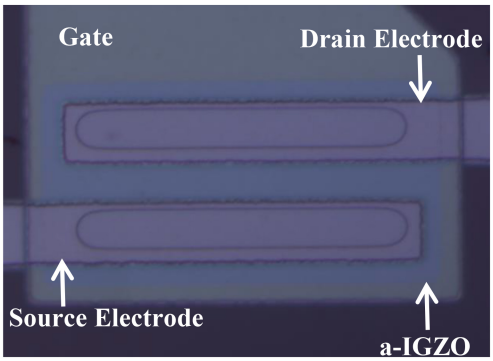
Amorphous InGaZnO (a-IGZO) thin-film transistor (TFT) is a promising technology for applications in active-matrix organic light-emitting diode (AMOLED) display [1] and DRAM application [2]. Despite its amorphous nature, low leakage current, small subthreshold swing (*SS*), and relatively high field-effect mobility can be readily achieved [3], [4]. However, oxygen related defects in the a-IGZO are potential issues affecting the reliability of the a-IGZO TFTs during their long-term operations. Understanding the degradation mechanisms under different bias stress conditions is the prerequisite for the optimization of device fabrication process and realization of a-IGZO TFTs with high reliability.

The two most frequently encountered bias conditions for the a-IGZO TFTs in active-matrix displays are positive gate bias stress (PBS) and negative gate bias stress (NBS). Under PBS, electron trapping in the gate dielectric or at the gate dielectric/channel interface is the dominant mechanism which causes the transfer curve to shift to the positive gate bias direction [5], [6], [7]. As holes are generally accepted to be absent in a-IGZO due to the existence of high-concentration donor-like trap states distributed in the bandgap near the valence band edge (E_V) [8], reduced V_{th} after NBS is attributed to the accumulation of ionized oxygen vacancies at the back a-IGZO surface [9]. More importantly, when illumination is applied in addition to the NBS, the negative bias illumination stress (NBIS) can induce an obvious negative shift of the transfer curve due to the ionization of neutral oxygen vacancies (V_O) though the a-IGZO TFTs may be stable under NBS [10], [11]. Supplying oxygen gas at a higher flow rate during the deposition of the a-IGZO or annealing the deposited a-IGZO in an oxygen atmosphere can reduce the V_O [12], [13], but excess oxygen in the a-IGZO will result into new reliability problems under PBS [14], [15].

In this work, increased V_{th} of a-IGZO TFTs under NBIS is observed, wherein the transfer curve in the on-state shifts sharply to the positive gate bias direction with deteriorated subthreshold characteristics after a small amount of negative



(a)



(b)

FIGURE 1. **(a) Schematic cross-sectional diagram and (b) optical plan-view picture of the a-IGZO TFT.**

shift. The increased V_{th} after NBIS is proposed to be due to the generation of oxygen interstitials, which function as acceptor-like trap states. The proposed mechanism is verified by the low frequency noise (LFN) characteristics and degradation behaviors under bipolar gate bias stress of the TFT after NBIS.

II. EXPERIMENTAL

The structure of the a-IGZO TFTs is schematically shown in Fig. 1, where the gate electrode is 300 nm molybdenum (Mo) and the gate dielectric is a stack of 150 nm nitride and 50 nm SiO_2 deposited by plasma-enhanced chemical vapor deposition (PECVD). The a-IGZO layer is 35 nm thick and deposited by RF magnetron sputtering. A 100 nm PECVD SiO_2 is used as the etching-stop layer (ESL) and 300 nm Mo forms the source/drain electrodes. After that 200 nm SiO_2 and 100 nm SiN_x were consecutively deposited by PECVD as the passivation layer and the source/drain electrodes were exposed. Finally, the TFTs were annealed in air ambient at 250 ^{o}C for 1 hour.

For the NBIS experiment, the negative bias was applied to the gate with source/drain grounded and the illumination was simultaneously applied from the passivation layer side, wherein a blue light-emitting diode with a wavelength of 445 nm was used. The photon energy of the illumination light is 2.51 eV, which is smaller than the bandgap of the a-IGZO. The default NBIS condition is a negative gate bias (V_{GS}) of -20 V with an illumination density (I_L) of 4.5 mW/cm^2. The transfer curves and capacitance-voltage (CV) curves

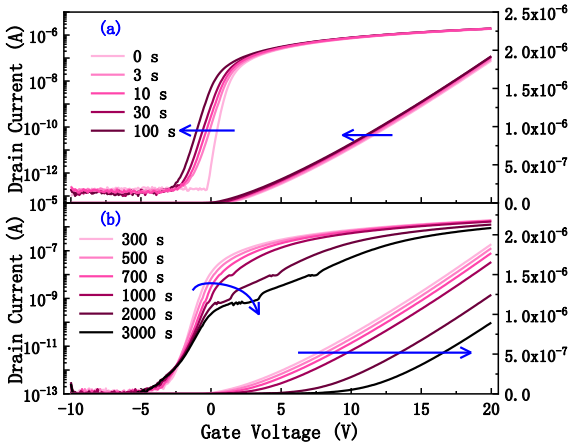


FIGURE 2. **Evolutions of the transfer curve under the default NBIS (a) in the first 100 s and (b) between 300 s and 3000 s.**

were measured with Agilent semiconductor parameter analyzer 4156C and LCR meter E4980, respectively. The LFN was measured with FS-pro multifunctional semiconductor parameter analyzer. Simulation of the transfer curve and CV curve were performed with Silvaco Atlas [16].

The transfer curves of the TFT before and after NBIS were measured at V_{DS} of 0.1 V. To characterize the degradation in the on-state of the a-IGZO TFT, the threshold voltage (V_{th}) is linearly extrapolated from the transfer curve, while the gate voltage when the transfer curve transits from the off-state region to the subthreshold region is defined as the turn-on voltage (V_{on}). The subthreshold swing (SS) is defined as the gate voltage difference when the drain current (I_D) increases from 10^{-11} A to 10^{-10} A in the subthreshold region. The default channel width and length of the TFT used in this paper are 50 μm and 10 μm except for that specially mentioned.

III. RESULTS AND DISCUSSION

Evolutions of the transfer curve of the a-IGZO TFT after NBIS are shown in Fig. 2. The on-state transfer curve in the linear scale shifts parallel to the negative gate bias direction in the first 100 s and then turns to shift to the positive gate bias direction instead. Thus, the shift of the transfer curve in the on-state is characterized by the variation of the threshold voltage from the initial one (ΔV_{th}). As shown in Fig. 3, ΔV_{th} is negative and reaches -0.53 V at the 100 s stress time. Then V_{th} starts to increase and ΔV_{th} turns out to be a positive 7.3 V after 3000 s stress time. Thus, though the mechanism for the reduction of V_{th} is initially dominant, it is finally overwhelmed by that for the increased V_{th}.

However, the subthreshold current does not exhibit parallel positive shift after NBIS as that in the on-state. The turn-on voltage shows a 2.26 V reduction after 100 s which is larger than that of 0.53 V for V_{th}. The difference between the variation of V_{on} (ΔV_{on}) and ΔV_{th} indicates the mechanism responsible for the degradation in the on-state and subthreshold current in the first 100 s is not

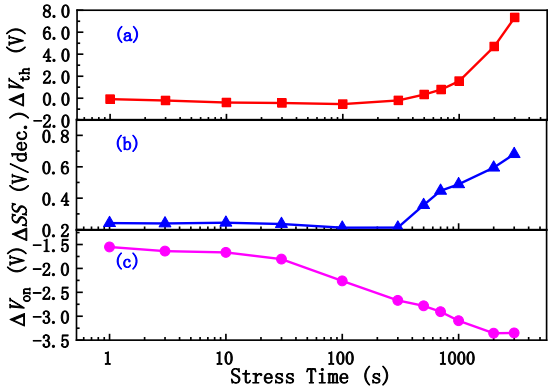


FIGURE 3. Dependence of (a) ΔV_{th}, (b) ΔSS, and (c) ΔV_{on} on stress time under the default NBIS.

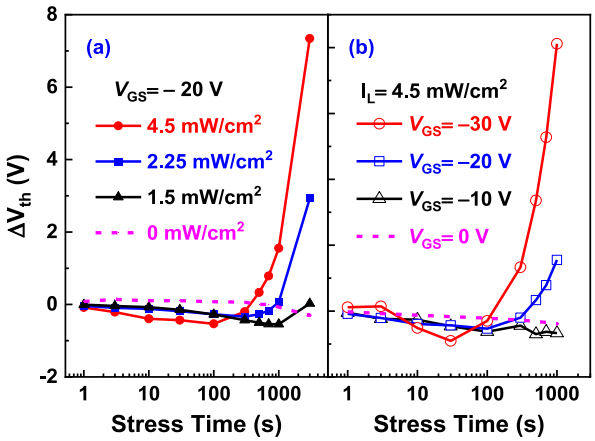


FIGURE 4. Effect of (a) illumination density and (b) gate bias on ΔV_{th} for the a-IGZO TFT under NBIS.

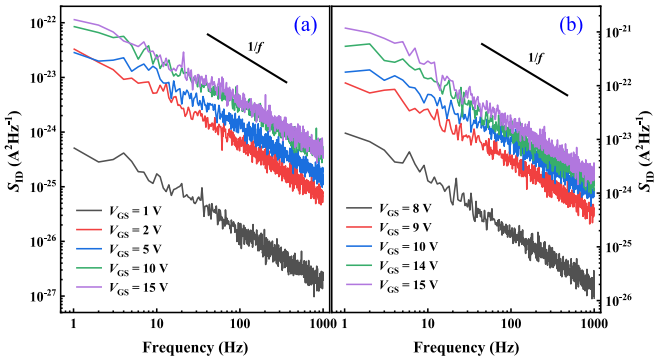


FIGURE 5. Plots of S_{ID} as a function of measured frequency at different gate voltages for (a) a pristine TFT and (b) the TFT underwent 3000 s default NBIS.

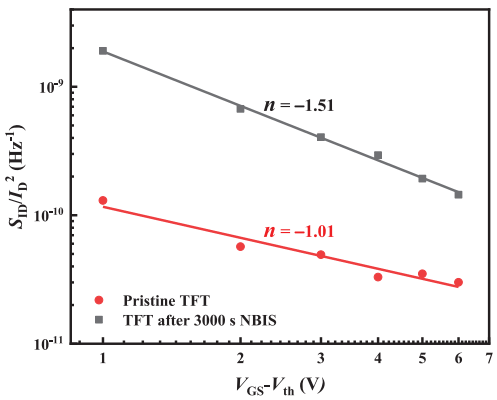


FIGURE 6. Comparison of S_{ID}/I_D^2 at 25 Hz versus the effective gate voltage for the pristine TFT and the TFT underwent NBIS.

due to the formation of positive charges in the gate oxide [16]. The subthreshold swing increased firstly from 0.27 V/decade to 0.57 V/decade and kept almost the same in the following stress time up to 300 s. After 300 s *SS* starts to synchronously increase with V_{th}. The simultaneous increase of *SS* and V_{th} in the second stress period shown in Fig. 3 implies the corresponding mechanisms are correlated. A current hump starts to appear in the subthreshold region of the transfer curve after 2000 s NBIS as shown in Fig. 2, indicating that more severe degradation occurs in the a-IGZO exposed to the illumination than that under the source/drain electrode.

Positive shift of the transfer curve of a-IGZO TFT can be explained by either the generation of charges in the insulators or the generation of trap states in the channel a-IGZO of the a-IGZO TFTs. For the former cases, it was explained with the generation of OH^- at the channel/dielectric interface from residual water moisture [18], [19] or the trapping of electrons at the back channel interface [20], where the generation of OH^- is an illumination independent process [9]. However, as shown in Fig. 4(a), the increase of V_{th} in this study exhibits a strong illumination dependence, i.e., ΔV_{th} reduces with the decrease of I_L and the increase of V_{th} is eventually absent when only a V_{GS} of −20 V is applied. Thus, generation of OH^- is excluded from the mechanism candidates explaining the observed increase of V_{th} after NBIS.

As a technique to clarify the degradation mechanism in TFTs [20], [21], LFN measurements were performed to a pristine a-IGZO TFT and that after NBIS to characterize the change in the a-IGZO TFT. The measured drain current noise power spectral density (S_{ID}) is firstly plotted versus the frequency as shown in Fig. 5. One can notice that the measured S_{ID} is inversely proportional the frequency at different gate voltages corresponding to the on-state region of the transfer curve. The dependence of S_I on frequency is fitted to be $S_{ID} \propto 1/f^{1.1}$, indicating that they are classical $1/f$ noise.

Then S_{ID} at a frequency of 25 Hz is normalized by I_D^2 and plotted versus the effective gate voltage (V_{GS}–V_{th}) as shown in Fig. 6, where power law dependence of the normalized drain current noise (S_{ID}/I_D^2) on the effective gate voltage can be observed for both the TFT before and after NBIS. But the power law coefficients (n) are different, i.e., it is −1.01 for the pristine TFT that for the TFT underwent NBIS increases to −1.51. Power law coefficient around −1 indicates a mobility fluctuation dominated noise generation while that around −2 refers to carrier number fluctuation

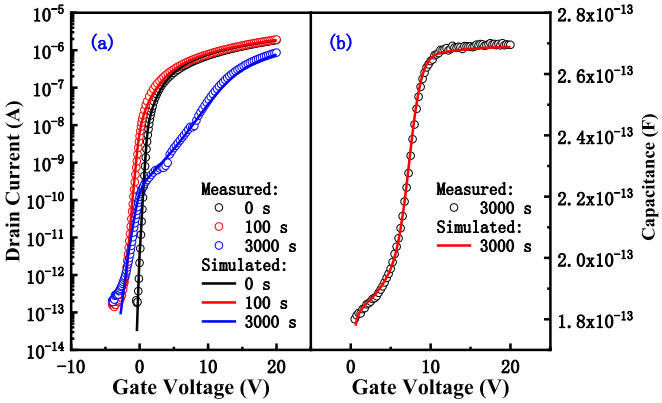


FIGURE 7. Comparison of the measured and simulated (a) transfer curves before and after NBIS and (b) CV curve after 3000 s default NBIS.

dominant noise [23]. If it were the electron trapping at the back interface between the a-IGZO and ESL or the generation of OH^- at the front interface between the gate oxide and the a-IGZO induces the positive shift of the transfer curve for the a-IGZO TFT after NBIS, it would be the carrier mobility fluctuation rather than the carrier number fluctuation increases in the low frequency noise and the power law coefficient would keep at around −1 [24]. So the increase of the power low coefficient after NBIS implies the increased contribution from carrier number fluctuation induced noise, which is resulted from the increase of trap states after NBIS [25].

The negative shift of the transfer curve and the deterioration of *SS* under NBIS in the first 100 s stress time can be explained by the generation of doubly charged oxygen vacancies (V_O^{2+}) and singly charged oxygen vacancies (V_O^{+}), which function as donor-like states and distribute close to and a little far away from the conduction band edge (E_C), respectively [25]. As shown in Fig. 7(a), the transfer curves after NBIS of 100 s were well fitted by increasing the density of donor-like states distributing in the 10 nm a-IGZO region adjacent to the gate dielectric [26]. The density of state (DOS) parameters for the simulation of the pristine TFT are summarized in Table 1 and those in the a-IGZO uncovered by the source/drain electrodes for the simulation of the transfer curve after NBIS are summarized in Table 2.

One can conclude from the negative shift of the transfer curve in the first 100 s NBIS that the effect from accumulation of ionized oxygen vacancies at the front channel surface, being responsible for the negative shift of the transfer curve [9], is more dominant than the effect from electron trapping at the back a-IGZO surface, which can lead to positive shift of the transfer curve [20]. So the positive shift of the transfer curve after 300 s NBIS is not due to trapping of NBIS generated electrons as ionized oxygen vacancies are also generated at the same time, which is consistent with the change in the LFN characteristics for the TFT before and after NBIS.

TABLE 1. DOS parameters for the defects in the a-IGZO of the pristine a-IGZO TFT.

Parameters	Description	Value
N_{TD} ($cm^{-3}eV^{-1}$)	peak concentration for the donor-like tail states	3.05×10^{16}
E_{TD} (eV)	peak position for N_{TD} relative to E_V	3.2
W_{TD} (eV)	decay energy of N_{TD}	0.4
N_{GD} ($cm^{-3}eV^{-1}$)	peak concentration for the donor-like deep states	1.0×10^{17}
E_{GD} (eV)	peak position for N_{GD} relative to E_V	2.7
W_{GD} (eV)	decay energy of N_{GD}	0.4
N_{TA} ($cm^{-3}eV^{-1}$)	concentration of acceptor-like trap states at E_C	2.0×10^{18}
W_{TA} (eV)	decay energy of N_{TA}	0.085
N_{GA} ($cm^{-3}eV^{-1}$)	peak concentration for the acceptor-like deep states	8.0×10^{15}
E_{GA} (eV)	peak position for N_{GA} relative to E_C	1.0
W_{GA} (eV)	decay energy of N_{GA}	0.5

TABLE 2. DOS parameters for the defects in the a-IGZO uncovered by the source/drain electrode of the TFT after 100 s and 3000 s NBIS.

Parameters	TFT after 100 s NBIS	TFT after 3000 s NBIS
N_{TD} ($cm^{-3}eV^{-1}$)	4.18×10^{18}	4.18×10^{18}
E_{TD} (eV)	3.2	3.2
W_{TD} (eV)	0.5	0.5
N_{GD} ($cm^{-3}eV^{-1}$)	5.1×10^{18}	2.56×10^{19}
E_{GD} (eV)	2.7	2.7
W_{GD} (eV)	0.4	0.4
N_{TA} ($cm^{-3}eV^{-1}$)	2.0×10^{18}	2.0×10^{18}
W_{TA} (eV)	0.085	0.085
N_{GA} ($cm^{-3}eV^{-1}$)	2.08×10^{17}	1.85×10^{18}
E_{GA} (eV)	1	1
W_{GA} (eV)	0.5	0.5

The on-state characteristics of the a-IGZO TFTs after 3000 s NBIS was then successfully fitted by increasing the density of acceptor-like deep states (g_{GA}) in addition to the increased donor-like deep states (g_{GD}) for the fitting of the subthreshold characteristics. It indicates that new acceptor-like deep states were generated during the NBIS. g_{GA} and g_{GD} used for the simulations of the transfer curves for the pristine TFT and those for the TFT underwent NBIS of 100 s and 3000 s are further compared in Fig. 8(a) and Fig. 8 (b), respectively. But because the acceptor-like trap states generated in the a-IGZO is estimated to be 1.6×10^{18} cm^{-3} after integrating the distribution profile of the acceptor-like trap states with the parameters listed in Table 2, which is less than 2% of the trap states introduced by oxygen vacancies [8], it is difficult to identify generated interstitial oxygen in the channel a-IGZO with X-ray photoelectron spectroscopy.

In addition to the transfer curves, the CV curves for the a-IGZO TFT after 3000 s NBIS were measured at a frequency of 300 kHz. One can notice from Fig. 7(b) that

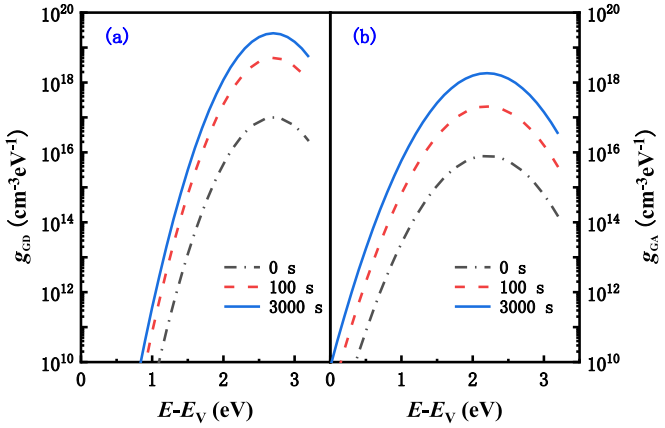


FIGURE 8. Comparison of (a) g_{GD} and (b) g_{GA} extracted from the simulation of pristine TFT and that underwent NBIS of 100 s and 3000 s.

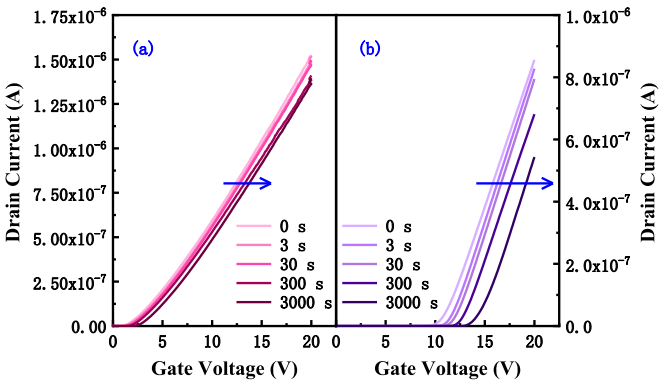


FIGURE 9. Evolutions of the transfer curve for (a) a pristine TFT and (b) one TFT underwent NBIS after the same bipolar gate bias stress. The channel width and length of the TFTs are 40 μm and 9 μm.

the measured CV curve can be well fitted by the simulation result with the same trap state distributions for the simulation of the transfer curve after 3000 s NBIS, confirming that the increased trap states after NBIS shown in Fig. 8 is reasonable.

Acceptor-like trap states play an important role in the dynamic degradation of n-type TFTs under bipolar gate bias stress [28], so the degradation of a pristine TFT and one TFT underwent NBIS after the same bipolar gate pulse stress is compared, where the pulse valley voltage is −20 V and the pulse peak voltage is 20 V, the pulse rising and falling time are 0.1 μs and the pulse duty ratio is 50%. As shown in Fig. 9, both the transfer curves for the pristine TFT and that underwent NBIS exhibit positive shift as previously reported [29]. But the ΔV_{th} for the TFT after NBIS is larger, i.e., after 3000 s it is 3.65 V for the TFT underwent NBIS and 1.14 V for the pristine TFT. The dynamic degradation of the TFTs under bipolar gate bias stress is induced by the transient electric field (E_x) and carriers during the pulse transition edges. The severe degradation for the TFT after NBIS is consistent with its higher g_{GA} which leads to higher transient electron concentration (n_e) as shown in Fig. 10(b) [30].

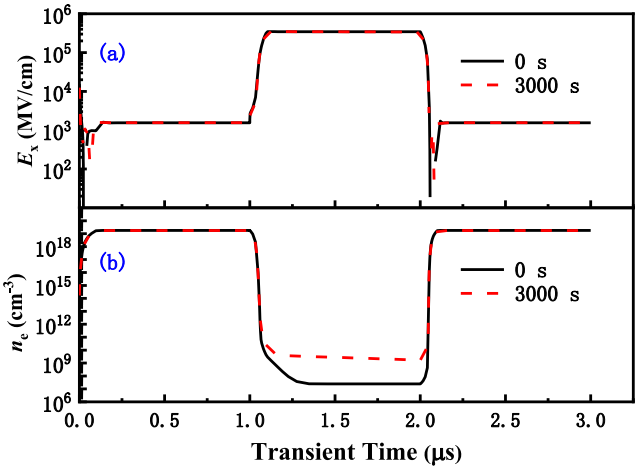


FIGURE 10. Comparison of the simulated (a) transient lateral electric field (E_x) and (b) n_e for the pristine TFT and the TFT underwent 3000 s NBIS.

In addition to oxygen vacancies, oxygen interstitials (O_i) is another kind of stoichiometric defects in a-IGZO [31], which have been theoretically calculated to function as acceptor-like trap states [32]. The electron concentration in the channel a-IGZO will be reduced due to the trapping of electrons by the increased acceptor-like trap states, which is consistent with the observed increase of V_{th} under NBIS. Thus, the generated acceptor-like trap states after NBIS is attributed to the generation of O_i. Residual excess oxygen in a-IGZO can exist in the form of oxygen-oxygen dimer [32], but it will lead to the decrease rather than increase of V_{th} of a-IGZO TFT under NBIS [14].

In addition to the illumination, one can notice in Fig. 4(b) that the increase of V_{th} is also affected by the magnitude of the negative gate bias during NBIS, i.e., the increase of V_{th} is reduced with the reduction of the magnitude of the negative gate bias and it's absent when only the illumination with I_L of 4.5 mW/cm^2 is applied. Therefore, the generation of O_i under NBIS is the collective result of effects from negative gate bias and illumination.

As ionization of oxygen vacancies and generation of oxygen interstitials are involved in the NBIS degradation and the degradation relates to both the gate bias and illumination, the degradation mechanism is thus proposed as schematically shown in Fig. 11. Ionization of the pre-existing V_O in the a-IGZO took place firstly by the illumination during NBIS. The generated V_O^+ and V_O^{2+}, functioning as donor-like trap states resulted into the increased *SS* and negative shift of the transfer curve in the first degradation stage. The weaker dependence of ΔV_{th} in the first stage on the gate bias and illumination shown in Fig. 4 indicates that the concentration of pre-existing V_O in the a-IGZO is relatively small [33].

When the electrons generated after ionization of pre-existing V_O drift further toward the back surface of the a-IGZO under the negative gate bias, those electrons with high energy may break weak metal-oxygen bonds, thereby simultaneously triggering the generation of O_i

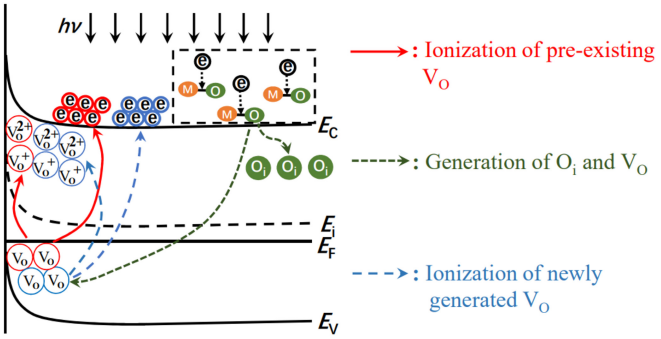


FIGURE 11. Schematic diagram showing the ionization of pre-existing V_O, generation of V_O and O_i and ionization of newly generated V_O in the a-IGZO under NBIS.

and V_O as Frenkel defects [34], [35]. Ionization of the newly generated V_O further increases *SS* and the generated O_i increases V_{th} of the a-IGZO TFT, which is consistent with simultaneous occurrence of increase of *SS* and V_{th} in the second degradation stage as shown in Fig. 3.

IV. CONCLUSION

Significant increase of V_{th} of a-IGZO TFTs after NBIS is observed and reported, which is resulted from the collective effects from the illumination and negative gate bias. Oxygen interstitials are proposed to be generated after NBIS, which function as acceptor-like trap states. The proposed generation of oxygen interstitials, functioning at acceptor-like trap states, is consistent with the LFN and reliability performance of the a-IGZO TFT after NBIS. The research results indicate the importance of strengthening the chemical bonds in a-IGZO in addition to the reduction of oxygen vacancies.

REFERENCES

[1] T.-K. Chang, C.-W. Lin, and S.-C. Chang, "LTPO TFT technology for AMOLEDs," in *SID Symp. Dig. Tech. Papers*, vol. 50, Jun. 2019, pp. 545–548, doi: 10.1002/sdtp.12978.

[2] K. Chen et al., "Improved multi-bit statistics of novel dual-gate IGZO 2T0C DRAM with in-cell V_{TH} compensation and $\Delta V_{SN}/\Delta V_{DATA}$ boosting technique," in *Int. Electron Devices Meeting Dig. Paper*, 2023, pp. 1–4, doi: 10.1109/IEDM45741.2023.10413770.

[3] H. Yabuta et al., "High-mobility thin-film transistor with amorphous $InGaZnO_4$ channel fabricated by room temperature RF-magnetron sputtering," *Appl. Phys. Lett.*, vol. 89, no. 11, Sep. 2006, Art. no. 112123, doi: 10.1063/1.2353811.

[4] T. Pi et al., "High-performance a-IGZO TFT fabricated with ultralow thermal budget via microwave annealing," *IEEE Trans. Electron Device*, vol. 69, no. 1, pp. 156–159, Jan. 2022, doi: 10.1109/TED.2021.3126692.

[5] K. Hoshino, D. Hong, H. Q. Chiang, and J. F. Wager, "Constant-voltage-bias stress testing of a-IGZO thin-film transistors," *IEEE Trans. Electron Device*, vol. 56, no. 7, pp. 1365–1370, Jul. 2009, doi: 10.1109/TED.2009.2021339.

[6] J. M. Lee, I.-T. Cho, J.-H. Lee, and H.-I. Kwon, "Bias-stress-induced stretched exponential time dependence of threshold voltage shift in InGaZnO thin film transistors," *Appl. Phys. Lett.*, vol. 93, no. 9, Sep. 2008, Art. no. 93504, doi: 10.1063/1.2977865.

[7] T.-C. Chen et al., "Investigating the degradation behavior caused by charge trapping effect under DC and AC gate bias stress for InGaZnO thin film transistor," *Appl. Phys. Lett.*, vol. 99, no. 2, Jul. 2011, Art. no. 22104, doi: 10.1063/1.3609873.

[8] K. Nomura et al., "Subgap states in transparent amorphous oxide semiconductor In-Ga-Zn-O observed by bulk sensitive X-ray photoelectron spectroscopy," *Appl. Phys. Lett.*, vol. 92, no. 20, May 2008, Art. no. 202117, doi: 10.1063/1.2927306.

[9] S. Li, M. Wang, D. Zhang, H. Wang, and Q. Shan, "A unified degradation model of a-InGaZnO TFTs under negative gate bias with or without an illumination," *IEEE J. Electron Devices Soc.*, vol. 7, no. 1, pp. 1063–1071, Oct. 2019, doi: 10.1109/JEDS.2019.2946383.

[10] H. Oh, S.-M. Yoon, M. K. Ryu, and C.-S. Hwang, "Photon-accelerated negative bias instability involving subgap states creation in amorphous In-Ga-Zn-O thin film transistor," *Appl. Phys. Lett.*, vol. 97, no. 18, Nov. 2010, Art. no. 183502, doi: 10.1063/1.3510471.

[11] J. G. Um, M. Mativenga, P. Migliorato, and J. Jang, "Increase of interface and bulk density of states in amorphous-indium-gallium-zinc-oxide thin-film transistors with negative-bias-under-illumination-stress time," *Appl. Phys. Lett.*, vol. 101, no. 11, Sep. 2012, Art. no. 113504, doi: 10.1063/1.4751849.

[12] K. H. Ji et al., "Effect of high-pressure oxygen annealing on negative bias illumination stress-induced instability of InGaZnO thin film transistors," *Appl. Phys. Lett.*, vol. 98, no. 10, Mar. 2011, Art. no. 103509, doi: 10.1063/1.3564882.

[13] G. W. Yang, J. Park, S. Choi, C. Kim, and D. M. Kim, "Total subgap range density of states-based analysis of the effect of oxygen flow rate on the bias stress instabilities in a-IGZO TFTs," *IEEE Trans. Electron Device*, vol. 69, no. 1, pp. 166–173, Jan. 2022, doi: 10.1109/TED.2021.3130219.

[14] S. Choi et al., "Excessive oxygen peroxide model-based analysis of positive-bias-stress and negative-bias-illumination-stress instabilities in self-aligned top-gate coplanar In–Ga–Zn–O thin-film transistors," *Adv. Electron. Mater.*, vol. 8, no. 5, May 2022, Art. no. 2101062, doi: 10.1002/aelm.202101062.

[15] S. Kim, Y. W. Jeon, Y. Kim, D. Kim, and H. K. Jung, "Impact of oxygen flow rate on the instability under positive bias stresses in DC-sputtered amorphous InGaZnO thin-film transistors," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 62–64, Jan. 2012, doi: 10.1109/LED.2011.2173153.

[16] (Silvaco, Santa Clara, CA, USA). *ATLAS User's Manual*. (Sep. 2014). [Online]. Available: http://www.Silvaco.com

[17] N. Liang, D. Zhang, M. Wang, H. Wang, Y. Yu, and D. Qi, "Investigations on the negative shift of the threshold voltage of polycrystalline silicon thin-film transistors under positive gate bias stress," *IEEE Trans. Electron Device*, vol. 68, no. 2, pp. 550–555, Feb. 2021, doi: 10.1109/TED.2020.3041568.

[18] N. D. Young and A. Gill, "Water-related instability in TFTs formed using deposited gate oxides," *Semicond. Sci. Technol.*, vol. 7, no. 8, pp. 1103–1108, Apr. 1992, doi: 10.1088/0268-1242/7/8/013.

[19] J.-C. Jhu, T.-C. Chang, K.-C. Chang, C.-Y. Yang, and W.-C. Chou, "Investigation of hydration reaction-induced protons transport in etching-stop a-InGaZnO thin-film transistors," *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1050–1052, Oct. 2015, doi: 10.1109/LED.2015.2466103.

[20] M. P. Hung, D. Wang, J. Jiang, and M. Furuta, "Negative bias and illumination stress induced electron trapping at back-channel interface of InGaZnO thin-film transistor," *ECS Solid State Lett.*, vol. 3, no. 3, pp. 13–16, Jan. 2014, doi: 10.1149/2.010403ssl.

[21] Z. Jiang, M. Zhang, S. Den, Y. Yang, M. Wong, and H.-S. Kwok, "Evaluation of positive-bias-stress-induced degradation in InSnZnO thin-film transistors by low frequency noise measurement," *IEEE Electron Device Lett.*, vol. 43, no. 6, pp. 886–889, Jun. 2022, doi: 10.1109/LED.2022.3165558.

[22] A. Tsormpatzoglou, N. A. Hastas, F. Mahmoudabadi, N. Choi, M. K. Hatalis, and C. A. Dimitriadis, "Characterization of high-current stress-induced instability in amorphous InGaZnO thin-film transistors by low-frequency noise measurements," *IEEE Electron Device Lett.*, vol. 34, no. 11, pp. 1403–1405, Nov. 2013, doi: 10.1109/LED.2013.2281948.

[23] T.-C. Fung, G. Baek, and J. Kanicki, "Low frequency noise in long channel amorphous In–Ga–Zn–O thin film transistors," *J. Appl. Phys.*, vol. 108, no. 7, Oct. 2010, Art. no. 74518, doi: 10.1063/1.3490193.

[24] M. Piero, M. D. H. Chowdhury, J. G. Um, M. J. Seok, M. Mallory, and J. Jin, "Characterization and modeling of a-IGZO TFTs," *J. Disp. Technol.*, vol. 11, no. 6, pp. 497–505, Jun. 2015, doi: 10.1109/JDT.2014.2328335.

[25] C.-Y. Jeong et al., "Investigation of the low-frequency noise behavior and its correlation with the subgap density of states and bias-induced instabilities in amorphous InGaZnO thin-film transistors with various oxygen flow rates," *Jpn. J. Appl. Phys.*, vol. 51, no. 10, Oct. 2012, Art. no. 100206, doi: 10.1143/JJAP.51.100206.

[26] J. Guo, D. Zhang, M. Wang, and H. Wang, "Degradation and its fast recovery in a-IGZO thin-film transistors under negative gate bias stress," *Chin. Phys. B*, vol. 30, no. 11, Oct. 2021, Art. no. 118102, doi: 10.1088/1674-1056/ac05aa.

[27] J.-H. Lee, H.-I. Kwon, H. Shin, B.-G. Park, and Y. J. Park, "Electrical instabilities and low-frequency noise in InGaZnO thin film transistors," in *17th IEEE Int. Symp. Phys. Failure Anal. Integr. Circuits Dig. Paper*, Jul. 2010, pp. 1–7, doi: 10.1109/IPFA.2010.5532306.

[28] T. Gao, M. Wang, H. Wang, and D. Zhang, "TCAD analysis of the four-terminal poly-Si TFTs on suppression mechanisms of the DC and AC hot-carrier degradation," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 606–612, 2019, doi: 10.1109/JEDS.2019.2916619.

[29] H. Wang, M. Wang, and Q. Shan, "Dynamic degradation of a-InGaZnO thin-film transistors under pulsed gate voltage stress," *Appl. Phys. Lett.*, vol. 106, Apr. 2015, Art. no. 133506, doi: 10.1063/1.4916825.

[30] Y. Yang, D. Zhang, M. Wang, L. Lu, and M. Wong, "Suppressed degradation of elevated-metal metal-oxide thin-film transistors under bipolar gate pulse stress," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 707–710, May 2018, doi: 10.1109/LED.2018.2821366.

[31] A. de Jamblinne de Meux, G. Pourtois, J. Genoe, and P. Heremans, "Defects in amorphous semiconductors: The case of amorphous indium gallium zinc oxide," *Phys. Rev. Appl.*, vol. 9, May 2018, Art. no. 54039, doi: 10.1103/PhysRevApplied.9.054039.

[32] W. H. Han, Y. Jun Oh, K. J. Chang, and J.-S. Park, "Electronic structure of oxygen interstitial defects in amorphous In-Ga-Zn-O semiconductors and implications for device behavior," *Phys. Rev. Appl.*, vol. 3, Apr. 2015, Art. no. 44008, doi: 10.1103/PhysRevApplied.3.044008.

[33] K.-A. Kim, M.-J. Park, W.-H. Lee, and S.-M. Yoon, "Characterization of negative bias-illumination-stress stability for transparent top-gate In-Ga-Zn-O thin-film transistors with variations in the incorporated oxygen content," *J. Appl. Phys.*, vol. 118, no. 23, Dec. 2015, Art. no. 234504, doi: 10.1063/1.4938013.

[34] X. Zhou et al., "Oxygen interstitial creation in a-IGZO thin-film transistors under positive gate-bias stress," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1252–1254, Sep. 2017, doi: 10.1109/LED.2017.2723162.

[35] W. Wu et al., "Improved reliability of a-IGZO thin-film transistor under positive gate bias stress by utilizing NH_3 plasma treatment," *Microelectron. Rel.*, vol. 151, Dec. 2023, Art. no. 115257, doi: 10.1016/j.microrel.2023.115257.