

Received 23 December 2023; revised 19 February 2024 and 20 March 2024; accepted 7 April 2024. Date of publication 15 April 2024; date of current version 8 May 2024. The review of this article was arranged by Editor P. Pavan.

Digital Object Identifier 10.1109/JEDS.2024.3388840

An Experimentally Verified Temperature Dependent Drain Current Fluctuation Model for Low Temperature Applications

YING SUN¹ (Graduate Student Member, IEEE), YUCHEN GU¹, JING WAN² (Senior Member, IEEE),
XIAO YU³ (Member, IEEE), BING CHEN⁴ (Member, IEEE), DAWEI GAO¹, RAN CHENG¹ (Member, IEEE),
AND GENQUAN HAN⁴ (Senior Member, IEEE)

1 College of Integrated Circuits, Zhejiang University, Hangzhou 311200, China
2 School of Information Science and Technology, Fudan University, Shanghai 200438, China
3 Research Center for Intelligent Chips, Zhejiang Lab, Hangzhou 311121, China
4 Hangzhou Institute of Technology, Xidian University, Hangzhou 311200, China

CORRESPONDING AUTHOR: R. CHENG (e-mail: chengran@zju.edu.cn)

This work was supported in part by the Fundamental Research Funds for the Central Universities under Grant 226-2023-00004; in part by the National Natural Science Foundation of China under Grant 62025402; in part by the Zhejiang Provincial Natural Science Foundation under Grant LDQ24F040001; in part by the Kun-Peng Program of Zhejiang Province (H. W.); in part by the Zhejiang Provincial Key Research and Development Program under Grant 2022C01063; and in part by the support from the Technology Innovation and Training Center, Polytechnic Institute, Zhejiang University, Hangzhou, Zhejiang, China.

ABSTRACT In this work, an accurate temperature-dependent drain current I_D fluctuation model valid from 10 to 300 K was proposed for 18 nm ultra-thin body and buried oxide (UTBB) n-channel field effect transistors (n-FETs). The temperature dependence of I_D fluctuation was characterized and investigated from 300 K down to 10 K. In moderate inversion mode, I_D fluctuation is more severe at sub-100 K while in the strong inversion mode, it still can be overshadowed by the charge screening effect. Cryogenic virtual source (CVS) device model was used to extract and analyze the carrier density and mobility which are used in the current fluctuation model. The current fluctuation model was experimentally verified under different inversion conditions, showing it can be used to analyze and optimize the flicker noise in the low temperature (LT) circuit applications.

INDEX TERMS Drain current fluctuation, low temperature, UTBB n-FET, scattering mechanism, virtual-source model.

I. INTRODUCTION

The rapid development of quantum computing [1] as well as the low temperature logic technology [2] activate the exploration on low temperature (LT) complementary metal oxide semiconductor (CMOS) devices and circuits. As transistors cool down to sub-10 K, their electrical parameters shift drastically since the carrier transport mechanisms are different [3]. The changed device parameters will consequently lead to the deterioration of circuit functions. On the other hand, at lower temperatures, the smaller subthreshold swing (SS) and lower leakage current can be beneficial to the reduction of power consumption [4]. For cryogenic circuits, operating in weak or moderate inversion regions can lead to maximum voltage gain, lower power dissipation and minimum total harmonic distortion [5]. However, at sub-10 K,

the drain current I_D fluctuation is much more severe due to the quantum tunneling of border traps, especially at weak or moderate inversion regions [6], [7], [8], [9], [10], [11], [12], [13], [14]. Several works on the current fluctuation at cryogenic temperatures ($T < 15$ K) and very low drain voltage V_D conditions ($V_D \leq 50$ mV) show that the current fluctuation induced by the coulomb blockade and resonant tunneling increases abnormally due to the more profound influence from the quantum dots at cryogenic temperatures for short-channel MOS transistors [6], [7], [10], [11]. The study of cryogenic low frequency noise shows that there is a strong correlation between the excess $1/f$ noise and the saturation of the SS at low temperatures [12], [13], [14]. The increased I_D fluctuation may further affect the performance of analog circuits and make functional errors in digital

circuits [15], [16], [17], [18] in cryogenic environment. Therefore, a temperature-dependent I_D fluctuation model is necessary to analyze and predict the optimal bias conditions to minimize the flicker noise in the LT circuits.

To establish such a model, I_D fluctuation for 18 nm ultra-thin body and buried oxide (UTBB) n-channel field effect transistors (n-FETs) was characterized and analyzed from 10 K to 300 K. The mechanisms leading to the change of I_D fluctuation as temperature decreases for different gate bias V_G conditions were investigated and compared. A cryogenic virtual source (CVS) device model [19] was exploited to extract accurate scattering-related parameters from the LT electrical data. Eventually, based on the experimental characterization and analysis, a temperature-dependent unified current fluctuation model was derived and verified, which can be used to model and optimize the noise issues in the LT circuits.

II. DEVICE AND MEASUREMENT SETUP

The devices-under-test (DUTs) were fabricated by foundry-level 22 nm UTBB CMOS process [20] with HfO_2 -based high- κ /metal gate stack (HKMG). The gate length L_G of the DUT is 18 nm and the gate width W_G of the DUT is 480 nm. The equivalent oxide thickness (EOT) of the gate stack is ~ 1 nm. The thickness of the buried oxide layer (BOX) is 20 nm, and the thickness of the channel is 6 nm. Tektronix 4200A semiconductor analyzer was used for the time-domain current sampling (I - t) test. The sampling interval is 30 ms. Lakeshore cryogenic probe station was used to provide the cryogenic environment for the current fluctuation characterization from 10 K to 300 K, and the temperature T step is 20 K when T is higher than 20 K. At each temperature point, the I - t characteristics were measured under the V_G from 100 mV to 800 mV (minimum step = 10 mV) and the V_D at 800 mV.

III. RESULTS AND DISCUSSION

A. TEMPERATURE DEPENDENCE OF THE I_D FLUCTUATION

Figs. 1(a)-(f) and (g)-(l) compare the I_D fluctuation as T increases from 10 K to 300 K for a DUT operated in the weak to moderate inversion mode ($V_G = 480$ mV, $V_D = 800$ mV) and the strong inversion mode ($V_G = 800$ mV, $V_D = 800$ mV), respectively. At any time t , the I_D fluctuation is defined as $I_{D,T}(t)/\bar{I}_{D,T}$, where $I_{D,T}(t)$ is the real-time I_D measured at each temperature, $\bar{I}_{D,T}$ is the averaged I_D over the total measurement time at the same temperature. As shown in Fig. 1, the I_D fluctuations become severe as the T cools down if the V_G keeps unchanged. As shown in Figs. 1(a)-(f), in the weak/moderate inversion mode, the fluctuation does not change too much from 300 K to 180 K. However, as T reduces to 180 K and below, the current fluctuation increases obviously as T reduces. To qualitatively analyze the temperature dependency of the I_D fluctuation, the amplitude of $I_{D,T}(t)/\bar{I}_{D,T}$ was calculated as

$$\Delta I_D/I_D = [\text{high}(I_{D,T}) - \text{low}(I_{D,T})]/\bar{I}_{D,T}. \quad (1)$$

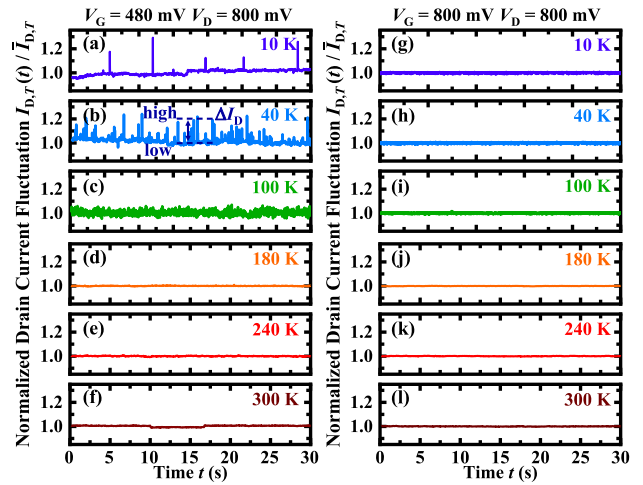


FIGURE 1. (a)-(f) The real-time I_D fluctuation $I_{D,T}(t)/\bar{I}_{D,T}$ at $V_G = 480$ mV and $V_D = 800$ mV for an 18 nm UTBB n-FET. The amplitude of I_D fluctuation ($\Delta I_D/I_D$) is 26.8% at 10 K, and 1.82% at 300 K. (g)-(l) $I_{D,T}(t)/\bar{I}_{D,T}$ at $V_G = 800$ mV and $V_D = 800$ mV. The I_D fluctuation at the strong inversion condition is significantly smaller than those in the weak or moderate inversion condition.

Here, $\text{high}[I_{D,T}]$ and $\text{low}[I_{D,T}]$, as shown in Fig. 1(b), were extracted by a self-developed K-Medoids method [21], representing the average values of the high- and low-state I_D clusters, respectively. $\Delta I_D/I_D$ is calculated as the statistical average of the current fluctuation at each measurement time frame. Therefore, the current fluctuation due to different traps is statistically included in the model. $\Delta I_D/I_D$ is 0.57% at 180 K, and it increases to 26.8% at 10 K. On the other hand, for the same transistor operated in the strong inversion mode as shown in Figs. 1(g)-(l), similar temperature dependency can also be found but the magnitude of $\Delta I_D/I_D$ is much smaller, since the current fluctuation in the strong inversion mode is significantly reduced by the charge screening of high-density carriers in the channel [22]. In the weak/moderate inversion mode, the coulomb potential of traps at the interface may block part of the channel, resulting in an inhomogeneous current flow. Whereas, in the strong inversion mode, current flow is more homogeneous as the high-density carriers in the channel screen the impact from the local trap potentials. Therefore, $\Delta I_D/I_D$ is generally higher in the weak/moderate inversion mode than that in the strong inversion mode.

B. PARAMETER EXTRACTION FOR THE I_D FLUCTUATION MODEL

A unified I_D fluctuation model was proposed here to understand the temperature dependency of I_D fluctuation at LT. According to Hung et al. [23], $\Delta I_D/I_D$ can be related to the low-field mobility μ and the surface charge density N as

$$\frac{\Delta I_D}{I_D} = \frac{-1}{W_G \times L_G} \left(\frac{1}{N} - \alpha \mu \right), \quad (2)$$

where α is the scattering coefficient due to coulomb scattering. As the gate capacitance for 18 nm UTBB FETs is too small to be measured, N and μ cannot be directly

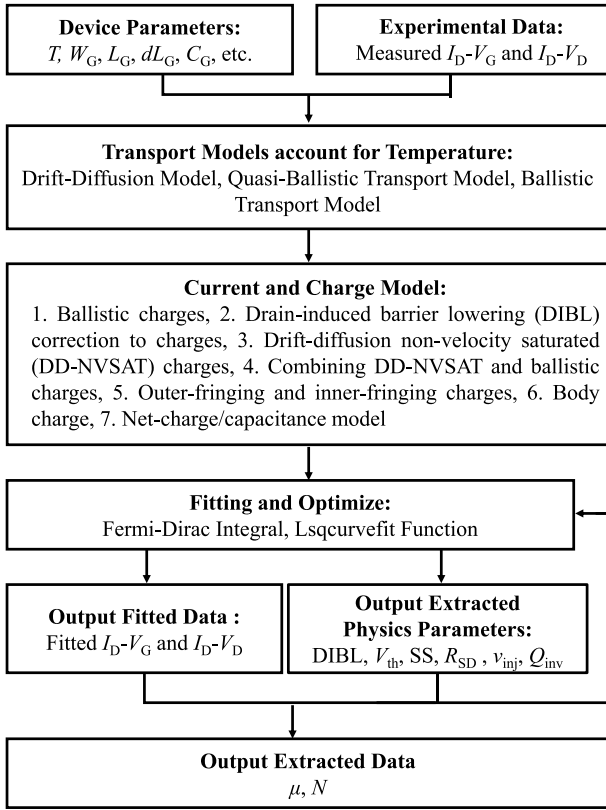


FIGURE 2. Flow chart of the CVS model for parameter extraction. This model requires only 12 input parameters such as T , W_G , L_G , overlap length including both source and drain sides dL_G , gate-to-channel area capacitance at the virtual source C_G etc., to fit its calculated current-voltage (I - V) curves with the experimental ones. With the diffusive, quasi-ballistic, ballistic transport and low temperature model included in the CVS model, the parameters such as μ and N can be directly extracted and output.

obtained from the experiment. To get the values of N and μ , the CVS model was exploited to extract parameters from 10 K to 300 K [19]. The CVS model is a semi-empirical physics-based device model for nanoscale FETs. Diffusive, quasi-ballistic model, ballistic transport model, and the low temperature model are all included in the CVS model for accurate data fitting and parameter extraction [24], [25], [26]. The parameter extraction process of the CVS model is illustrated in Fig. 2, and a detailed description on the extraction process can be found in [19]. In this model, the surface charge density $N(V_G, V_D)$ is calculated as

$$N(V_G, V_D) = \phi_t C_{inv} m \ln\left(1 + e^{(V_G - V_{th} + \theta \phi_t F_f)/m \phi_t}\right) / e, \quad (3)$$

where $\phi_t = k_B T/q$, k_B is the Boltzmann constant, C_{inv} is the inversion gate capacitance, m is the subthreshold coefficient, which is related to the SS by $SS = m \phi_t \ln 10$, θ is empirical parameters associated with threshold voltage shift between the strong and weak inversion, “inversion transition” function F_f is a Fermi function that allows for a smooth transition between the two values of reference voltage and is centered at the point halfway between them.

Fig. 3(a) shows the measured and the fitted I_D - V_G characteristics for a UTBB FET at 10 K, 100 K, 200 K and 300

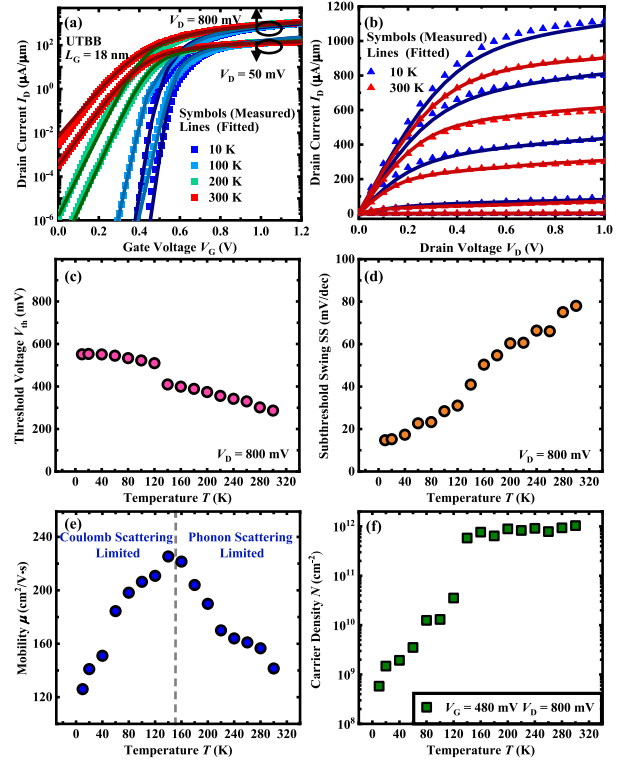


FIGURE 3. (a) I_D - V_G characteristics for an 18 nm UTBB n-FET measured at 10 K, 100 K, 200 K, and 300 K. The symbols are the experimental data, and the lines are fitted using the CVS model. The fitted data are in good agreement with the experimental I_D - V_G data from 10 K to 300 K. (b) The measured and fitted I_D - V_D characteristics at 10 K and 300 K. (c) V_{th} is extracted by the constant current method at an I_D of 5.56 $\mu A/\mu m$. As T decreases from 300 K to 10 K, it shifts from 286 mV to 551 mV, as shown in Fig. 3(c), and SS decreases from 79.6 mV/dec to 14.7 mV/dec, as shown in Fig. 3(d). μ for T from 10 to 300 K was extracted at a fixed N and provided in Fig. 3(e). For T increases from 10 K to ~ 150 K, μ increases due to the reduced coulomb scattering [27], [28]. As already reported by some studies on the cryogenic mobility of UTBB transistors, higher level of interface traps will lead to a stronger dependency of μ on the coulomb scattering when the temperature decreases [28], [29], [30]. In addition, the devices used in this study are fabricated with higher channel doping concentration, which also leads to a stronger dependency of μ on the coulomb scattering. Therefore, the obvious decrease of μ as T reduces from 150 K should be attributed to the high channel doping level, the interface traps, and the neutral atoms. Whereas, for T higher than 150 K, the phonon scattering starts to

K for $V_D = 50$ mV and 0.8 V. The measured and the fitted I_D - V_D characteristics are shown in Fig. 3(b) for 10 K and 300 K. As shown in Fig. 3, the fitted curves coincide well with the measured data, which is necessary to guarantee the accurate parameter extraction from the model. The threshold voltage V_{th} is extracted by the constant current method at an I_D of 5.56 $\mu A/\mu m$. As T decreases from 300 K to 10 K, it shifts from 286 mV to 551 mV, as shown in Fig. 3(c), and SS decreases from 79.6 mV/dec to 14.7 mV/dec, as shown in Fig. 3(d). μ for T from 10 to 300 K was extracted at a fixed N and provided in Fig. 3(e). For T increases from 10 K to ~ 150 K, μ increases due to the reduced coulomb scattering [27], [28]. As already reported by some studies on the cryogenic mobility of UTBB transistors, higher level of interface traps will lead to a stronger dependency of μ on the coulomb scattering when the temperature decreases [28], [29], [30]. In addition, the devices used in this study are fabricated with higher channel doping concentration, which also leads to a stronger dependency of μ on the coulomb scattering. Therefore, the obvious decrease of μ as T reduces from 150 K should be attributed to the high channel doping level, the interface traps, and the neutral atoms. Whereas, for T higher than 150 K, the phonon scattering starts to

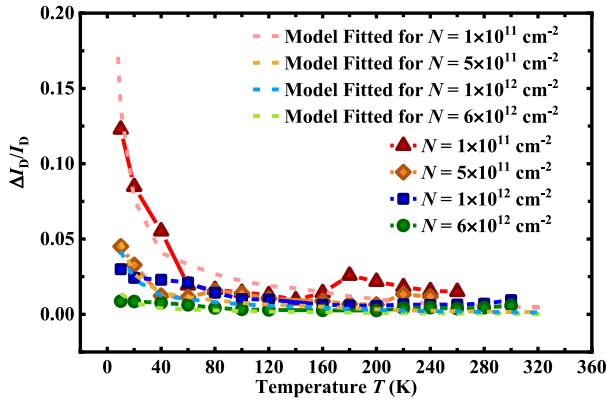


FIGURE 4. The change of $\Delta I_D/I_D$ as a function of T under various N . At a fixed V_D of 800 mV, the temperature dependence of $\Delta I_D/I_D$ was studied for N ranging from $1 \times 10^{11} \text{ cm}^{-2}$ to $6 \times 10^{12} \text{ cm}^{-2}$. Based on the unified temperature-dependent current fluctuation model described in (4) and (5), $\Delta I_D/I_D$ is fitted from sub-10 K to 320 K, as shown in the red dash line ($N = 1 \times 10^{11} \text{ cm}^{-2}$), yellow dash line ($N = 5 \times 10^{11} \text{ cm}^{-2}$), blue dash line ($N = 1 \times 10^{12} \text{ cm}^{-2}$) and green dash line ($N = 6 \times 10^{12} \text{ cm}^{-2}$).

dominate and it increases as T rises, resulting in the decrease in μ as T increases from 150 K to 300 K. Fig. 3(f) shows the extracted N at $V_G = 480$ mV and $V_D = 800$ mV as a function of T . Due to the increase in the Fermi potential, the bandgap widening, and the scaling of Fermi-Dirac occupation function [31], N decreases as T cools down to 10 K at the fixed V_G and V_D conditions.

With the extracted N and μ , the temperature dependency of $\Delta I_D/I_D$ is analyzed in Fig. 4. To ensure the devices are working at the same surface charge condition, in each split for comparison, $\Delta I_D/I_D$ has been plotted as a function of T at the fixed N and the same V_D . For moderate to strong inversion mode ($N \geq 10^{11} \text{ cm}^{-2}$) in Fig. 4, $\Delta I_D/I_D$ increases as T reduces from 300 K to 10 K. When T reduces below 100 K, $\Delta I_D/I_D$ increases rapidly for moderate inversion mode ($10^{11} \text{ cm}^{-2} \leq N \leq 10^{12} \text{ cm}^{-2}$), which may be probably due to the increase in α , according to (2). Moreover, in Fig. 4, it is also observed that $\Delta I_D/I_D$ at lower N is more severe than that at higher N , due to the stronger charge screening effect in the latter case.

C. TEMPERATURE DEPENDENCE OF SCATTERING COEFFICIENT

In Hung's model [23], it is typically understood that μ is closely related to T while α is a temperature-independent constant. To develop an accurate unified model for the I_D fluctuation from 10 to 300 K, the correlation of α and T is re-examined for each fixed N , as shown in Fig. 5(a). As T reduces from 300 K to 10 K, α increases by an order of magnitude. As α is the scattering coefficient due to the coulomb scattering, an increase in α suggests a stronger effect of coulomb scattering on the current fluctuation at LT. A linear relationship between α and T^{-1} for each fixed N can be obtained, which is consistent with the simplified 2-D electron gas model theoretically predicted by Sah et al. [32]. Here, α_0 is the fitting constant and shows an exponential

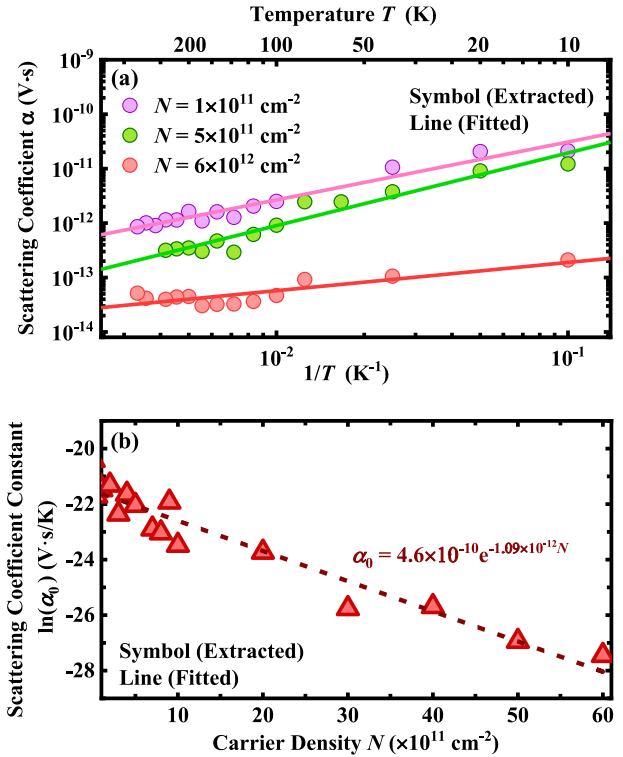


FIGURE 5. (a) The change of α as a function of T for different N . α is inversely proportional to T . (b) The value of $\ln(\alpha_0)$ and the fitting line as a function of N . The temperature-independent scattering coefficient constant α_0 is extracted from the linear relationship between α and T^{-1} .

relationship with N , as shown in Fig. 5(b). Since α_0 is temperature-independent, its value can be directly used to evaluate the current fluctuation as

$$\frac{\Delta I_D}{I_D} = \frac{-1}{W_G \times L_G} \left[\frac{1}{N(T)} - \alpha_0 T^{-1} \mu(T) \right] \quad (4)$$

and

$$\alpha_0 = \beta e^{\gamma N(T)} \quad (5)$$

where β and γ are the fitting constants.

Based on this modified model, $\Delta I_D/I_D$ is fitted from sub-10 K to 320 K, as shown in Fig. 4. The fitted trendline is in good agreement with the experimental data. Due to the impact of cryogenic quantum dots on the current fluctuation at very low V_D [10], [11], the model is mainly valid for transistors operated at high V_D cases. As the current fluctuation is closely related to the noise power spectrum density [12], [33], the unified temperature-dependent current fluctuation model, which was experimental validated from 10 K to 300 K, can be further developed to analyze the magnitude and bias dependence of the flicker noise for the LT circuit applications.

IV. CONCLUSION

In this work, the temperature dependence of I_D fluctuation was investigated for the 18 nm UTBB n-FETs, from 300 K down to 10 K. Enhanced I_D fluctuation was observed for n-FETs working at weak to moderate inversion mode at LT,

which needs to be optimized for the near-threshold LT circuit designs. Whereas, the higher carrier density at the strong inversion mode can still alleviate the I_D fluctuation due to the charge screening effect at LT. CVS model was exploited to accurately extract the scattering-related parameters used in the temperature dependent current fluctuation model. Based on these, a unified temperature-dependent I_D fluctuation model was developed and validated, which can be further used to estimate the noise characteristics in the LT circuit applications.

ACKNOWLEDGMENT

The authors would like to express their deep gratitude to Prof. Hanming Wu for his valuable discussion with the authors.

REFERENCES

- [1] E. Charbon et al., "Cryo-CMOS for quantum computing," in *IEEE Int. Electron Devices Meeting Tech. Dig.*, 2016, pp. 13.5.1–13.5.4, doi: [10.1109/IEDM.2016.7838410](https://doi.org/10.1109/IEDM.2016.7838410).
- [2] H. L. Chiang et al., "Cold CMOS as a power-performance-reliability booster for advanced FinFETs," in *Proc. IEEE Symp. VLSI Technol.*, 2020, pp. 1–2, doi: [10.1109/VLSITechnology18217.2020.9265065](https://doi.org/10.1109/VLSITechnology18217.2020.9265065).
- [3] Y. Liu, L. Lang, Y. Chang, Y. Shan, X. Chen, and Y. Dong, "Cryogenic characteristics of multianoscales field-effect transistors," *IEEE Trans. Electron Devices*, vol. 68, no. 2, pp. 456–463, Feb. 2021, doi: [10.1109/TEDE.2020.3041438](https://doi.org/10.1109/TEDE.2020.3041438).
- [4] C. Enz, A. Beckers, and F. Jazaeri, "Cryo-CMOS compact modeling," in *IEEE Int. Electron Devices Meeting Tech. Dig.*, 2020, pp. 25.3.1–25.3.4, doi: [10.1109/IEDM13553.2020.9371894](https://doi.org/10.1109/IEDM13553.2020.9371894).
- [5] D. J. Comer and D. T. Comer, "Operation of analog MOS circuits in the weak or moderate inversion region," *IEEE Trans. Educ.*, vol. 47, no. 4, pp. 430–435, Nov. 2004, doi: [10.1109/TE.2004.825537](https://doi.org/10.1109/TE.2004.825537).
- [6] J. Michl et al., "Evidence of tunneling driven random telegraph noise in cryo-CMOS," in *IEEE Int. Electron Devices Meeting Tech. Dig.*, 2021, pp. 31.3.1–31.3.4, doi: [10.1109/IEDM19574.2021.9720501](https://doi.org/10.1109/IEDM19574.2021.9720501).
- [7] Y. Sun, X. Li, B. Chen, and R. Cheng, "Phenomenon and mechanism investigation of the cryogenic random telegraph noise for 18 nm FDSOI CMOS," in *Proc. IEEE 16th Int. Conf. Solid-State Integr. Circuit Technol.*, 2022, pp. 1–3, doi: [10.1109/ICSICT55466.2022.9963364](https://doi.org/10.1109/ICSICT55466.2022.9963364).
- [8] B. C. Paz et al., "Variability evaluation of 28nm FD-SOI technology at cryogenic temperatures down to 100 mK for quantum computing," in *Proc. IEEE Symp. VLSI Technol.*, 2020, pp. 1–2, doi: [10.1109/VLSITechnology18217.2020.9265034](https://doi.org/10.1109/VLSITechnology18217.2020.9265034).
- [9] X. Zhan et al., "A dual-point technique for the entire I_D - V_G characterization into subthreshold region under random telegraph noise condition," *IEEE Electron Device Lett.*, vol. 40, no. 5, pp. 674–677, May 2019, doi: [10.1109/LED.2019.2903516](https://doi.org/10.1109/LED.2019.2903516).
- [10] H. Yang, M. Robitaille, X. Chen, H. Elgabra, L. Wei, and N. Y. Kim, "Random telegraph noise of a 28-nm cryogenic MOSFET in the coulomb blockade regime," *IEEE Electron Device Lett.*, vol. 43, no. 1, pp. 5–8, Jan. 2022, doi: [10.1109/led.2021.3132964](https://doi.org/10.1109/led.2021.3132964).
- [11] Z. Li et al., "Random telegraph noise from resonant tunnelling at low temperatures," *Sci. Rep.*, vol. 8, no. 1, p. 250, 2018, doi: [10.1038/s41598-017-18579-1](https://doi.org/10.1038/s41598-017-18579-1).
- [12] R. Asanovski et al., "Understanding the excess $1/f$ noise in MOSFETs at cryogenic temperatures," *IEEE Trans. Electron Devices*, vol. 70, no. 4, pp. 2135–2141, Apr. 2023, doi: [10.1109/TEDE.2022.3233551](https://doi.org/10.1109/TEDE.2022.3233551).
- [13] H. Oka et al., "Toward long-coherence-time Si spin qubit: The origin of low-frequency noise in cryo-CMOS," in *Proc. IEEE Symp. VLSI Technol.*, 2020, pp. 1–2, doi: [10.1109/VLSITechnology18217.2020.9265013](https://doi.org/10.1109/VLSITechnology18217.2020.9265013).
- [14] B. C. Paz et al., "Performance and low-frequency noise of 22-nm FDSOI down to 4.2 K for cryogenic applications," *IEEE Trans. Electron Devices*, vol. 67, no. 11, pp. 4563–4567, Nov. 2020, doi: [10.1109/TEDE.2020.3021999](https://doi.org/10.1109/TEDE.2020.3021999).
- [15] R. Wang et al., "Too noisy at the bottom?—Random telegraph noise (RTN) in advanced logic devices and circuits," in *IEEE Int. Electron Devices Meeting Tech. Dig.*, 2018, pp. 17.2.1–17.2.4, doi: [10.1109/IEDM.2018.8614594](https://doi.org/10.1109/IEDM.2018.8614594).
- [16] T. Gong et al., "Classification of three-level random telegraph noise and its application in accurate extraction of trap profiles in oxide-based resistive switching memory," *IEEE Electron Device Lett.*, vol. 39, no. 9, pp. 1302–1305, Sep. 2018, doi: [10.1109/LED.2018.2858245](https://doi.org/10.1109/LED.2018.2858245).
- [17] T. Shimizu et al., "Vth fluctuations due to random telegraph signal on work function control in Hf-doped silicate gate stack," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2009, pp. 389–394, doi: [10.1109/IRPS.2009.5173284](https://doi.org/10.1109/IRPS.2009.5173284).
- [18] J. Chen, Y. Nakasaki, and Y. Mitani, "Deep insight into process-induced pre-existing traps and PBTI stress-induced trap generations in high- κ gate dielectrics through systematic RTN characterizations and ab initio calculations," in *Proc. IEEE Symp. VLSI Technol.*, 2016, pp. 1–2, doi: [10.1109/VLSIT.2016.7573373](https://doi.org/10.1109/VLSIT.2016.7573373).
- [19] Y. Sun et al., "A universal temperature dependent carrier backscattering model for low temperature high performance CMOS applications," *IEEE Trans. Electron Devices*, vol. 71, no. 1, pp. 107–113, Jan. 2024, doi: [10.1109/TEDE.2023.3305963](https://doi.org/10.1109/TEDE.2023.3305963).
- [20] Y.-F. Cao, M. Arsalan, J. Liu, Y.-L. Jiang, and J. Wan, "A novel one-transistor active pixel sensor with in-situ photoelectron sensing in 22 nm FD-SOI technology," *IEEE Electron Device Lett.*, vol. 40, no. 5, pp. 738–741, May 2019, doi: [10.1109/LED.2019.2908632](https://doi.org/10.1109/LED.2019.2908632).
- [21] X. Li, Y. Sun, J. Wan, B. Chen, R. Cheng, and G. Han, "Machine learning method for accurate analysis of complicated low temperature random telegraph noise," in *Proc. IEEE Int. Conf. IC. Design Technol.*, 2022, pp. 20–23, doi: [10.1109/ICICDT56182.2022.9933107](https://doi.org/10.1109/ICICDT56182.2022.9933107).
- [22] H. Nakamura, N. Yasuda, K. Taniguchi, C. Hamaguchi, and A. Toriumi, "Existence of double-charged oxide traps in Submicron MOSFET's," *Jpn. J. Appl. Phys.*, vol. 28, no. 11, pp. 2057–2060, 1989, doi: [10.1143/JJAP.28.L2057](https://doi.org/10.1143/JJAP.28.L2057).
- [23] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Trans. Electron Devices*, vol. 37, no. 3, pp. 654–665, Mar. 1990, doi: [10.1109/16.47770](https://doi.org/10.1109/16.47770).
- [24] W. Chakraborty, K. Ni, J. Smith, A. Raychowdhury, and S. Datta, "An empirically validated virtual source FET model for deeply scaled cool CMOS," in *Proc. IEEE Int. Electron Devices Meeting*, 2019, pp. 39.4.1–39.4.4, doi: [10.1109/IEDM19573.2019.8993666](https://doi.org/10.1109/IEDM19573.2019.8993666).
- [25] G. Zhou, F. A. Mamun, J. Yang-Scharlotta, D. Vasileska, and I. S. Esqueda, "Cryogenic characterization and analysis of nanoscale SOI FETs using a virtual source model," *IEEE Trans. Electron Devices*, vol. 69, no. 3, pp. 1306–1312, Mar. 2022, doi: [10.1109/TEDE.2022.3142650](https://doi.org/10.1109/TEDE.2022.3142650).
- [26] "Virtual source model in nanoHUB." Accessed: Jun. 25, 2023. [Online]. Available: <https://nanohub.org/resources/vsm0d>
- [27] S. C. Sun and J. D. Plummer, "Electron mobility in inversion and accumulation layers on thermally oxidized silicon surfaces," *IEEE Trans. Electron Devices*, vol. 27, no. 8, pp. 1497–1508, Aug. 1980, doi: [10.1109/T-ED.1980.20063](https://doi.org/10.1109/T-ED.1980.20063).
- [28] H. C. Han et al., "In-depth cryogenic characterization of 22 nm FDSOI technology for quantum computation," in *Proc. Joint Int. EUROSIOI Workshop Int. Conf. Ultimate Integr. Silicon (EuroSOI-ULIS)*, 2021, pp. 1–4, doi: [10.1109/EuroSOI-ULIS53016.2021.9560181](https://doi.org/10.1109/EuroSOI-ULIS53016.2021.9560181).
- [29] F. A. Mamun, D. Vasileska, and I. S. Esqueda, "Impact of back-gate biasing on the transport properties of 22 nm FD-SOI MOSFETs at cryogenic temperatures," *IEEE Trans. Electron Devices*, vol. 69, no. 10, pp. 5417–5423, Oct. 2022, doi: [10.1109/TEDE.2022.3199328](https://doi.org/10.1109/TEDE.2022.3199328).
- [30] M. L. Vermeer, R. J. E. Huetting, L. Pirro, J. Hoentschel, and J. Schmitz, "Interface states characterization of UTB SOI MOSFETs from the subthreshold current," *IEEE Trans. Electron Devices*, vol. 68, no. 2, pp. 497–502, Feb. 2021, doi: [10.1109/TEDE.2020.3043223](https://doi.org/10.1109/TEDE.2020.3043223).
- [31] A. Beckers, F. Jazaeri, and C. Enz, "Cryogenic MOS transistor model," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3617–3625, Sep. 2018, doi: [10.1109/TEDE.2018.2854701](https://doi.org/10.1109/TEDE.2018.2854701).
- [32] C. T. Sah, T. H. Ning, and L. L. Tschoop, "The scattering of electrons by surface oxide charges and by lattice vibrations at the silicon-silicon dioxide interface," *Surface Sci.*, vol. 32, no. 3, pp. 561–575, 1972, doi: [10.1016/0039-6028\(72\)90183-5](https://doi.org/10.1016/0039-6028(72)90183-5).
- [33] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A physics-based MOSFET noise model for circuit simulators," *IEEE Trans. Electron Devices*, vol. 37, no. 5, pp. 1323–1333, May 1990, doi: [10.1109/16.108195](https://doi.org/10.1109/16.108195).