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Fully Vertical GaN-on-SiC p-i-n Diodes With BFOM of 2.89 GW/cm^2

JIALUN LI [1], RENQIANG ZHU [1,2] (Member, IEEE), KA MING WONG [1], AND KEI MAY LAU [3] (Life Fellow, IEEE)

1 Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong
2 Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, Shenzhen 518000, China
3 Division of Emerging Interdisciplinary Area, Hong Kong University of Science and Technology, Hong Kong

CORRESPONDING AUTHOR: K. M. LAU (e-mail: eekmlau@ust.hk)

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(Jialun Li and Renqiang Zhu contributed equally to this work.)

ABSTRACT This letter reports a high-performance fully-vertical GaN-on-SiC p-i-n diode enabled by a conductive n-AlGaN buffer. The buffer conductivity was optimized by tuning the Al composition. The diode presents an ultra-low specific ON-resistance of 0.25 mΩ·cm^2, a high current swing of 10^{11}, and a high breakdown voltage of 850 V with a 5-μm-thick drift layer, leading to a Baliga's figure of merit (BFOM) of 2.89 GW/cm^2. The diode performance at elevated temperatures and the OFF-state leakage mechanism are analyzed. The demonstrated fully-vertical GaN-on-SiC p-i-n diode with a conductive buffer reveals a simple way towards realizing high-performance fully-vertical GaN-on-SiC devices for high power applications.

INDEX TERMS Gallium nitride, fully-vertical, GaN-on-SiC, conductive buffer, p-i-n diode.

I. INTRODUCTION

GaN power devices have developed rapidly in the past decades. While extensive research effort brings the successful commercialization of lateral GaN HEMTs for sub-650 V applications [1], the development of vertical GaN power devices did not catch up with the pace, mainly hindered by the high cost and small size of GaN substrates. Therefore, it is necessary to develop vertical GaN power devices on cost-effective foreign substrates, i.e., sapphire, Si, and SiC for high power applications. Quasi-vertical GaN power devices have been demonstrated on these substrates [2], [3], [4], [5], [6], [7], but they typically suffer from current crowding, etching-induced sidewall leakage and non-optimal wafer area utilization [8]. Researchers used two substrate engineering techniques, namely flip-chip bonding and selective removal of substrate and buffer, to realize fully-vertical GaN-on-Si power devices [9], [10], [11], but their fabrication processes are somewhat complex. On the other hand, employing a conductive buffer between the substrate and GaN drift layer can greatly simplify the fabrication process. Fully-vertical GaN-on-Si power diodes have been realized with GaN/AlN strained layer superlattice (SLS) buffer [12], [13], [14]. Yet, the epitaxy thickness is limited by the large lattice and thermal mismatch between GaN and Si, and the device performance is limited by the high resistivity of the SLS buffer.

Compared to Si and sapphire, SiC substrate has the advantage of higher thermal conductivity, closer lattice-match with GaN and simpler to achieve fully-vertical structure. Using the GaN-on-SiC platform also allows monolithic integration of GaN and SiC devices [8]. In the 2000s, some researchers demonstrated fully-vertical GaN-on-SiC p-i-n diodes with conductive AlGaN buffer [15], [16], [17]. However, there is still plenty of room for performance improvement. Recently, fully-vertical GaN-on-SiC Schottky barrier diode with fluorine-implanted termination was demonstrated [8]. In this work, we present high-performance fully-vertical GaN-on-SiC p-i-n diodes with a relatively simple fabrication process. Grown on an optimized AlGaN buffer of high conductivity, the diode features a high current swing of 10^{11}, a high breakdown voltage (V_{BR}) of 850 V and an ultra-low specific ON-resistance ($R_{ON,sp}$) of 0.25 mΩ·cm^2, giving a superior Baliga's figure of merit (BFOM = $(V_{BR})^2/R_{ON,sp}$) of 2.89 GW/cm^2.

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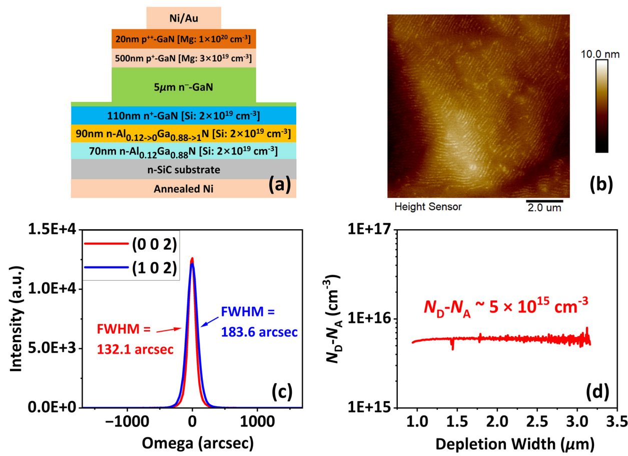

FIGURE 1. **(a) Cross-sectional schematic of fabricated fully vertical GaN-on-SiC p-i-n diodes. (b) AFM scan image of the as-grown sample. (c) XRD rocking curves of the as-grown sample. (d) Calculated net doping concentration in the drift layer from *C-V* measurement.**

II. EPITAXIAL GROWTH AND DEVICE FABRICATION

The p-i-n epitaxial structure for the diode was grown on n-type 4H-SiC substrates by metal–organic chemical vapor deposition (MOCVD), as shown in Fig. 1(a). The epilayers, from bottom to top, consist of a 70-nm n-$Al_{0.12}Ga_{0.88}N$ [Si: 2×10^{19} cm^{-3}], a 90-nm n-$Al_{0.12\text{->}0}Ga_{0.88\text{->}1}N$ [Si: 2×10^{19} cm^{-3}], a 110-nm n^+-GaN [Si: 2×10^{19} cm^{-3}], a 5-μm n^--GaN drift layer, a 500-nm p^+-GaN [Mg: 3×10^{19} cm^{-3}], and a 20-nm p^{++}-GaN [Mg: 1×10^{20} cm^{-3}] capping layer. The Al composition in the AlGaN buffer is calibrated by x-ray diffraction (XRD) measurements. Fig. 1(b) shows a 10 × 10 μm^2 atomic force microscope (AFM) scan of the as-grown sample, with a root-mean-square roughness of 1.27 nm. Fig. 1(c) shows the XRD rocking curves of the as-grown sample, with FWHM of (002) and (102) orientations values 132.1 arcsec and 183.6 arcsec, respectively. The threading dislocation density (TDD) is estimated to be 1.21 × 10^8 cm^{-2} based on empirical equations [18]. Fig. 1(d) shows the net carrier concentration in the drift layer obtained from room temperature *C-V* measurement at 1 MHz, which is as low as 5 × 10^{15} cm^{-3} [19].

The key to fabricating high-performance fully-vertical GaN-on-SiC power devices is to optimize the conductivity of the AlGaN buffer. Test structures with different Al compositions in the buffer were grown by MOCVD and fabricated to check for conductivity, as shown in Fig. 2. The highest buffer conductivity has been achieved with an Al composition of 0.12, and it was adopted for p-i-n diode epi-layer growth.

The diode fabrication process started with Cl_2/BCl_3-based dry etching of mesa (~5.5-μm deep) for device isolation [20], followed by hot tetramethylammonium hydroxide (TMAH) treatment to remove the etching damage and smoothen the etched surface. Then, 120 nm Ni was evaporated on the SiC substrate backside as cathode, followed by a rapid thermal annealing step at 950 °C in N_2 to form ohmic contact. The frontside is protected by a layer of plasma-enhanced chemical vapor deposition (PECVD) grown SiO_2 in this step [8]. Finally, Ni/Au was evaporated on the frontside and annealed as anode.

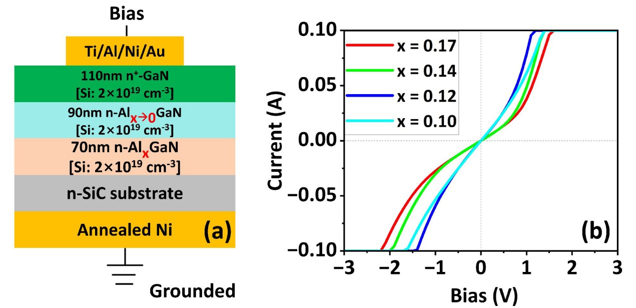

FIGURE 2. **(a) Schematic of the test structure for optimizing the buffer conductivity. (b) Vertical *I-V* characteristics of test structures with different Al compositions in AlGaN.**

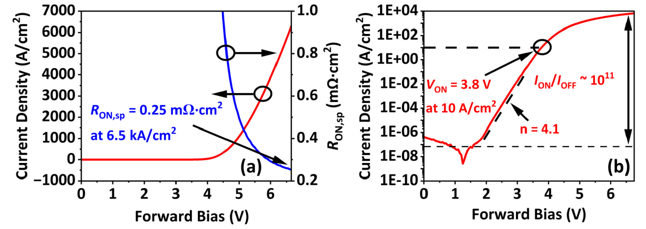

FIGURE 3. **Forward *J-V* characteristic of a representative diode in (a) linear scale and (b) semi-log scale.**

III. DEVICE RESULTS AND DISCUSSION

Fig. 3(a) plots the forward current density versus voltage (*J-V*) characteristics and $R_{ON,sp}$ of a representative device in linear scale. The diode has a mesa diameter of 60-μm and an anode diameter of 44-μm. $R_{ON,sp}$ is as low as 0.25 mΩ·cm^2 at 6.5 kA/cm^2. Fig. 3(b) plots the forward *J-V* characteristics in semi-log scale, showing a high current swing of 10^{11}. The ideality factor is extracted to be 4.1, and the turn-on voltage (V_{ON}) defined at 10 A/cm^2 is 3.8 V. The ideality factor and V_{ON} are somewhat higher than those of vertical GaN p-i-n diodes without current conducting through an as-grown buffer–substrate heterojunction [10], [19], [21], [22]. This can be attributed to the large conduction band offset at the AlGaN/SiC heterojunction interface, deep-level assisted tunneling, non-ideal p-GaN ohmic contact and enhanced recombination process associated with dry etching damage [8], [15], [23], [24], [25].

Fig. 4 shows the forward *J-V* characteristics at elevated temperatures up to 175 °C in linear and semi-log scale. At high injection, the increase of $R_{ON,sp}$ with higher temperature can be explained by reduction in electron mobility in the drift layer associated with enhanced phonon scattering [26]. The current before turn-on remains low at high temperatures, maintaining a stable current swing of 10^{11}. V_{ON} and ideality factor are also extracted as a function of temperature. The decrease in V_{ON} and ideality factor as temperature increases

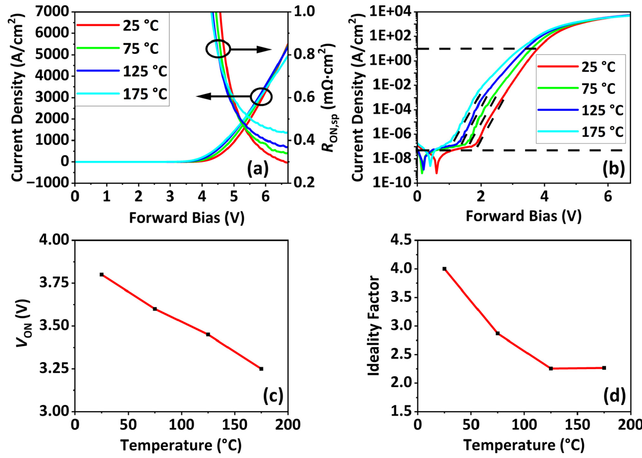

FIGURE 4. Forward *J-V* characteristic of a representative diode at elevated temperatures in (a) linear scale and (b) semi-log scale. Extracted (c) V_{ON} and (d) ideality factor at elevated temperatures.

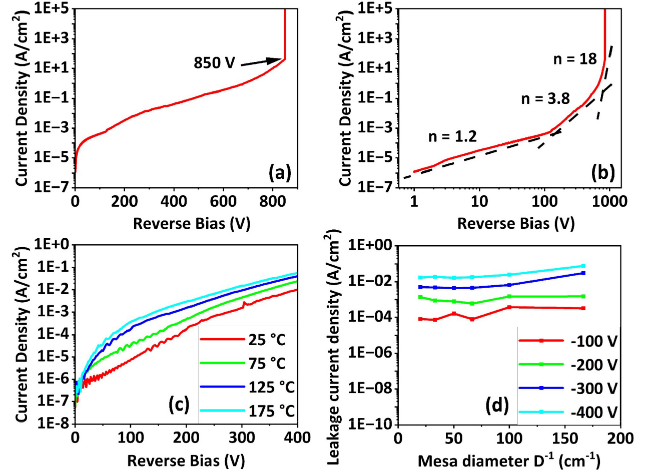

FIGURE 5. Reverse *J-V* characteristic of a representative diode in (a) semi-log scale (b) log scale. (c) Reverse *J-V* characteristics up to -400 V at elevated temperatures. (d) Leakage current density of diodes with different mesa diameter *D* (D = 60, 100, 150, 200, 300 and 500-μm), as a function of $1/D$ at reverse bias of 100, 200, 300 and 400 V.

can be attributed to bandgap narrowing, thermally-enhanced carrier diffusion, improved p-GaN metal contact and increase of thermally generated carriers [3], [8], [10], [25].

Fig. 5(a) shows the reverse *J-V* characteristics of a representative diode in semi-log scale, presenting a hard breakdown voltage of 850 V. The breakdown voltage can be further improved by employing advanced edge termination techniques such as field plates [3]. The reverse *J-V* characteristics in Fig. 5(a) is plotted in log scale in Fig. 5(b), clearly showing linear dependence and two changes in slope at −133 V and −683 V, indicating the coexistence of acceptor and donor traps. The acceptor and donor trap density are estimated to be 3.68×10^{16} cm^{-3} and 2.97×10^{16} cm^{-3} from the two traps-filled-limited voltages [27]. With J proportional to V^n, the reverse leakage current can be modeled by trap-assisted space-charge-limited current (SCLC) conduction, with n fitted to be 1.2, 3.8 and 18 in the three regions [28].

Fig. 5(c) shows the reverse *J-V* characteristics up to −400 V at elevated temperatures. The leakage current at −400 V increases less than one order of magnitude from 25 °C to 175 °C. From the Arrhenius plot of ln(J) - 1/T at −400 V, the thermal activation energy is extracted to be 132 meV, suggesting the existence of deep hopping centers [9], [29]. Reverse *J-V* characteristics of diodes with different mesa diameters are also tested and shown in Fig. 5(d). The leakage current density has little dependence on the diode mesa perimeter, indicating that the sidewall leakage current is insignificant, and the bulk component is the main contributor to the total leakage current [30].

Finally, in Fig. 6, the p-i-n diode in this work is benchmarked with state-of-the-art quasi- and fully-vertical GaN p-i-n diodes on foreign substrates and bulk GaN substrates in terms of $R_{ON,sp}$ versus V_{BR}. The high BFOM of 2.89 GW/cm^2 is superior to the reported vertical GaN p-i-n diodes on foreign substrates. The performance can be further improved by optimizing the AlGaN buffer to reduce

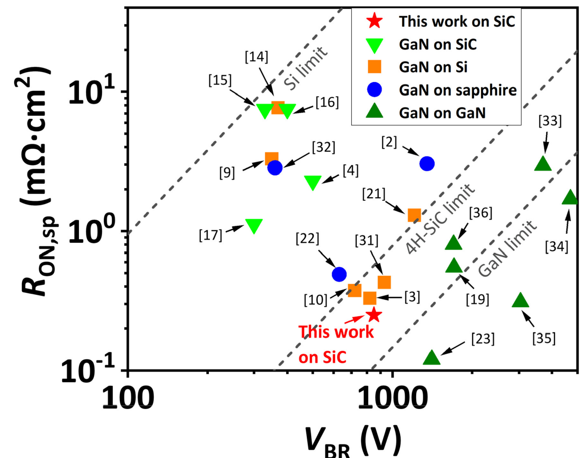

FIGURE 6. $R_{ON,sp}$ versus V_{BR} benchmarking of the diode in this work against reported state-of-the-art vertical GaN p-i-n diodes.

the buffer-substrate heterojunction resistance and growing a thicker drift layer. The demonstrated high-performance fully-vertical GaN-on-SiC p-i-n diode with simple fabrication process is promising for high-power applications and paves a simple way towards realizing high-performance fully-vertical GaN-on-SiC power devices.

IV. CONCLUSION

In this work, we demonstrate a fully-vertical GaN-on-SiC p-i-n diode with an optimized AlGaN buffer, simple fabrication process and record performance. The device performance at elevated temperatures and reverse leakage mechanism are analyzed. The high performance, including high-current capability, ultra-low $R_{ON,sp}$, high current swing and high breakdown voltage are promising for power electronics and demonstrates the huge potential of direct epitaxially-grown vertical GaN-on-SiC power devices.

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REFERENCES

[1] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016, doi: 10.1109/JESTPE.2016.2582685.

[2] S. E. Harrison, Q. Shao, C. D. Frye, L. F. Voss, and R. J. Nikolic, "1.1 kV vertical p-i-n GaN-on-sapphire diodes," in *Proc. 76th Device Res. Conf. (DRC)*, 2018, pp. 1–2, doi: 10.1109/DRC.2018.8442240.

[3] R. Abdul Khadar, C. Liu, L. Zhang, P. Xiang, K. Cheng, and E. Matioli, "820-V GaN-on-Si quasi-vertical p-i-n diodes with BFOM of 2.0 GW/cm^2," *IEEE Electron Device Lett.*, vol. 39, no. 3, pp. 401–404, Mar. 2018, doi: 10.1109/LED.2018.2793669.

[4] J. B. Limb, D. Yoo, J.-H. Ryou, S. C. Shen, and R. D. Dupuis, "Low on-resistance GaN pin rectifiers grown on 6H-SiC substrates," *Electron. Lett.*, vol. 43, no. 6, pp. 366–367, 2007, doi: 10.1049/el:20070065.

[5] R. Zhu, H. Jiang, C. W. Tang, and K. M. Lau, "Enhancing ON- and OFF- state performance of quasi-vertical GaN trench MOSFETs on sapphire with reduced interface charges and a thick bottom dielectric," *IEEE Electron Device Lett.*, vol. 43, no. 3, pp. 346–349, Mar. 2022, doi: 10.1109/LED.2022.3146276.

[6] R. Zhu, H. Jiang, C. W. Tang, and K. M. Lau, "GaN quasi-vertical trench MOSFETs grown on Si substrate with ON-current exceeding 1 A," *Appl. Phys. Exp.*, vol. 15, no. 12, Nov. 2022, Art. no. 121004, doi: 10.35848/1882-0786/aca26e.

[7] P. Gribisch, R. D. Carrascon, V. Darakchieva, and E. Lind, "Tuning of quasi-vertical GaN FinFETs fabricated on SiC substrates," *IEEE Trans. Electron Devices*, vol. 70, no. 5, pp. 2408–2414, May 2023, doi: 10.1109/TED.2023.3263154.

[8] Y. Li, S. Yang, K. Liu, K. Cheng, K. Sheng, and B. Shen, "Fully-vertical GaN-on-SiC schottky barrier diode: Role of conductive buffer structure," *IEEE Trans. Electron Devices*, vol. 70, no. 2, pp. 619–626, Feb. 2023, doi: 10.1109/TED.2022.3227227.

[9] X. Zou, X. Zhang, X. Lu, C. W. Tang, and K. M. Lau, "Fully vertical GaN p-i-n diodes using GaN-on-Si epilayers," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 636–639, May 2016, doi: 10.1109/LED.2016.2548488.

[10] Y. Zhang, M. Yuan, N. Chowdhury, K. Cheng, and T. Palacios, "720-V/0.35-mΩ·cm^2 fully vertical GaN-on-Si power diodes by selective removal of Si substrates and buffer layers," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 715–718, May 2018, doi: 10.1109/LED.2018.2819642.

[11] R. A. Khadar, C. Liu, R. Soleimanzadeh, and E. Matioli, "Fully vertical GaN-on-Si power MOSFETs," *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 443–446, Mar. 2019, doi: 10.1109/LED.2019.2894177.

[12] S. Mase, Y. Urayama, T. Hamada, J. J. Freedsman, and T. Egawa, "Novel fully vertical GaN p–n diode on Si substrate grown by metalorganic chemical vapor deposition," *Appl. Phys. Exp.*, vol. 9, no. 11, Oct. 2016, Art. no. 111005, doi: 10.7567/APEX.9.111005.

[13] K. Zhang, S. Mase, K. Nakamura, T. Hamada, and T. Egawa, "Demonstration of fully vertical GaN-on-Si Schottky diode," *Electron. Lett.*, vol. 53, no. 24, pp. 1610–1611, Nov. 2017, doi: 10.1049/EL.2017.3166.

[14] S. Mase, T. Hamada, J. J. Freedsman, and T. Egawa, "Effect of drift layer on the breakdown voltage of fully-vertical GaN-on-Si p-n diodes," *IEEE Electron Device Lett.*, vol. 38, no. 12, pp. 1720–1723, Dec. 2017, doi: 10.1109/LED.2017.2765340.

[15] D. Yoo, J. Limb, J.-H. Ryou, W. Lee, and R. D. Dupuis, "GaN full-vertical p-i-n rectifiers employing AlGaN:Si conducting buffer layers on n-SiC substrates," *Appl. Phys. Lett.*, vol. 88, no. 19, May 2006, Art. no. 193503, doi: 10.1063/1.2201554.

[16] D. Yoo, J. B. Limb, J.-H. Ryou, W. Lee, and R. D. Dupuis, "Epitaxial growth and device design optimization of full-vertical GaN p-i-n rectifiers," *J. Electron. Mater.*, vol. 36, no. 4, pp. 353–358, Feb. 2007, doi: 10.1007/s11664-006-0069-1.

[17] A. Nishikawa, K. Kumakura, and T. Makimoto, "Low on-resistance of GaN p-i-n vertical conducting diodes grown on 4H-SiC substrates," *Phys. Status Solidi C*, vol. 4, no. 7, pp. 2662–2665, Jun. 2007, doi: 10.1002/pssc.200674713.

[18] M. A. Moram and M. E. Vickers, "X-ray diffraction of III-nitrides," *Rep. Prog. Phys.*, vol. 72, no. 3, Dec. 2008, Art. no. 36502, doi: 10.1088/0034-4885/72/3/036502.

[19] K. Nomoto et al., "1.7-kV and 0.55-mΩ·cm^2 GaN p–n diodes on bulk GaN substrates with avalanche capability," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 161–164, Feb. 2016, doi: 10.1109/LED.2015.2506638.

[20] H. Fukushima et al., "Vertical GaN p–n diode with deeply etched mesa and the capability of avalanche breakdown," *Appl. Phys. Exp.*, vol. 12, no. 2, Feb. 2019, Art. no. 026502, doi: 10.7567/1882-0786/aafdb9.

[21] X. Guo et al., "1200-V GaN-on-Si quasi-vertical p-n diodes," *IEEE Electron Device Lett.*, vol. 43, no. 12, pp. 2057–2060, Dec. 2022, doi: 10.1109/LED.2022.3219103.

[22] B. S. Zheng et al.,"Suppression of current leakage along mesa surfaces in GaN-based p-i-n diodes," *IEEE Electron Device Lett.*, vol. 36, no. 9, pp. 932–934, Sep. 2015, doi: 10.1109/LED.2015.2458899.

[23] Z. Hu et al., "Near unity ideality factor and Shockley-Read-Hall lifetime in GaN-on-GaN p-n diodes with avalanche breakdown," *Appl. Phys. Lett.*, vol. 107, no. 24, 2015, Art. no. 243501, doi: 10.1063/1.4937436.

[24] X. Zhang, X. Zou, X. Lu, C. W. Tang, and K. M. Lau, "Fully- and quasi-vertical GaN-on-Si p-i-n diodes: High performance and comprehensive comparison," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 809–815, Mar. 2017, doi: 10.1109/TED.2017.2647990.

[25] J. M. Shah, Y.-L. Li, T. Gessmann, and E. F. Schubert, "Experimental analysis and theoretical model for anomalously high ideality factors (n>>2.0) in AlGaN/GaN p-n junction diodes," *J. Appl. Phys.*, vol. 94, no. 4, pp. 2627–2630, Jul. 2003, doi: 10.1063/1.1593218.

[26] I. C. Kizilyalli, A. P. Edwards, O. Aktas, T. Prunty, and D. Bour, "Vertical power p-n diodes based on bulk GaN," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 414–422, Feb. 2015, doi: 10.1109/TED.2014.2360861.

[27] C. Zhou, Q. Jiang, S. Huang, and K. J. Chen, "Vertical leakage/breakdown mechanisms in AlGaN/GaN-on-Si devices," *IEEE Electron Device Lett.*, vol. 33, no. 8, pp. 1132–1134, Aug. 2012. doi: 10.1109/LED.2012.2200874.

[28] Y. Zhang et al., "Design space and origin of off-state leakage in GaN vertical power diodes," in *Proc. Int. Electron Devices Meeting (IEDM)*, 2015, pp. 35.1.1–35.1.4, doi: 10.1109/IEDM.2015.7409830.

[29] Q. Shan et al., "Transport-mechanism analysis of the reverse leakage current in GaInN light-emitting diodes," *Appl. Phys. Lett.*, vol. 99, no. 25, Dec. 2011, Art. no. 253506, doi: 10.1063/1.3668104.

[30] Y. Zhang et al., "Origin and control of OFF-state leakage current in GaN-on-Si vertical diodes," *IEEE Trans. Electron Devices*, vol. 62, no. 7, pp. 2155–2161, Jul. 2015, doi: 10.1109/TED.2015.2426711.

[31] F. Jia et al., "930V and low-leakage current GaN-on-Si quasi-vertical PiN diode with beveled-sidewall treated by self-aligned fluorine plasma," *IEEE Electron Device Lett.*, vol. 43, no. 9, pp. 1400–1403, Sep. 2022, doi: 10.1109/LED.2022.3195263.

[32] W. Liu et al., "Avalanche ruggedness of GaN p-i-n diodes grown on sapphire substrate," *Phys. Status Solidi A*, vol. 215, no. 18, Jun. 2018, Art. no. 1800069, doi: 10.1002/PSSA.201800069.

[33] I. C. Kizilyalli, A. P. Edwards, H. Nie, D. Bour, T. Prunty, and D. Disney, "3.7 kV vertical GaN PN diodes," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 247–249, Feb. 2014, doi: 10.1109/LED.2013.2294175.

[34] H. Ohta et al., "Vertical GaN p-n junction diodes with high breakdown voltages over 4 kV," *IEEE Electron Device Lett.*, vol. 36, no. 11, pp. 1180–1182, Nov. 2015, doi: 10.1109/LED.2015.2478907.

[35] S.-W. H. Chen et al., "Vertical GaN-on-GaN PIN diodes fabricated on free-standing GaN wafer using an ammonothermal method," *J. Alloys Compd.*, vol. 804, pp. 435–440, Oct. 2019, doi: 10.1016/j.jallcom.2019.07.021.

[36] M. Xiao et al., "Robust avalanche in 1.7 kV vertical GaN diodes with a single-implant bevel edge termination," *IEEE Electron Device Lett.*, vol. 44, no. 10, pp. 1616–1619, Oct. 2023, doi: 10.1109/LED.2023.3302312.