Effect of Buffer Charge Redistribution on RF Losses and Harmonic Distortion in GaN-on-Si Substrates

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ABSTRACT Understanding and mitigation of substrate RF losses and signal distortion are critical to enable high-performance GaN-on-Si front-end-modules. While the origin of RF losses and consequently a decreased effective substrate resistivity (ρ_{eff}) in GaN-on-Si substrates is now understood to be diffusion of Al and Ga atoms into the silicon substrate during III-N growth, the effect of upper III-N buffer layers on the ρ_{eff} degradation under stressed conditions remains unclear. In this paper, we show that up to 50% variation in ρ_{eff} at 2 GHz can take place over more than 1,000 s when the substrate is stressed at 50 V. Additionally, Coplanar Wave Guide (CPW) large-signal measurements under the same experimental conditions show a variation of 2nd harmonic power of up to 5dB. A thermally activated stress and relaxation behavior shows the signature of traps which are present in the C-doped layers. With the help of a simplified TCAD model of the GaN-on-Si stack, we link this behavior to slow charge redistribution in the C-doped buffer continuously modifying the flat-band voltage (V_{FB}) of the Metal-Insulator-Semiconductor (MIS) structure. Free carrier transport across the buffer is shown to have the greatest contribution on the large time constants, highlighting the importance of vertical transport paths in GaN-on-Si stacks.

INDEX TERMS C-doped buffer layer, effective resistivity, GaN-on-Si substrate, harmonics distortion, RF characterization, traps.

I. INTRODUCTION

INTEGRATION of GaN HEMTs on Si substrate is a promising way to enable RF front-end-modules with high power handling for 5G and beyond [1]. The large breakdown field and saturation velocity of GaN offer high saturation power and efficiency for mm-wave power amplifiers (PA). While GaN is typically grown on SiC substrate, GaN-on-Si devices enable the use of large-scale, low-cost Si wafer and potential co-integration with CMOS technology [2]. However, the use of a lossy Si substrate can lead to substrate-induced RF losses and signal distortion [3].

For GaN-on-high resistivity (HR) Si wafer, it is commonly accepted that RF losses are dominated by a parasitic surface conduction (PSC) layer which forms close to Si top surface [4], [5], [6], [7]. The PSC layer is mainly formed by diffusion of Al and Ga atoms into the first 1-2 micrometres of the Si substrate during high thermal budget epitaxy of the III-N layers. Such a layer can then capacitively couple to the overlying circuitry through the semi-insulating buffer layers, and reduce the effective resistivity of the substrate (ρ_{eff}) to well below the nominal resistivity of the HR Si wafer [8]. A lower ρ_{eff} can lead to increased crosstalk and harmonic distortion (HD) [3], [9]. As demonstrated in [6], [7], by carefully engineering the III-N buffer and AlN nucleation layers, it is possible to recover high values of ρ_{eff} with low levels of distortion, comparable to state-of-the art "trap-rich" Silicon-on-Insulator (SOI) substrates [10].

GaN-on-Si stacks typically contain one or multiple layers of $Al_xGa_{1-x}N$ with moderate to high C or Fe doping levels to increase their resistivity and increase blocking voltage. The inclusion of those dopants, acting as deep traps in the buffer, is also responsible for the degradation of the HEMT on-resistance (R_{ON}) when the device is subjected to prolonged drain bias stress [11]. The mechanisms responsible for this current collapse have been extensively studied in recent years [12], [13]. Buffer traps can also impact substrate-related RF figures-of-merit such as ρ_{eff}. Significant hysteresis in the evolution of ρ_{eff} with backside chuck bias has been linked to charge (de-)trapping in the upper buffer layers [14]. This renders the prediction of HD by inspection of $\rho_{eff}(V)$ curves difficult. Furthermore, degradation of ρ_{eff} can occur when the substrate is stressed, and recovery times can exceed 1,000 s, owing to charge redistribution mechanisms in the buffer [15].

In this paper, we extend our previous work [15] and analyse in detail the interplay between buffer charge redistribution and time dependence of ρ_{eff} during chuck bias stress transient. For the first time, we show that HD is also time dependent, highlighting a potential additional reliability concern for highly-resistive GaN-on-Si stacks. With help of TCAD simulations, we discuss the influence of different process parameters on the transient response. The paper is structured as follows. After describing the measured and simulated samples in Section II, experimental response of ρ_{eff} and HD to a backside (chuck) bias stress in high-performance GaN-on-Si substrates are shown (Section III). In Section IV, general theoretical considerations are given for generic Metal-Insulator-Semiconductor (MIS) structures with non-trivial charge distributions. Section V provides TCAD simulations of 1D and 2D structures, reproducing experimental features as well as predicting the impact of buffer thickness and buffer transport mechanisms. Guidelines for reducing the time-dependence of ρ_{eff} are also proposed.

II. EXPERIMENTAL DETAILS
A. SUBSTRATE FABRICATION AND PROCESSING
III-N stacks in this work were grown using a Veeco Turbodisc Maxbright MOCVD reactor on 200 mm-diameter, 3-6 kΩ·cm CZ-Si (111) wafers. They comprise an AlN nucleation layer (~175 nm), followed by a ~1.2 μm-thick carbon-doped AlGaN/AlNsuperlattice buffer, a 1 μm-thick carbon-doped GaN buffer, and finally a ~300 nm unintentionally doped (UID) GaNlayer (see Fig. 1). The growth was stopped before the nitride barrier layer on top of GaN UID layer (channel in HEMTs) to avoid 2DEG channel formation.

Following III-N growth, one wafer underwent nitrogen isolation implant [16] (sample B) while another wafer was kept un-implanted (sample A). On HEMT stacks with top barrier, the implant creates a high concentration of defects, suppressing the 2DEG for DC isolation. The implant consists of 3 steps of increasing energy (75, 150 and 375 keV). It is suggested by TRIM simulations that N-induced defects are not found at depth greater than ~600 nm from channel
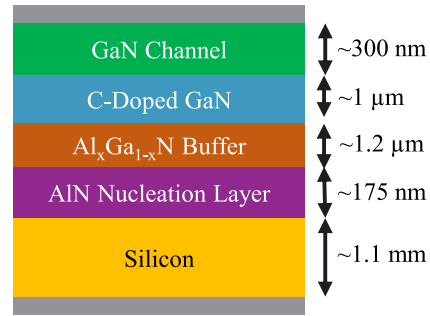
FIGURE 1. Cross-sectional schematic of the studied and simulated GaN-on-Si stack. Electrodes are represented schematically in gray.
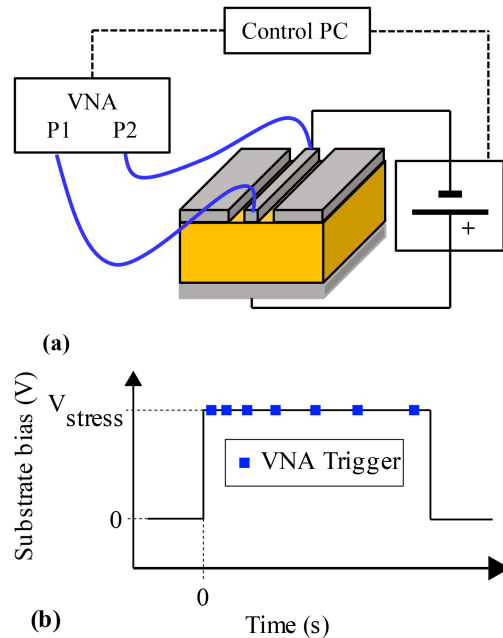
FIGURE 2. (a) Experimental setup for the small-signal CPW stress measurements. For time-dependent HD measurements, a power amplifier and RF filters are added between VNA P1 and the CPW line. (b) Schematic of the measurement sequence. After substrate DC bias has been stepped to +50 V or −50 V, successive RF measurements (represented by squares) are taken on the CPW line. The relaxation phase is also represented.

surface [7], [14]. Consequently, the Si substrate is most probably not reached by the isolation implant.

2 mm-long CPW lines (central conductor width W = 85 μm, slot width S = 50 μm) were patterned on both samples using e-beam evaporation of a ~1 μm-thick Ti/Au stack.

B. MEASUREMENT TECHNIQUES
On-wafer S-parameters measurements were carried out under dark conditions on a temperature-controlled chuck with a pair of GSG |Z| probes. To track the time evolution of ρ_{eff} in response to a chuck bias step, a custom setup was developed (see Fig. 2a). Chuck bias and VNA trigger are synchronized by the controller PC, which also tracks stress and relaxation time. Logarithmically spaced time delays are imposed between each RF measurement, represented by the blue squares in Fig. 2b. The time resolution and smallest

time step of this setup is of ∼100 ms, corresponding to the sum of PC-VNA communication, VNA acquisition and VNA saving times. DC bias ramp time is shorter than 1 ms. Only 11 frequency points are measured around a frequency f_0= 2 GHz to reduce the VNA acquisition time associated with a full frequency sweep.

A separate setup was then constructed to evaluate the drift of HD over time [3]. HD was measured using a fundamental tone of f_0 = 900 MHz. Again, to improve time resolution down to 1 s, only 5 points of the input power sweep were used, centred around P_{in} = 15 dBm. Second (H2) and third (H3) harmonic power are measured at the end of the CPW line. In order to correct for the varying RF loss along the line, H2 and H3 are interpolated at an output first harmonic power (the fundamental H1) of 15 dBm which is a commonly used power level for reporting substrate-induced distortion [7], [10]. The noise floor of the HD setup is ∼−110 dBm.

After each stress sequence, a 10,000 s relaxation ensured a return to equilibrium conditions before the next stress experiment or temperature change.

C. SIMULATION FRAMEWORK

A 1-D GaN-on-Si stack was implemented in Silvaco Atlas TCAD to better understand the charge redistribution mechanisms at play [15]. It consists in a simplified 4-layer representation of the GaN-on-Si buffer (see Fig. 1). Carbon doping is modelled as a dominant acceptor trap level ($E_t = E_v + 0.9$ eV), compensated by a shallow donor level (compensation ratio: 50%) [17]. Density is set to 10^{19}cm^{-3} and capture cross section to 10^{-13} cm^2. Drift-diffusion transport and Shockley-Read-Hall (SRH) models are used in these simulations.

In the C-doped GaN region, a Poole-Frenkel mobility model is included to obtain a good fit to the experimental data (see also Section V for more details). For electric field levels of ∼2×10^5V/cm (comparable with what is expected in the stacks considered here), the Poole-Frenkel transport mechanism has been found to accurately describe transport through defects in C-doped GaN [18], [19], [20]. Surface p-type doping is included in Si according to SRP data to reproduce the PSC layer. A background doping of 10^{16} cm^{-3} is used for GaN. For simplicity, no additional interface charge is considered.

III. RESULTS
A. SMALL-SIGNAL TIME DEPENDENCE

Fig. 3 shows the chuck bias stress experiments for the considered GaN-on-Si stacks. To remove the effect from decreasing ρ_{eff} with temperature, data is normalized to the second measured point. In contrast with our previous work [15], we choose to focus on the stress phase rather than the relaxation phase. Indeed, it is easier to ensure a same equilibrium initial state at each temperature for the stress phase, after having allowed a very long relaxation time from the previous experiment.
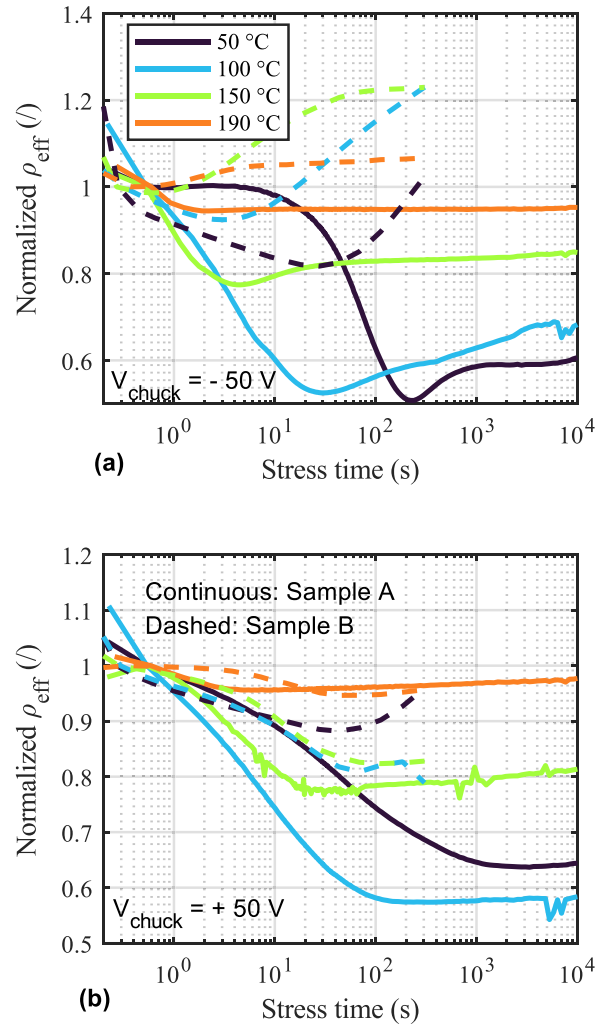
FIGURE 3. Experimental stress sequences for the GaN-on-Si substrates considered here, for chuck temperature ranging from 50 °C to 190 °C: (a) V_{chuck} = −50 V and (b) V_{chuck} = +50 V. The data is normalized to the 2nd measured point to remove the absolute decrease of ρ_{eff} with temperature (see [15]).

A.1. SAMPLE A (UN-IMPLANTED)

At 50 °C, the un-implanted GaN-on-Si substrate shows a ρ_{eff} of ∼ 1.2 kΩ·cm at 0 V. From Fig. 3 the following experimental observations can be made:

- Time to steady-state for both bias conditions exceeds 1,000 s at the lowest considered temperature of 50 °C;
- At temperatures of 50 and 100 °C, ρ_{eff} changes by a factor of 2 over the stress phase;
- Steady-state is reached at shorter periods of time as temperature increases;
- Relative variations of ρ_{eff} are smaller at higher temperatures.

An Arrhenius dependence is obtained for the experimental time constants, as previously shown in [15]. The activation energies corresponding to the thermally activated mechanisms are 0.57 eV and 0.44 eV for the stress biases of V_{chuck}= +50 V and V_{chuck} = −50 V, respectively. Those values, while in range with energies often found in GaN

devices by other means [13], [15], [21], are different from the 0.9 eV typically reported for C traps at low doping levels. Such barrier reduction has been observed and could be linked to Poole-Frenkel conduction [22].

A dip in ρ_{eff} is observed for the stress curves at -50 V. We speculate that this is related to a temporary depletion of the PSC layer leading to relatively low conductivity. For the $+50$ V condition, the absence of dip indicates no inversion of polarity over the course of the experiment.

It should be noted that no measurable DC current was observed for the entirety of the stress/relaxation sequence, i.e., there is no leakage at the AlN/Si interface.

A.2. SAMPLE B (IMPLANTED)

At 50°C, the implanted GaN-on-Si substrate shows a ρ_{eff} of ~ 1.0 kΩ·cm at 0 V. Although the isolation implant slightly degrades ρ_{eff}, such a highly-resistive substrate can still be considered quasi-lossless and is well suited for high-quality passives integration [7]. For this sample, time-dependent effects were more limited: less than 20% variation of ρ_{eff} is observed during the stress phase. The high density of defects induced by the N implant leads to strong Fermi level pinning in the buffer and furthermore additional buffer charge lowering the ρ_{eff} [7]. When ρ_{eff} decreases, the conductivity of the PSC layer increases and thus reduces its sensitivity to buffer charge change (see Section-IV.C).

Consequently, all subsequent analysis will focus on the un-implanted sample A. Indeed, while it seems that passive structures lying on implanted regions (sample B) will be protected from the time-dependence of ρ_{eff}, active devices will lie on top of MIS structures similar to sample A. A degradation of ρ_{eff} over time of this MIS stack could affect switch distortion or power amplifier efficiency [23], [24].

B. LARGE-SIGNAL TIME DEPENDENCE

Fig. 4 shows the experimental variation of H2 and H3 during chuck bias stress sequences for the selected temperatures of 50°C and 150°C in sample A. Experimental conditions are identical to those in Fig. 3. In all experiments, H2 dominated H3 by more than 20 dB, which is expected for substrate-induced HD [10].

At 50°C, H2 values are below -75 dBm for the bias conditions explored here, proving the technological relevance of an optimized GaN-on-Si technology compared with RF SOI [3].

Over the considered stress time of 10,000 s, a time dependence of H2 is observed. Similar to ρ_{eff}, H2 only reaches steady-state after more than 1,000 s for both bias conditions. Although variations in H2 over that period are limited to 5 dB, these results highlight an additional reliability concern for substrates subjected to prolonged bias stress. Because H3 is low and close to the equipment noise floor, time dependence can only be seen at $+50$ V and 50 °C, where a $\sim$5dB increase is observed. Section V provides more discussion and qualitative understanding of large-signal results.
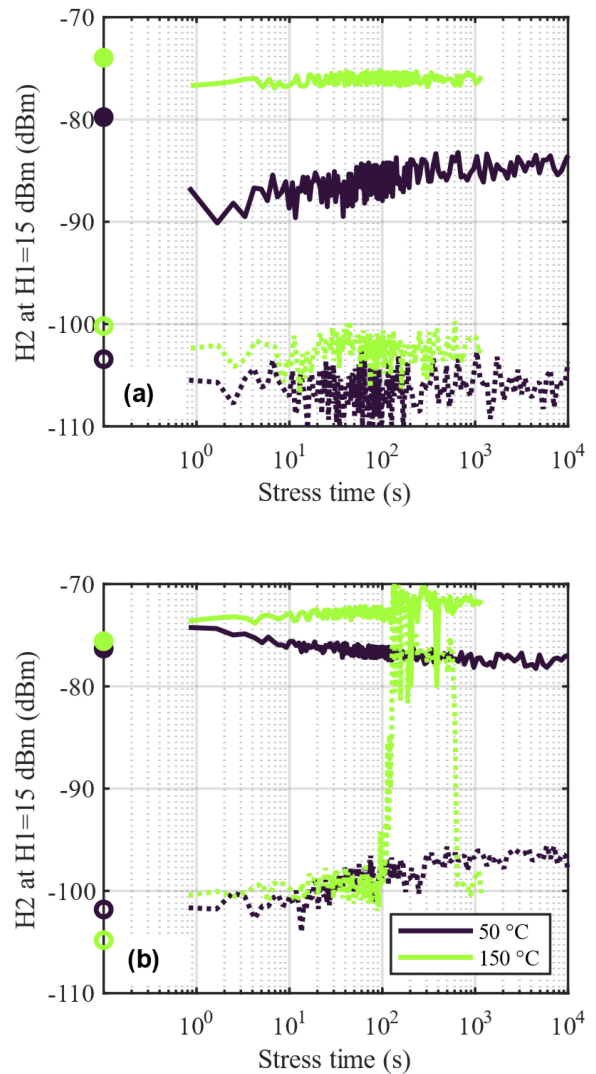
FIGURE 4. Experimental variation of 2nd (continuous) and 3rd (dotted) harmonic power at the output of 2 mm-long CPW lines of sample A while stressing the chuck at (a) -50 V and (b) +50 V. Because measurement acquisition time is larger for HD measurement compared with S-parameters, the experimental time resolution is only of ~1 s. Symbols indicate the pre-stress measurement.

At 150 °C, HD degrades as expected compared with 50 °C, mostly due to the increase of the intrinsic free carriers number in Si [7]. The time dependence cannot clearly be separated from the measurement noise. Also, the larger minimal time step in the HD setup complicates observation of variations occurring over less than 10 s. Such variations can be expected from ρ_{eff} changes in Fig. 3 and the difference between pre-stress HD (symbols in Fig. 4) and the first measured point in the stress sequence.

IV. CHARGE BALANCE IN MO(I)SCAPACITORS
A. GAN-ON-SI CPW AS AN MIS STRUCTURE

The complex nature of GaN-on-Si stacks (which typically contain more than 10 individual layers) makes modelling them a difficult task, especially in a TCAD environment.

Regarding RF substrate loss description however, it is helpful to describe the CPWs fabricated on a GaN-on-Si stack as simple Metal-Insulator-Semiconductor (MIS) structures.

DC current across the AlN/Si interface exists and has been studied in other works for a wide range of voltages [6]. When the full buffer is grown on top of the nucleation layer, DC voltage drop across the AlN/Si interface becomes small compared to the applied voltage, and the measured current is negligible for the biases considered here ($|V_{chuck}| \leq$ 50 V) [25].

Furthermore, there is no layer in the III-N stack with sufficient conductivity to contribute significantly to conductive RF loss. Free carrier concentration in the bulk III-N materials is many orders of magnitude lower than in silicon and careful optimisation of the buffer structure suppressed any undesired two-dimensional electron/hole gas (2DEG/2DHG). This has been confirmed by capacitance measurements, where capacitance in strong accumulation corresponds to the full III-N stack thickness. Finally, current injection from the top metallization into the GaN channel does not contribute significantly to the observed stress/relaxation sequences. As shown in [14], passivating the GaN channel with a thick SiO$_2$ layer did not alter the hysteresis observed in ρ_{eff}-V$_{chuck}$ curves.

The previous considerations allow us to ignore any DC current from the CPW traces to the chuck and to consider the complex GaN-on-Si substrate as a variation of the extensively studied MIS structure with additional charge redistribution mechanisms.

FIGURE 5. (a) Charge distribution used in the simulated MIS stack. (b) Flat-band voltage shift calculated for the charge distribution shown in (a). The position of the peak charge is varied from the GaN channel/buffer interface to the buffer/AlN interface. ΔV_{FB} depends on the charge density, but also on its position in the buffer.

B. CHARGE DISTRIBUTION AND FLAT-BAND VOLTAGE

For MIS systems, the flat-band voltage (V_{FB}) determines the number of free carriers at Si surface under zero bias condition [26]. V_{FB} corresponds to the voltage to be applied for zero band bending in silicon, and is given by:

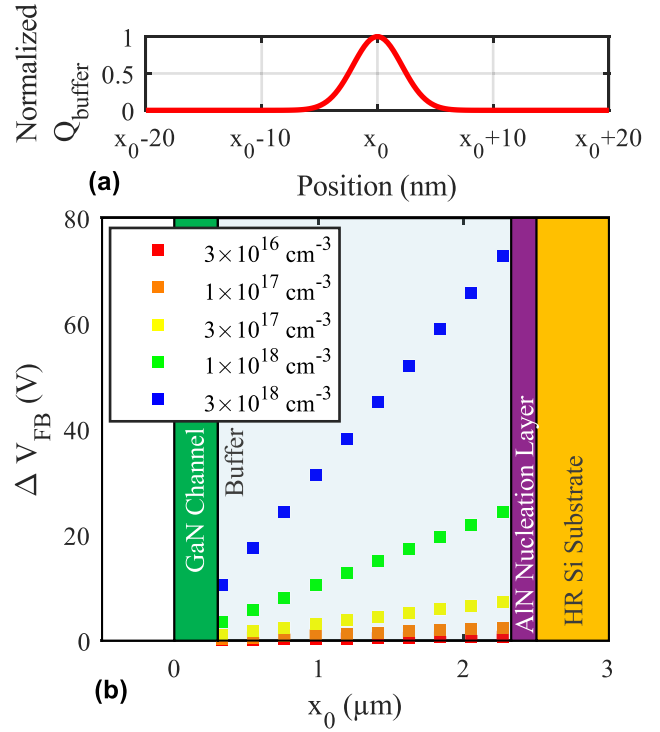$$V_{FB} = W_{MS} - \frac{Q_{buffer}}{C_{buffer}} \quad (1)$$

where W_{MS} is the metal-semiconductor workfunction, Q_{buffer} is the equivalent interface buffer charge per unit area contributing to V_{FB} and C_{buffer} is the capacitance per unit area of the semi-insulating III-N layers. The presence of a non-zero Q_{buffer} will lead to a flat-band shift ΔV_{FB} compared with the theoretical charge-free case.

For SOI substrates, oxide charge is entirely confined in a region close to the oxide/silicon interface and is independent of bias. In such cases, Eq. (1) is valid. However, due to the semiconducting nature of III-N buffers, GaN-on-Si buffer charge can consist of a spatial distribution of trapped charges and free carriers, that can furthermore depend on bias. Q_{buffer} is then given by:

$$Q_{buffer} = \frac{1}{t_{buffer}} \int_0^{t_{buffer}} x \, q(x) dx \quad (2)$$

where $q(x)$, the space-dependent charge per unit volume, is integrated from the metal/III-N interface ($x = 0$) to the AlN/Si interface ($x = t_{buffer}$). Eq. (2) demonstrates that equivalent interface charge, and consequently V_{FB} is dependent on the spatial distribution of charge.

To exemplify this effect, a simplified 1-D MIS system is considered. Dimensions of the III-N layers correspond to Fig. 1 and a 3-layer III-N stack was used. Instead of the C trap levels, a simple positive charge distribution $q(x)$ sharply localized around a variable depth x_0 is added (Fig. 5a). Fig. 5b shows the calculated ΔV_{FB} for this MIS structure. As an example, a charge peak with a density of 10^{18}cm^{-3} located at $x_0 = 1$ μm from the GaN channel surface causes a flat-band shift of ~10 V.

By sweeping the position of the peak charge x_0 from the GaN channel/buffer interface to the buffer/AlN interface, ΔV_{FB} changes by a factor exceeding 3. While the effect is limited for low charge, for the highest charge density studied (3×10^{18}cm^{-3}, comparable to active C doping concentration in GaN-on-Si buffers [12]), up to 60 V shift is theoretically possible.

The shift in V_{FB} caused by charge redistribution across the semi-insulating layers will in turn affect the conductivity of the PSC (G$_{PSC}$) layer and ρ_{eff}. Indeed, changing V_{FB} is equivalent to applying a corresponding bias on the MIS structure, attracting or pushing free carriers away from the AlN/Si interface. Fig. 6 shows the evolution of free electron concentration close to the surface of the high-resistivity
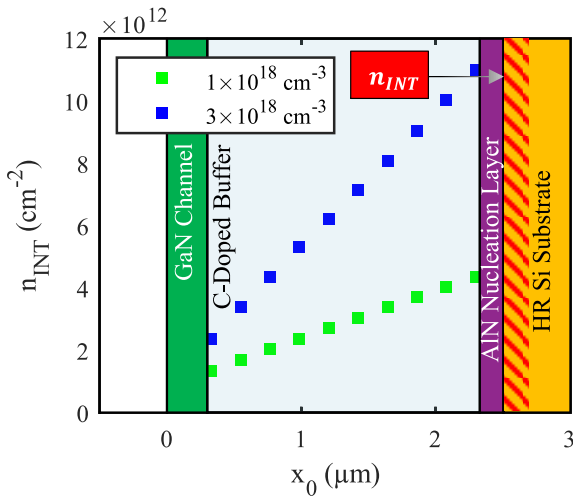
FIGURE 6. Interface free carrier sheet density for different positions of the localized charge. For high peak charge, n_{INT} is strongly affected by buffer charge location.

n-type Si substrate (n_{INT}), simulated for different positions of a positive charge distributed according to Fig. 5a.

C. A HIGH-PERFORMANCE SUBSTRATE ISSUE

The considerations above only become relevant for high-ρ_{eff} substrates. To exemplify this, consider the 2D-extension of the 1-D system analysed in previous sections. Electrodes are added on top of the III-N buffer to represent the cross-section of a CPW line. A small-signal simulation of this 2D structure allows extraction of ρ_{eff} as a function of the position of the localized charge x_0. Three different Si substrates are considered for the simulation. The p-type doping profile close to Si surface responsible for the PSC layer and measured by spreading resistance profiling (SRP) is included and multiplied by 1 (physical profile), 10 and 100 (hypothetical high-loss substrates) to obtain ρ_{eff} values of 1.1 k, 550 and $120 \Omega \cdot cm$, respectively.

As expected from Section-IV.B, ρ_{eff} is affected by the position of the charge peak (x_0) for all substrates, as shown in Fig. 7. However, the relative variation is more significant for the high-ρ_{eff} substrate (up to ~15% variation) than for the low-ρ_{eff} one (negligible variation). Indeed, when a high number of free carriers are present in the PSC layer (low ρ_{eff}) the ΔV_{FB} change induced by buffer charge redistribution cannot modulate G_{PSC} as much as when few free carriers populate the PSC (high ρ_{eff}).

Furthermore, this implies that the buffer charge redistribution has a more significant effect at low temperature. As temperature increases, thermo-generated free carriers in the Si substrate contribute to its conductivity increase, and thus the decrease of the ρ_{eff}. Consequently, the relative variation of ρ_{eff} during the stress experiments at 190 °C (where $\rho_{eff} \cong 220 \Omega \cdot cm$) is more limited compared with 50 °C (where $\rho_{eff} \cong 1,200 \Omega \cdot cm$).
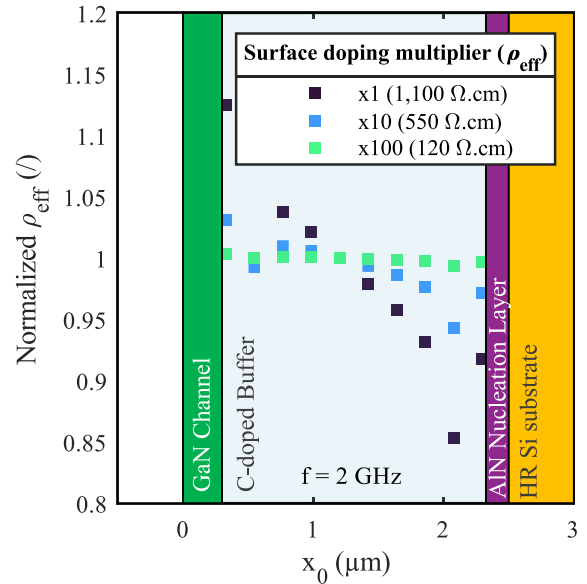
FIGURE 7. Variation of normalized ρ_{eff} as a function of the position of the localized charge (peak density: $3 \times 10^{17} cm^{-3}$) for three different substrates showing typical ρ_{eff} values. The relative variation is strongest for the substrate showing highest ρ_{eff}.

V. REDISTRIBUTION OF TRAPPED CHARGE IN GAN-ON-SI STACKS

In this section, the theoretical concepts of buffer charge redistribution and its effect on PSC conductivity in MIS structures are applied to a more complex GaN-on-Si substrate. The simple charge distribution considered in Section IV is now replaced by the C traps as described in Section II.C, and the more exact 4-layer stack of Fig. 1 is used.

In [15], it was already shown that a simple 3-layer GaN-on-Si stack TCAD model could reproduce the time-dependent experimental features of the ρ_{eff} relaxation curve. Slow redistribution of trapped charge between the top and bottom buffer interfaces was identified as the main source of slow time-dependent behaviours.

Fig. 8 shows the simulated normalized ρ_{eff} during the stress phase ($V_{chuck} = +50$ V) for sample A. More detail on the small-signal transient simulation methodology can be found in [15].

A qualitative match with experimental data is achieved. Notably, the inclusion of a Poole-Frenkel transport mechanism representing transport through defects across the III-N layers leads to a better reproduction of time constants compared to our previous work [15]. The activation energy extracted from the simulated curves (0.62 eV) is also closer to the experimental one (0.57 eV).

The same TCAD model is used in the following to investigate the key parameters responsible for the slow charge redistribution. The impact of carbon doping concentration, buffer thickness and transport in the buffer are investigated.

A. CARBON DOPING CONCENTRATION

Fig. 9 shows the simulated stress transient ($V_{chuck} = -50$ V) for increasing carbon concentration. Top and
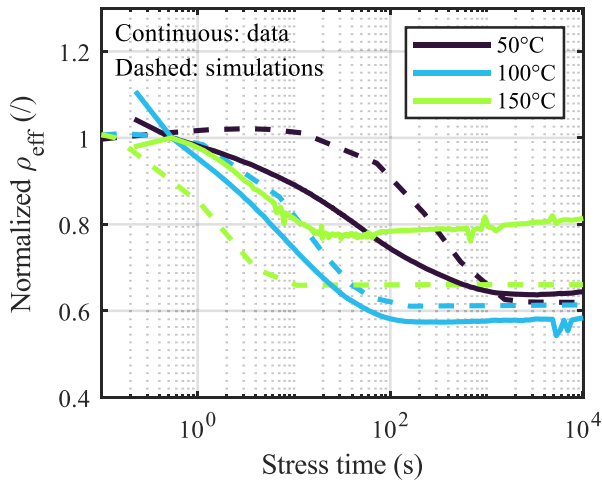
FIGURE 8. Simulated and measured normalized effective resistivity during the stress phase (V_{chuck} = +50 V). Long time constants and temperature-dependent features observed experimentally are reproduced by the 2D TCAD model.

FIGURE 9. Simulated evolution of trapped charge close to top and bottom interfaces of the C-doped buffer while stressing the substrate at V_{chuck} = −50 V, for different C concentrations. The charge is normalized to the C concentration. Redistribution of charges is not significantly accelerated or slowed down by changing C doping in the buffer.

bottom buffer charges are defined as trapped charges integrated across the closest 200 nm to the relevant interface (buffer/channel and buffer/AlN, respectively). In response to the bias step, positive charges (holes) are attracted towards the bottom of the buffer. Consequently, negative trapped charges decrease (increase) at the bottom (top) of the buffer.
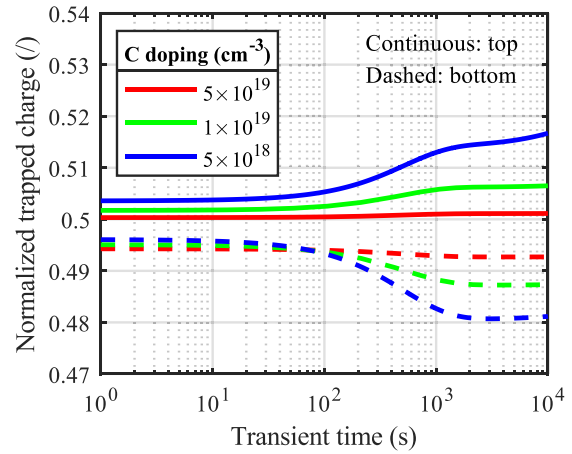
By changing C doping concentration, no significant change in time constant is observed. For a given stress bias, the quantity of charges to be redistributed inside the buffer is constant and independent of C doping. An increased C doping will allow the depletion region contributing to charge redistribution to become narrower. However, the rate of redistribution, dominated by transport across the buffer, is not significantly affected.

For [C] = 5×10^{18}cm^{-3}, the low C concentration is not sufficient to provide enough charges in the top and bottom 200 nm of the buffer used for integration. The depletion region extends beyond that thickness and the first 200 nm are entirely depleted. Consequently, trapped charges in Fig. 9 seem to saturate earlier but in reality, the redistribution processes keep taking place closer to the centre of the buffer.
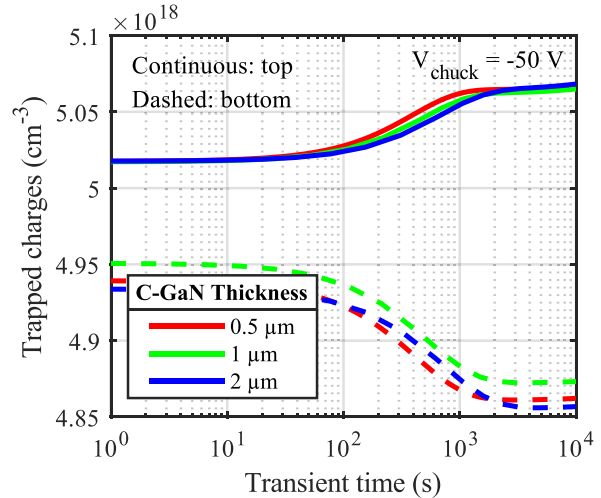
B. BUFFER THICKNESS

Reducing the thickness of the buffer reduces the distance between the conductive PSC layer and the overlying circuits. Effective resistivity and substrate linearity is in turn reduced. However, thinner buffers bring the additional benefit of lower thermal budget, and potentially lesser Al and Ga diffusion [7].

Fig. 10 shows the simulated stress transient (V_{chuck} = −50 V) for typical values of GaN-on-Si buffer thickness. GaN channel and AlN thicknesses were kept constant, and only the C-doped buffer thickness was varied. While charges redistribution takes place in > 10,000 s for the 3 μm-thick buffer, saturation is reached in ~5,000 s for the thinner

FIGURE 10. Simulated evolution of top and bottom buffer charge during the stress phase (V_{chuck} = −50 V) for different C-GaN thicknesses. [C] = 10^{19} cm^{-3}.

buffer (1 μm). Thinning the buffer reduces the distance that free carriers must travel between the traps that emit them (at the top of the buffer) and the traps that capture them (at the bottom of the buffer). Consequently, a steady-state is reached faster.

C. VERTICAL TRANSPORT PATHS

From the previous discussions, it appears that the time constants are more dominated by transport across the C-doped buffer than by the C traps themselves. Charge transport across III-N layers has been extensively studied in order to mitigate current collapse issues in GaN HEMTs. Several mechanisms have been proposed to model the vertical leakage in highly doped buffers, namely variable-range hopping (VRH) or Poole-Frenkel transport (PF) [27], [28]. Both mechanisms represent transport through defects in the
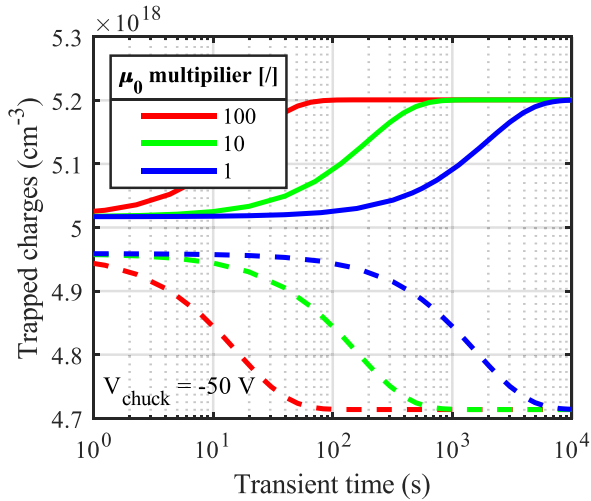
FIGURE 11. Simulated evolution of top and bottom buffer charge during the stress phase ($V_{chuck} = -50$ V) for varying hole mobility. Enhanced hole transport across the III-N layers can greatly reduce the time-dependence of ρ_{eff} through accelerated charge redistribution.

III-N layers, such as dislocations. PF was found to fit our experimental ρ_{eff} data better. PF mobility is given by:

$$\mu_{PF} = \mu_0 \exp\left(\frac{E_a}{kT} + \gamma\sqrt{E}\right) \qquad (3)$$

where E, the vertical electric field, was estimated assuming uniform potential drop across the buffer and γ, E_a were taken from [18]. Zero-field mobility μ_0 was left as a fitting parameter and the best fit was achieved for $\mu_0 = 320$ cm^{2}V^{-1}s^{-1}.

In this section, μ_0 is varied to confirm the importance of charge transport in the time-dependence of ρ_{eff}. Varying μ_0 can also be seen as a simplified way of adding vertical leakage paths in the buffer. The necessity of vertical leakage paths in GaN-on-Si buffers has been highlighted in the past as a solution to limit dynamic R_{ON} [11]. In practice, an increased number of dislocations in the defective buffer can provide such additional leakage paths. The TCAD experiment can help understand the dependence of ρ_{eff} on vertical transport. Fig. 11 shows the simulation results for a μ_0 factor of 1 (fit to experimental data), 10 and 100 (high value, representing a high dislocation density). For the lowest mobility, steady-state is reached in ∼6,000 s, comparable with the experiment. With enhanced hole transport, the steady-state is reached significantly faster: 700 s and 80 s for a factor of 10 and 100, respectively. From Fig. 11, it is clear that the limiting factor in slow charge redistribution in the GaN-on-Si buffer is the transport of holes between the top and bottom interfaces of the buffer.

VI. TIME DEPENDENCE OF HARMONIC DISTORTION
From previous sections, the slow charge redistribution in the buffer layers will modify G_{PSC} through modulation of the MIS structure's V_{FB}. This is observed experimentally by

a slowly varying ρ_{eff}. Moreover, the substrate linearity is affected, as previously shown in Fig. 4.

In addition to the slow charge redistribution and V_{FB} change, the PSC layer also sees the RF bias imposed by the large-signal excitation of the HD measurement. HD is dictated by the bias sensitivity of the PSC layer to the large-signal excitation only, because variations in buffer charge take place over times significantly longer that the large signal period ($f_0^{-1} = $ ∼1 ns). However, the slow change of the MIS V_{FB} during the stress sequence can alter both G_{PSC} and its sensitivity to rapid bias changes. For example, in response to a change in V_{FB} change the PSC could be in a state of strong accumulation (less bias-sensitive conductivity, low HD) or closer to depletion (highly bias-sensitive conductivity, high HD).

Consequently, it is difficult to correlate the time dependence of ρ_{eff} to that of HD. Indeed, predicting HD during the stress sequence would require the knowledge of instantaneous $G_{PSC}(V_{large-signal})$ curves at each point in time.

VII. CONCLUSION
Experimental substrate stress-relaxation sequences show a slow response of effective substrate resistivity for un-implanted GaN-on-Si substrates. This time-dependence, characterized by relaxation times exceeding 1,000 s, should be limited in order to avoid detrimental effects on substrate linearity. To gain more insight on the charge redistribution at play in the GaN-on-Si buffer, a 1-D, 3-layer stack was implemented in TCAD.

From those simulations, the time constants appear to be limited by the efficiency of free carriers (holes) transport vertically through the buffer, likely with help of a Poole-Frenkel mechanism. More particularly, increasing the zero-field hole mobility in the C-doped buffer layers leads to a significant decrease in time constants. This corresponds to increasing the amount of conducting defects such as dislocations in the buffer. To lesser extent, thinning down the buffer can also contribute to a faster response. Similar to R_{ON} degradation studies, this shows the importance of vertical transport paths in GaN-on-Si buffers.

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