Received 14 September 2023; revised 21 January 2024; accepted 28 March 2024. Date of publication 1 April 2024; date of current version 28 May 2024.
The review of this article was arranged by Editor E. Choi.

Digital Object Identifier 10.1109/JEDS.2024.3384008

Small-Signal and Large-Signal RF Characterization and Modeling of Low and High Voltage FinFETs for 14/16 nm Technology Node SoCs

ANIRBAN KAR [1] (Graduate Student Member, IEEE), SHIVENDRA SINGH PARIHAR [1] (Member, IEEE), JUN Z. HUANG [2], HUILONG ZHANG [2] (Member, IEEE), WEIKE WANG [2], KIMIHIKO IMURA [2], AND YOGESH SINGH CHAUHAN [1] (Fellow, IEEE)

1 NanoLab, Department of Electrical Engineering, Indian Institute of Technology Kanpur, Kanpur 208016, India
2 MaxLinear Inc., Carlsbad, CA 92008, USA

CORRESPONDING AUTHOR: A. KAR (e-mail: anirbank@iitk.ac.in)

This work was supported in part by the Swarna Jayanti Fellowship under Grant DST/SJF/ETA02/2017-18, and in part by the Fund for Improvement of Science and Technology Infrastructure (FIST) Scheme of the Department of Science and Technology under Grant SR/FST/ETII-072/2016.

ABSTRACT Modern System-on-Chip (SoC) architectures necessitate low-voltage (LV) core transistors featuring excellent digital, analog, and radio frequency (RF) properties, as well as thick oxide transistors serving as robust I/O buffers and high-voltage (HV) transistors essential for efficient power management. This study presents a comprehensive DC to RF characterization, a detailed modeling strategy, and subsequent model parameter extraction for commercially produced LV and HV Fin Field Effect Transistors (FinFETs) at 14/16 nm technology. The industry-standard BSIM-CMG compact model is modified to accurately capture the characteristics of the HV FinFET devices integrated with the digital LV FinFETs for SoC applications. A detailed analysis of the DC, analog, and RF performance of LV, I/O, and HV FinFETs compared to the contemporary planar CMOS technology is performed. The large-signal performance of the device is evaluated using the developed model and validated with the measured data. Finally, a concise overview of the performance indicators associated with the modeled device is also presented.

INDEX TERMS FinFET, RF, LDMOS, SoC, large-signal, compact model, BSIM-CMG, high-voltage.

I. INTRODUCTION

THE ADVANCEMENT of planar digital logic technology has facilitated the scaling of complementary metal-oxide-semiconductor (CMOS)-based radio frequency (RF) system-on-chip (SoC) to the 20 nm technology nodes, employing techniques such as high-k dielectrics, metal gates, and strain engineering [1]. However, these approaches have encountered challenges such as leakage currents and short-channel effects that adversely affect the analog and RF performances [2]. Fin Field Effect Transistor (FinFET) technology has been embraced at the sub-22 nm technology node to overcome these challenges as an alternative to conventional planar CMOS technologies [3], [4], [5], [6], [7], [8]. FinFETs offer benefits like reduced leakage current, lower threshold voltage (V_{TH}), enhanced drive current, and improved output resistance, eventually enhancing analog performance within a specific leakage current range. Additionally, the inherent design of FinFETs enables reduced silicon footprint and decreased power consumption, making them particularly well-suited for developing next-generation digital and RF SoC architectures [5]. Nevertheless, the three-dimensional (3-D) architecture of FinFETs introduces higher parasitic effects, which impact its RF performance [9]. This is attributed to the saturation of transconductance ($\mathrm{g_m}$) as channel length scales below approximately 20 nm, along with the detrimental impact of higher parasitic effects.

The continuous progression of semiconductor technology has yielded advancements in the design of SoC-based

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integrated circuits (ICs), resulting in enhanced operational efficiency concerning power management, layout optimization, and seamless signal integration [10], [11], [12], [13], [14], [15]. The architectural framework of SoC-based designs necessitates not only optimal RF efficiency but also the amalgamation of both low-power digital blocks and high-voltage (HV) units. HV devices are employed in SoC architectures to facilitate the integration of regulators and converters for various power rails, WiFi, and mobile transceiver units [16], [17], [18]. Notably, at the 22 nm technology node, planar RF laterally diffused metal-oxide-semiconductor (LDMOS) devices based on fully depleted silicon-on-insulator (FDSOI) show promising results, especially in the Internet of Things (IoT) and SoC applications [19]. However, at the 14/16 nm technology nodes, low-voltage (LV) FinFETs have showcased commendable performance achievements in low-power operation and high-performance logic paradigms [20], [21], [22], [23]. To facilitate the ongoing scalability of SoCs, it is crucial to integrate FinFET technology-based HV devices with LV FinFETs. This integration will improve the performance, spatial efficiency, and power consumption of the SoCs. The HV units in SoCs conventionally operate within a voltage range spanning 3.3 V to 5 V, with a designated breakdown voltage rating typically two-fold that of the nominal supply voltage (V_{DD}) [18]. The holistic growth of FinFET-based SoCs demands extensive characterization and analysis of DC, small-signal RF, and large-signal characteristics of FinFET devices.

In this work, we have exhibited the comprehensive RF characterization and modeling of state-of-the-art, production-level 14/16 nm FinFET-based LDMOS (Fin-LDMOS) devices along with their LV FinFET counterparts, demonstrating their digital and analog performance metrics. The industry-standard Berkeley Short-channel IGFET Model-Common Multi-Gate (BSIM-CMG) model [24] has been modified to incorporate the impact of overlap charges and drift resistance of the extended drain region of the HV device [25]. This enhancement enables the model to accurately represent the DC, RF, and large-signal characteristics of HV devices.

To summarize, the key contributions of this work are:

- For the first time, we have presented the RF and large-signal characterization of the 14/16 nm Fin-LDMOS HV transistors.
- We use the modified industry-standard BSIM-CMG model to accurately capture the DC and RF characteristics of the LDMOS transistors all the way up to 43.5 GHz.
- We have presented the parasitic networks necessary to represent the load-pull measurement setup and the pad parasitics, which, along with the developed model's proper DC and RF model parameter sets, accurately capture the large-signal characteristics of the transistors.
- We have provided a detailed small to large-signal RF parameter extraction strategy of the Fin-LDMOS transistors using the newly developed BSIM-CMG-based compact model
- We have presented the key figures of merit of the transistors at 14/16 nm node and compared them with contemporary state-of-the-art technologies.

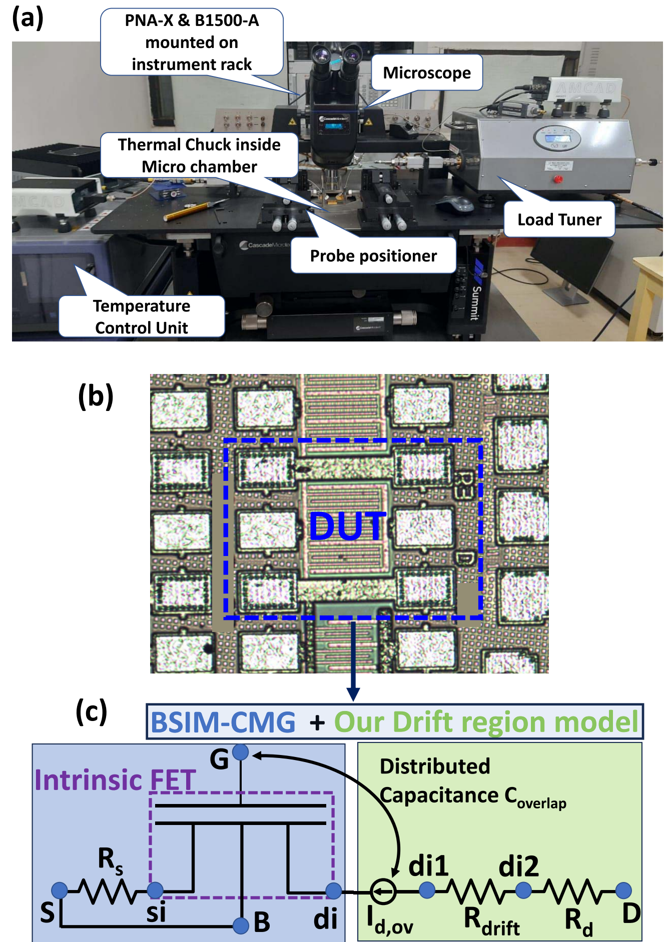

FIGURE 1. **(a) Load-pull setup for large-signal measurements (b) Microscopic image of the on-wafer DUT (c) Equivalent model diagram of the HV FinFET.**

In this article, a brief description of the measured device and its characterization is presented in Section II. The modeling strategy is explained in Section III, and Section IV explains the parameter extraction procedure using the modified BSIM-CMG model. Section V provides a concise overview of the performance metrics associated with the modeled device, and finally, we conclude in Section VI.

II. DEVICE CHARACTERIZATION

Fig. 1(b) (a) shows the load-pull measurement setup, and the fabricated Ground-Signal-Ground (G-S-G) structure of the device under test (DUT) is shown in Fig. 1(b) (b). We have performed in-house DC, small-signal RF, and large-signal load-pull characterization of the device to analyze the performance metrics of the FinFET devices at 14/16 nm technology node.

DC & Small Signal Measurements: We have comprehensively characterized production-level multi-fin, multi-finger

n-channel silicon FinFET devices, encompassing both LV and HV variants. The characterization process involves on-wafer measurements, employing the Cascade Summit 11K Probe station. Bias voltages essential for the DUT have been supplied using the Keysight B1500A equipment, while high-frequency S-parameter measurements spanning the range of 500 MHz to 43.5 GHz have been performed using the Network Analyzer Keysight PNA-X N5244A. Infinity probes are used for accurate DC and RF characterization. We have adopted Open-Short de-embedding and Short-Open-Load-Through (SOLT) techniques to mitigate the influences of contact pads and wiring-related parasitics. Specifically, Open-Short de-embedding countered pad-related effects, while SOLT techniques mitigated the wiring-related effects [26].

Large Signal Load-Pull Measurements: An AMCAD passive load-pull measurement system, utilizing the Cascade Summit probe station, facilitates the acquisition of large-signal measurements. The load-pull configuration incorporates a Maury Microwave Load Tuner (Model: XT982GL01), capable of covering frequencies ranging from 0.6 GHz to 18 GHz. This setup is complemented by Keysight's Network Analyzer (Model: PNA-X N5244A), which is configured in conjunction with the tuner to generate the RF signal. The Keysight B1500A unit is also employed to provide the necessary DC bias. The load-pull measurements are executed using a high-power bidirectional coupler positioned at both the input and output of the DUT. This coupler effectively segregates the incident and reflected RF signals during load-pull evaluations. The PNA-X Network Analyzer captures the incident and reflected waves traversing the source and receiver paths. Subsequently, it calculates the large-signal performance parameters, including delivered output power (P_{out}), transducer gain (GT), power gain (Gp), Power Added Efficiency (PAE), and gain compression, etc. The measurement procedure involves calibration of the load-pull system and sweeping the delivered input signal power within a range of −43 dBm to −12 dBm, at frequencies 2.5 GHz and 6 GHz. The HV device has been biased at a gate-to-source voltage (V_{GS}) of 1 V/0.6 V and a drain-to-source voltage (V_{DS}) of 3.5 V to get the optimum performance.

III. MODEL DESCRIPTION

The equivalent circuit diagram of the HV device representing the compact model integration is shown in Fig. 1(b) (c). The industry-standard BSIM-CMG is extensively employed to model FinFET devices in digital, analog, and radio frequency applications [24], [27], [28]. The BSIM-CMG model is a charge-based core model that forms the model's basic mathematical formulation [23], [27], [28]. The higher-order effects like velocity saturation, channel length modulation, source-drain resistances, self-heating, mobility degradation, drain-induced barrier lowering (DIBL), V_{TH} roll-off, etc. are incorporated into the core model to capture the characteristics of the LV FinFET devices accurately [24], [28]. The unified core model relies on the bias voltage and charges relation as defined using (1) [23], [27].

$$v_g - v_o - v_{ch} = -q_m + \ln(-q_m) + \ln\left(\frac{q_t^2}{e^{q_t} - q_t - 1}\right) \quad (1)$$

where,

$$v_o = v_{fb} - q_{dep} - \ln\left(\frac{2qn_i^2 A_{ch}}{V_t C_{ins} N_{ch}}\right)$$
$$q_t = \left(q_m + q_{dep}\right) r_N. \quad (2)$$

Here, $v_g = V_G/V_t$ is the normalized gate potential (V_t is the thermal voltage), $r_N = A_{ch} C_{ins}/\epsilon_{si} W^2$, v_{ch} is the normalized channel potential along the source to drain direction, C_{ins} is the oxide capacitance per unit length, $q_m = Q_m/(V_t C_{ins})$, and $q_{dep} = (qN_{ch}A_{ch})/(V_t C_{ins})$ are normalized mobile and depletion charges in the device, respectively [23]. The three terms on the right-hand side of (1) represent the charge components in the different regimes of operation of the device. The first term denotes the linear dependency between the charge and gate voltage at strong inversion; the second logarithmic term indicates the relation between the charge and voltage at weak inversion, and the third term represents the behavior at moderate inversion.

However, the model does not incorporate a dedicated formulation for the drift region resistance and charges in the gate overlap region of the HV devices. This aspect is crucial for achieving accurate simulations of HV transistors. In our previous work, we developed a model for the drift resistance and gate overlap charges in the drift region of the HV device [25]. The drift region has been modeled as a function of the voltage drop in the drift region, as shown in (3).

$$R_{drift} = R_0\left[1 + \delta\left(\frac{|V_{di1,di2}|}{V_{drift}}\right)^{\beta}\right]^{1/\beta} \quad (3)$$

where,

$$\delta = \frac{|V_{di1,di2}|^{4-\beta}}{|V_{di1,di2}|^{4-\beta} + \alpha V_{drift}^{4-\beta}} \quad (4)$$

where, $V_{drift} = q \cdot W \cdot NDR \cdot t_{dr} \cdot VDRSAT \cdot R_0$, α and β are fitting parameters. Here, W denotes the effective width of the device, while NDR represents the doping density in the drift region. The parameter t_{dr} corresponds to the thickness of the drift region, and VDRSAT signifies the factor that characterizes the velocity saturation of carriers traversing the drift region. The inclusion of the term δ ensures the fulfillment of the Gummel symmetry test, as detailed in [29]. The potential difference between nodes $di2$ and $di1$ [illustrated in Fig. 1(c)] is denoted by $V_{di1,di2}$. The bias-independent resistance of the drift region, denoted as R_0, is formulated as $R_0 = LDRIFT/(q \cdot \mu_{DR} \cdot NDR \cdot ADR)$. In this expression, μ_{DR}, NDR, LDRIFT, and ADR represent the drift region's mobility, doping concentration, length, and cross-sectional area, respectively. The HV transistor

functions as an intrinsic core component, to which a drift region model is introduced [see Fig. 1(c)]. This extended drain region, denoted as the drift region, offers high resistance, allowing a maximum voltage drop across it. This high resistance subsequently causes the carrier velocity to saturate, thereby inducing a state of quasi-saturation in the drain current behavior [30], [31], [32], [33] [see Fig. 4]. The gate overlap charges model developed in [25] has been used to model the capacitance behavior of the device. The overlap charge (Q_{OV}) formulation is shown in (5) - (7). The calculated Q_{OV} have been shared between internal nodes di ($Q_{di,OV}$) and $di1$ ($Q_{di1,OV}$), as shown in [25]. The Q_{OV} is a function of the bias voltages (V_{GS} and V_{DS}) and also depends on parameters like flat-band voltage of the drift region VFB, length of the overlap region LOV, and doping of the drift region NDR [25]. All other variables in the equations have the same representation as in [25]. These overlap charges give rise to overlap capacitances in the HV device. This modified BSIM-CMG code has been used to extract the parameters to model the RF characteristics of the device.

$$Q_{OV} = \eta \cdot \mathrm{W} \cdot \mathrm{LOV}\left[q_{ova} + \frac{1}{6} \cdot \frac{\Delta q^2}{q_H}\right]. \tag{5}$$

$$Q_{di1,OV} = \eta \cdot \mathrm{W} \cdot \mathrm{LOV}\left[\frac{q_{ova}}{2} - \frac{\Delta q}{12} \cdot \left(1 - \frac{\Delta q}{q_H} - \frac{1}{5} \cdot \frac{\Delta q^2}{q_H^2}\right)\right] \tag{6}$$

$$Q_{di,OV} = Q_{OV} - Q_{di1,OV} \tag{7}$$

IV. COMPACT MODEL EXTRACTION

A. CALIBRATION FOR DC

To begin with the model extraction, we extract the parameters of BSIM-CMG governing the sub-threshold behavior of the transistor. We choose the transfer characteristics ($I_{DS} - V_{GS}$) at lower V_{DS} to extract the sub-threshold region parameters. We tune parameters associated with the metal work function (PHIG) to extract the V_{TH} and also fine-tune trap-related parameters such as CIT to align with the sub-threshold slope characteristics. To accurately capture the impact of drain voltage, we optimize the DIBL-related parameters like ETA0, CDSCD, and PDIBL0 by fitting the sub-threshold region at multiple V_{DS}. Once we achieve a good agreement between measurement and simulation results in the sub-threshold regime, we extract the model parameters that impact the transistor characteristics in the moderate and strong inversion region. The low field mobility is extracted in the vicinity of V_{TH} using the U0 parameter; other mobility-related parameters like EU, UA, ETAMOB, and UD are determined by fitting $I_{DS} - V_{GS}$ and transconductance vs. gate voltage (g_m - V_{GS}) characteristics at higher V_{GS}, as depicted in Fig. 2 (a). The parameter UA is optimized to fit the peak region of the g_m, and model parameter EU is optimized by fitting the slope of $I_{DS} - V_{GS}$ in moderate to strong inversion regime. Source and drain resistance parameters (RSW, RDW) are extracted in the strong inversion, corresponding to the device's operation in the linear mode at low V_{DS}. To model the transistor behavior at higher V_{DS}, we simultaneously fit the $I_{DS} - V_{GS}$ and output characteristics ($I_{DS} - V_{DS}$). We extract model parameters associated with carrier velocity saturation and channel length modulation to capture the $I_{DS} - V_{DS}$ behavior observed at higher V_{GS}. On the other hand, the impact of DIBL is extracted at lower V_{GS} using both $I_{DS} - V_{GS}$ and $I_{DS} - V_{DS}$ characteristics. Parameters such as VSAT, VSAT1, KSATIV, PTWG, and PCLM are adjusted to account for the influence of velocity saturation, g_m degradation, and channel length modulation. Model parameter PTWG is tuned to fit the decrease in the g_m with increasing V_{GS} at higher V_{DS}. The channel length modulation parameter PCLM is extracted by observing the slope of $I_{DS} - V_{DS}$ at higher V_{GS}. The MEXP parameter is also fine-tuned to ensure a seamless transition of the $I_{DS} - V_{DS}$ data at mid-V_{DS} range,

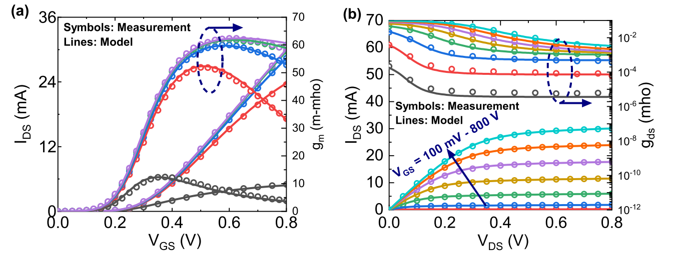

FIGURE 2. DC characteristics of LV FinFET (a) $I_{DS} - V_{GS}$ at V_{DS} = 50 mV, 300 mV, 500 mV, 700 mV and 800 mV.(b) $I_{DS} - V_{DS}$ at V_{GS} = 100 mV - 1.5 V in steps of 200 mV [15].

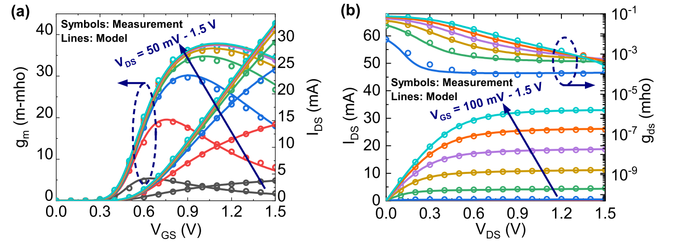

FIGURE 3. (a) Transfer (at V_{DS} = 50 mV, 300 mV - 1.5 V in steps of 300 mV) and (b) Output characteristics (at V_{GS} = 100 mV - 1.5 V in steps of 200 mV) of n-type I/O FinFET (thick-oxide) [15].

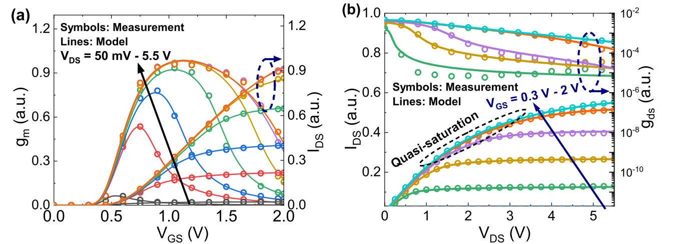

FIGURE 4. Terminal characteristics of HV FinFETs: (a) Normalized drain current and transconductance versus gate voltage at multiple drain bias (V_{DS} = 50 mV, 0.5 V, 1 V, 2 V, 3.5 V, and 5.5 V). The effect of drift resistance is evident at higher gate bias, where the drain current is almost constant with increasing gate bias. (b) $I_{DS} - V_{DS}$ characteristics (at V_{GS} = 0.3 V - 2 V in steps of 300 mV) highlight the quasi-saturation effect. The drift region is velocity saturated when the intrinsic MOS is in the linear region, resulting in an insignificant current increase with increasing gate bias at higher V_{DS}.

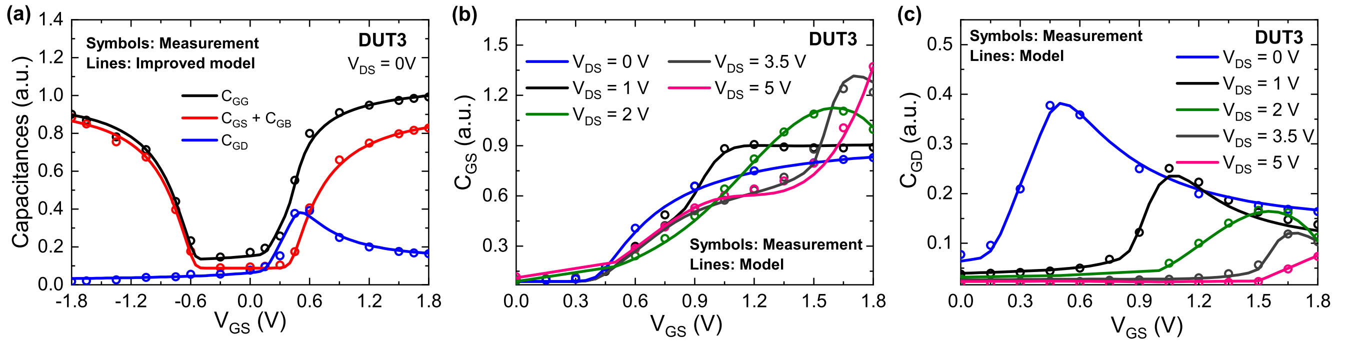

FIGURE 5. The variation of capacitance with gate and drain bias at 500 MHz frequency (a) Normalized capacitances at V_{DS} = 0 V. (b) Normalized V_{GS} at multiple V_{DS} (c) Normalized C_{GD} at multiple V_{DS} [25].

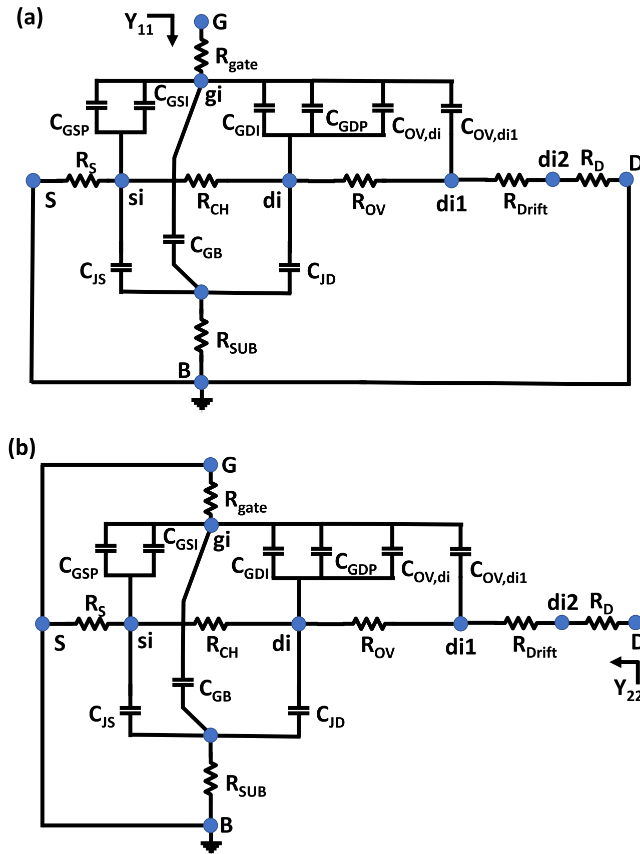

FIGURE 6. Equivalent network representation of the HV FinFET for evaluating (a) Y_{11} (b) Y_{22}.

as demonstrated in Fig. 2 (b). A similar methodology is applied to the extraction of I/O FinFET models (see Fig. 3).

B. ADDITIONAL STEPS FOR HV FINFETS

HV metal-oxide-semiconductor field effect transistors (MOSFETs) are conceptually represented as intrinsic MOSFETs connected in series with an extended drain region, the latter being characterized by a bias-dependent drift resistance. In HV devices, the carriers in the drift region, in addition to the channel carriers, also undergo velocity

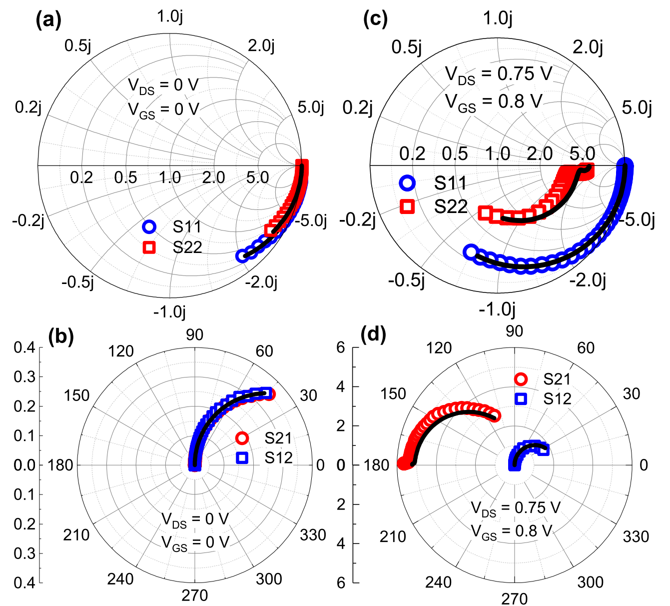

FIGURE 7. S-parameter validation of LV FinFET device for 500 MHz to 43.5 GHz frequency range (a) S_{11}, (b) S_{22}, (c) S_{21}, and (d) S_{12} for different biases.

saturation. The manifestation of the drift region's resistance and the consequential quasi-saturation phenomenon [30], [31], [32], [33] are clearly visible in the behavior of the drain current [see Fig. 4 (b)]. In the initial phase, we extract model parameters related to the intrinsic field effect transistor (FET) (as mentioned earlier) to effectively model the DC characteristics [see Fig. 4]. Subsequently, the parameters of the drift resistance model, namely VDRSAT, NDR, and β are adjusted to accurately capture the degradation of g_m at high V_{GS} and the notable quasi-saturation effects within the $I_{DS} - V_{DS}$ behavior. The NDR parameter, which modulated the resistance of the drift region, is tuned to capture the g_m degradation. The VDRSAT and β are adjusted to capture the $I_{DS} - V_{DS}$ characteristics at high V_{GS} and mid-V_{DS}. It can be clearly observed in Fig. 4 (b) that in the mid-V_{DS} regime, the drain current becomes insensitive to the V_{GS}, which is termed as quasi-saturation. The parameters VDRSAT and β

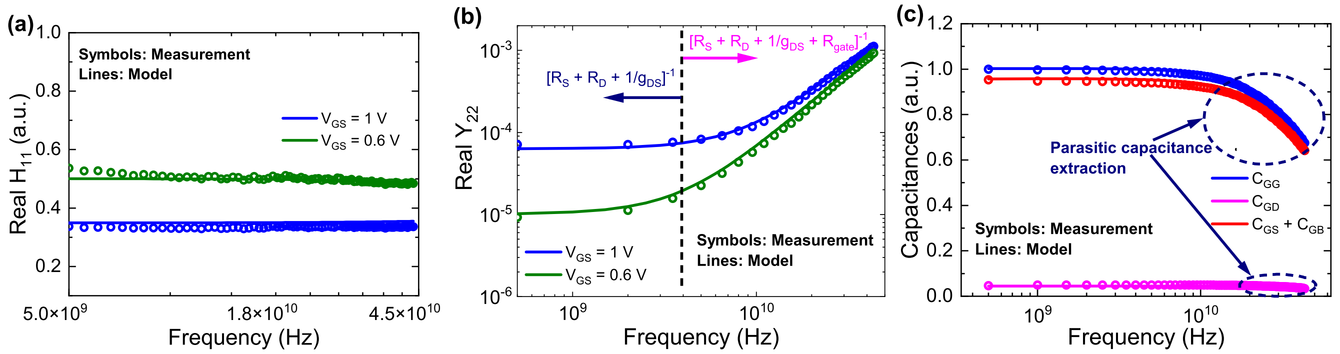

FIGURE 8. **Extracted RF characteristics of the HV FinFET: (a) Gate resistance (R_{gate}) (b) Output conductance (c) Transcapacitances variation with respect frequency at V_{DS} = 3.5 V.**

are extracted by fitting the impact of quasi-saturation. The parameters related to overlap charges are extracted from the capacitance vs. V_{GS} characteristics. The drift region of the HV device accumulates earlier compared to the inversion in the channel region, which leads to an early rise of the gate-to-drain capacitance (C_{GD}) compared to the gate-to-source capacitance (C_{GS}) as shown in [see Fig. 5(a)]. The parameter VFB is tuned to accurately capture the onset of C_{GD} rise. The parameter LOV (length of gate overlap region) is extracted by fitting the peak value of C_{GD}.

C. SMALL-SIGNAL RF MODEL EXTRACTION

The first step of the accurate RF model extraction is the development of the accurate DC model. After achieving the accurate DC model parameter set, we start extraction of the model parameters related to high frequency. The initial step in RF model extraction involves the removal of probe and pad parasitic effects from the measured S-parameters. To achieve this, we employ the conventional open-short de-embedding technique [34], resulting in de-embedded S-parameters. Key factors influencing the RF performance of transistors encompass the impact of self-heating and parasitic components, which include source-drain resistances (R_S, R_D), gate and substrate resistance, source/drain junction capacitance, intrinsic gate capacitance, overlap, and fringing capacitances. After calibrating the DC current model, we extract gate and junction capacitance across the entire frequency spectrum (500 MHz to 43.5 GHz in this work), utilizing de-embedded Y-parameters. The detailed equations for deriving the capacitances can be found in our previous work [25]. Given that R_S and R_D have already been obtained from DC model extraction, the subsequent step of RF model extraction involves the optimization of gate network parameters. At high frequencies, the capacitances linked to the gate network facilitate the propagation of the signal from the gate to the channel [see Fig. 6]. As a result, the physical gate electrode resistance (R_{gate}) is the primary component impacting the RF performance in the strong inversion regime. During the transistors' ON state, the applied RF signal at the gate terminal interacts with the inversion charge layer beneath the oxide and subsequently flows from the gate

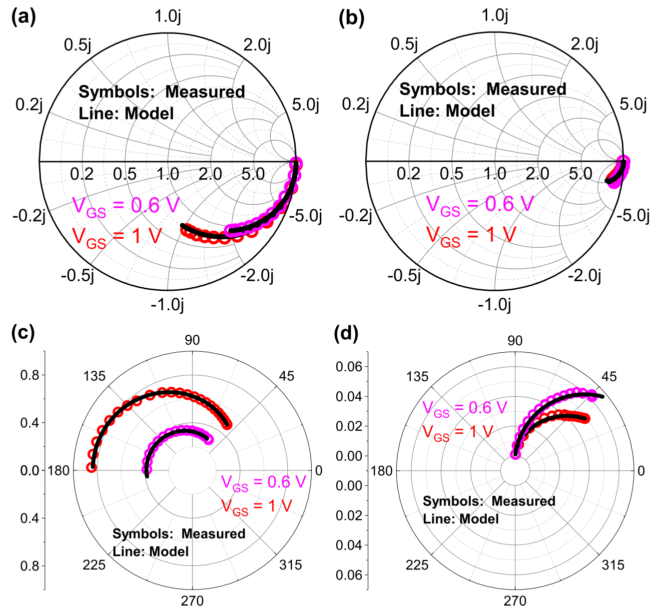

FIGURE 9. **S-parameter validation of HV device for 500 MHz to 43.5 GHz frequency range (a) S_{11}, (b) S_{22}, (c) S_{21}, and (d) S_{12} for different gate biases at V_{DS} = 3.5 V.**

toward the source and drain terminals. Consequently, the components of input and output impedance are influenced by the R_{gate}, representing the distributed resistance of the gate material along the channel [35]. As discussed earlier, the impact of R_{gate} being primarily dominant at higher frequencies, we extract the R_{gate} related model parameters by fitting the real part of H_{11} above 5 GHz. Fig. 8(a) shows that the gate electrode resistance of the HV device has been properly extracted using the BSIM-CMG. The total impedance seen from the drain terminal consists of the impact of drain resistance, channel resistance, and gate resistance.

The impact of drain and channel resistance can be observed at lower frequencies. Channel resistance is impacted by self-heating significantly. However, the impact of self-heating starts reducing with the increase in operating frequency. The frequency at which self-heating no longer

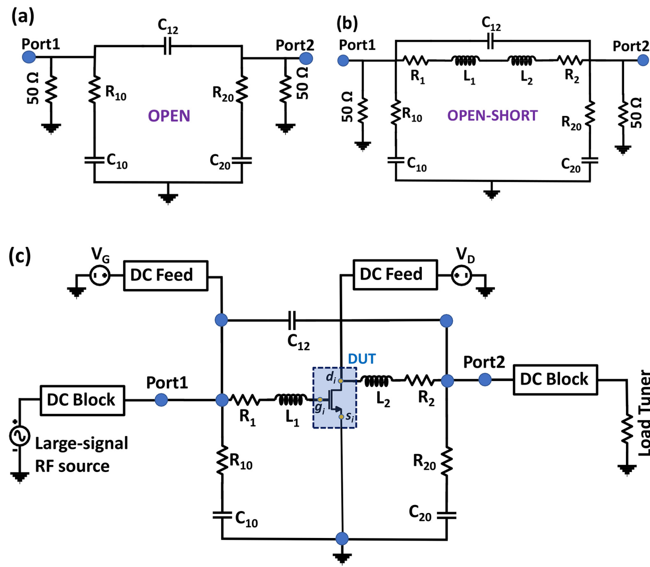

FIGURE 10. **(a) Parasitic network for the open dummy structure (b) Combined parasitic network for the open and short dummy structures. (c) The complete load-pull setup including the parasitic network.**

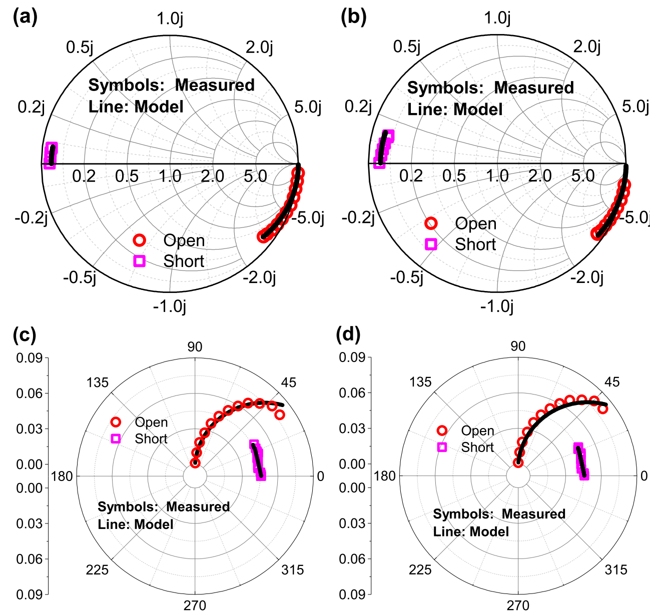

FIGURE 11. **S-parameter fitting of open and short structures of the HV FinFET for extracting parasitic network elements of large-signal analysis (a) S_{11}, (b) S_{22}, (c) S_{21}, and (d) S_{12} for different gate biases at V_{DS} = 3.5 V.**

impacts transistor characteristics is defined as the isothermal frequency (f_{iso}). The increase in output conductance (g_{DS}) beyond the f_{iso} is attributed to the impedance imposed by the gate network and modeled through the integration of gate resistance, as depicted in Fig. 8(b). The value of the R_{gate} is deduced from the Real(H_{11}) as shown in Fig. 8(a). In high-frequency modeling, the frequency dependence of capacitance is imperative for validating the accuracy of extracted parasitic capacitance

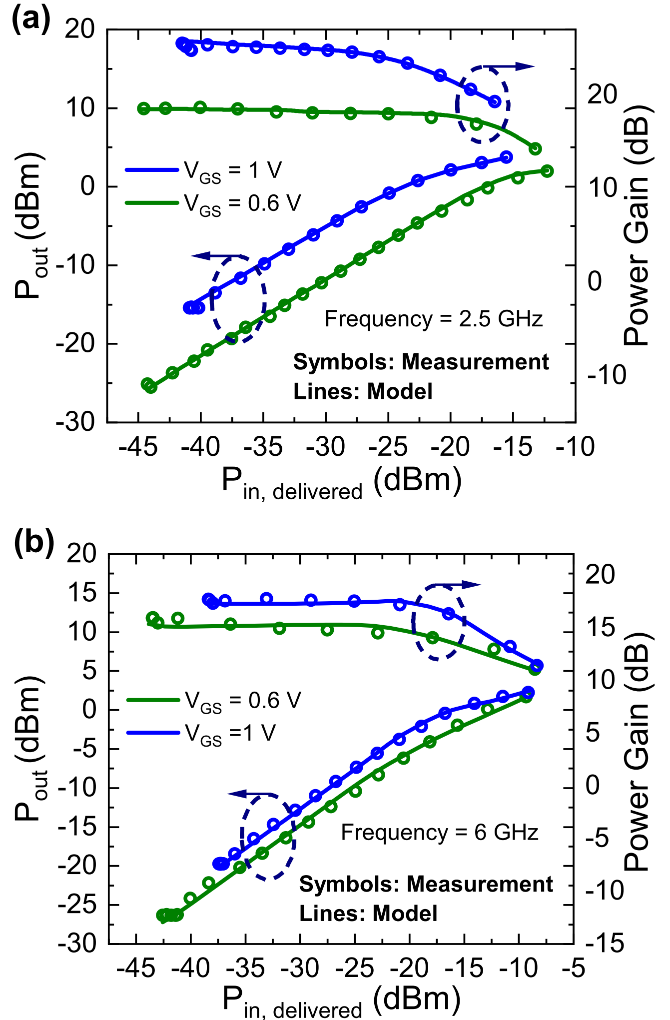

FIGURE 12. **Large-signal characteristics of the HV device at two frequencies (a) 2.5 GHz, and (b) 6 GHz. The transistor is biased at V_{DS} = 3.5 V.**

values. Junction capacitance becomes a key component as the operating frequency increases. At low frequencies, the intrinsic capacitances (C_{GSI}, C_{GDI}, and C_{GBI}) dominate the overall capacitance. However, at higher frequencies, the parasitic junction capacitances of the device dominate, as shown in Fig. 8(c). The junction and overlap capacitance parameters like CJS, CJD, ASEO, and ADEO, etc., are extracted from the high-frequency characteristics of Imaginary(Y_{12}) and Imaginary(Y_{11}) as shown in Fig. 8(c). To validate the accuracy of the modeling strategy and extracted model parameters, measured and modeled S-parameters are presented in Fig. 7 (LV devices) and Fig. 9 (HV devices). The good correlation between the simulated and measured data for both the weak and strong inversion regimes confirms the accuracy of the extracted model.

D. LARGE-SIGNAL RF MODEL EXTRACTION

To model the large-signal characteristics of the device, proper extraction of the parasitic related to pads and connections

TABLE 1. List of model parameters and extraction strategy.

Associated curves	Relevant parameters	Extraction strategy
C_{GG}, I_{DS} vs. V_{GS}	PHIG, EOT, NDEP	Extract the EOT by accurately matching the peak value of C_{GG}. Carefully tune the PHIG and NDEP to match the V_{TH} (both current and capacitance curves) at low V_{DS}.
I_{DS} vs V_{GS}	CDSC, CIT	Tune these parameters at low V_{DS} to capture the sub-threshold slope of the drain current.
I_{DS}, g_m vs. V_{GS}	U0, EU, UD, UA, ETAMOB	At moderate inversion, extract the low-field mobility (U0) by fitting the drain current at mid-V_{GS}. Extract the mobility degradation parameters (UA, UD, EU, ETAMOB) at strong inversion by the simultaneous fitting of the drain current and its slope (g_m) at high V_{GS}.
I_{DS} vs V_{GS}	RSW, RDW	Extract the source/drain resistances at strong inversion (high V_{GS}) and low V_{DS} (simultaneously optimize the mobility degradation parameters).
I_{DS} vs. V_{GS}	CDSCD, ETA0, DSUB	Optimize the DIBL parameters at weak inversion to calibrate the V_{TH} roll-off at high V_{DS} and low V_{GS}.
I_{DS}, g_m vs. V_{GS}, and I_{DS} vs. V_{DS}	VSAT1, KSATIV, VSAT, PTWG	At high V_{DS}, optimize the velocity saturation parameters VSAT1 and VSAT by simultaneously fitting the I_{DS} vs. V_{GS} and I_{DS} vs. V_{DS} curves (looking at the highest V_{GS} and V_{DS} regime). Extract the KSATIV and PTWG from I_{DS} vs. g_m plot by fitting the mid-V_{GS} and high V_{GS} regime, respectively.
I_{DS} vs. V_{DS}	MEXP, PCLM	Obtain the MEXP value by fitting the transition region between the linear and saturation region of the I_{DS} vs. V_{DS} curve. Get the PCLM value by fitting the slope of I_{DS} vs. V_{DS} curve at high V_{DS} and mid-V_{GS}.
I_{DS} vs. V_{DS}, and I_{DS} vs. V_{GS}	VDRSAT, β	Extract the drift region parameters from the high V_{GS} and mid-V_{DS} regime as explained in Section-IV(B) to capture the quasi-saturation effect.
g_m vs. I_{DS}	NDR	Tune it to capture the g_m degradation at high V_{GS} and mid-V_{DS}.
C_{GD} vs. V_{GS}	VFB, LOV	At V_{DS} = 0 V, tune VFB to capture the onset of C_{GD} rise, and tune the LOV value to calibrate the peak value of C_{GD} (as described in detail in Section-IV(B)).
C_{GS}, C_{GD} vs. V_{GS}	CGSO, CGDO, CGBO	Extract the overlap capacitance-related parameters by fitting the capacitance values at V_{GS} = 0 V and V_{DS} = 0 V.
C_{GS}, C_{GD} vs. V_{GS}	CGSL, CGDL, CFS, CFD	Extract the bias-dependent parasitics by calibrating the C_{GS} and C_{GD} vs. V_{GS} curves at higher drain biases in the high and mid-V_{GS} regime.
Re(H_{11}) vs freq.	RGATE	Get the gate resistance parameter value by fitting the Real(H_{11}) vs. frequency curve at high gate bias.
Re(Y_{22}) vs. freq.	RTH0, CTH0	Calibrate the iso-thermal frequency (f_{iso}) by accurately tuning the RTH0 and CTH0. The RTH0 value (along with RSW and RDW) is also used to capture the self-heating effect by fitting the value of Re(Y_{22}) below the f_{iso}.
C_{GS}, C_{GD}, and C_{GG} vs. freq.	CJS, CJD, ASEO, ADEO	Extract the junction parasitic-related capacitances from the capacitance vs. frequency plots at high-frequency regimes where the impact of junction capacitances dominates. The cut-off frequency is decided by the junction capacitances.

between the pads and the DUT are necessary. A lumped lossy element-based sub-circuit is designed to account for the losses in the pads and connections. The proper values of the lumped elements are extracted by fitting the measured data of the open and short dummy structures [34]. The open dummy structure can be modeled by employing lumped circuit components [see Fig. 10 (a)] that are connected in parallel to the DUT. At higher frequencies, it is important to consider the crosstalk between the G-S-G contact pads of the dummy and the coupling across the pads from port 1 to port 2. The capacitance C_{12} accounts for the interaction between pads of port-1 and port-2. The resistors R_{10} and R_{20} represent the losses incurred to the silicon substrate. The values of the capacitive and resistive components [see Fig. 10 (a)] are extracted by fitting the S-parameters of the open dummy structure as shown in Fig. 11. Once the parameters related to open structures have been extracted, it is necessary to define the parasitic components that are connected in series between the DUT and the pads. The components R_1, L_1, R_2, and L_2 represent the parasitic components that connect the pads to the DUT. In Fig. 10 (b), the values of R_{10}, R_{20}, C_{10}, C_{20}, and C_{12} are the same as that has been extracted from the open dummy. The values of series connected resistances and inductances are extracted using the S-parameter characteristics of the short dummy device [see Fig. 11]. Once all the parasitic

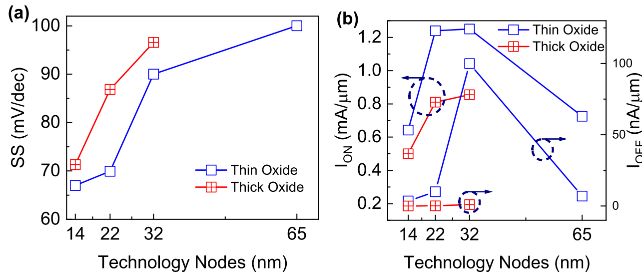

FIGURE 13. Digital performance metrics of LV-FinFETs: (a) Sub-threshold swing and (b) I_{ON} and I_{OFF} from different CMOS technology nodes [8], [36], [37].

component values are extracted, we connect the DUT to all the parasitic components and provide DC biases and large signal RF signal as shown in Fig. 10 (c). The simulation is performed using the ADS tool, and the power delivered to the load (Z_{LOAD}) is compared to the measured data. The DUT has been characterized at two frequencies (2.5 GHz and 6 GHz) for two gate biases (0.6 V and 1 V). The parasitic sub-circuit, along with the modified BSIM-CMG model for the DUT, fits the large-signal data accurately [see Fig. 12]. A detailed description of the model parameters used to calibrate the transistor characteristics and the corresponding extraction strategy is shown in Table 1.

V. PERFORMANCE METRICS

In the previous sections, we have discussed the device characterization and compact model extraction using the measured device. Next, we summarize the key performance metrics extracted from the measurement data of both LV- and HV-FinFETs.

A. LV FINFET

Fig. 13 (a) shows a continuous reduction in the sub-threshold swing with technology scaling. Thin oxide devices result in a steeper sub-threshold slope compared to the thick oxide I/O devices; this improvement in sub-threshold slope with thin oxide core devices is significantly higher in FinFET technologies. Fig. 13 (b) depicts a clear enhancement in terms of off-state performance at 14 nm FinFET technology node. However, we have observed a decrease in the ON state performance. Fig. 14 shows that a gate overdrive voltage V_{GS} - V_{TH} of 0.2 V to 0.3 V is most suited for low-power analog and RF performance due to the balanced compromise between timing and power dissipation. Fig. 14 (a) and Fig. 14(b) depict that for both thin and thick oxide LV-FinFETs maximum transconductance-efficiency (g_m/I_{DS}) is close to 25 V^{-1}. The maximum voltage gain for core devices decreases with increasing V_{GS}, while in I/O devices, it remains almost constant up to certain V_{GS} and increases at very high V_{GS}. Thick oxide I/O devices exhibit almost twice the voltage gain compared to thin oxide core devices. The improvement in the device transconductance at smaller technology nodes also leads to

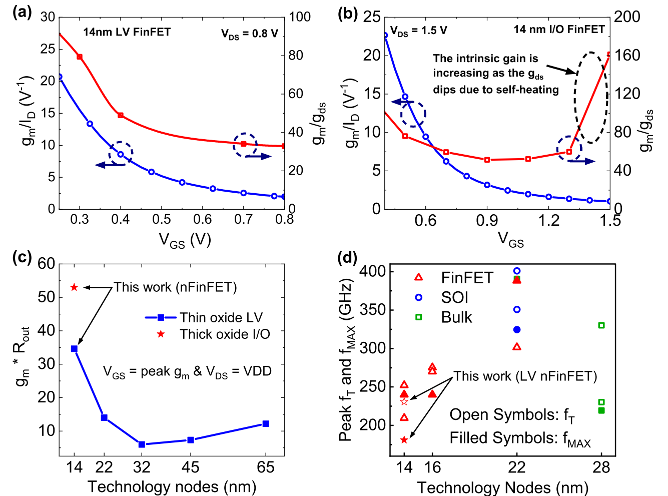

FIGURE 14. Impact of gate voltage on analog performance metrics viz. transconductance efficiency and voltage gain of 14 nm (a) LV-FinFETs and (b) I/O FinFETs. Analog and RF performance comparison of LV, I/O FinFETs for various CMOS technology nodes: (c) Voltage gain, (d) f_T and f_{MAX} [38].

an improved voltage gain. Fig. 14(c) shows the improved intrinsic gain of the device at the 14 nm technology node. The continuous reduction of metal wire width, shrinking transistor dimensions, and use of high permittivity material with each newer generation CMOS technology are causing a significant increase in the parasitic. This increase in the parasitic components severely hinders the high-frequency characteristics of the FinFET technology and results in smaller unity gain frequency (f_T) and maximum oscillation frequency (f_{MAX}) as shown in Fig. 14 (d). However, as the parasitic are highly layout-dependent, which varies from foundry to foundry; for the 16 nm and 14 nm FinFETs from various foundries, these layout-dependent parasitic result in a varying RF performance and are summarized in Fig. 14(d). From our measurements of core LV-FinFETs, we have observed the f_T and f_{MAX} of ~225 GHz and ~175 GHz, respectively.

B. HV FINFETS

Fig. 4 illustrates the characteristics of $I_{DS} - V_{GS}$ and $I_{DS} - V_{DS}$ for a 5 V HV device based on FinFET technology. This HV device exhibits peak saturated drain current ($I_{DS,sat}$) $= 647.05$ μA-μm^{-1} and linear drain current ($I_{DS,lin}$) $= 11.7$ μA-μm^{-1}. Notably, the $I_{DS,sat}$ demonstrates an enhancement of 21% compared to the 22 nm planar LDMOS technology [19]. However, due to the reduced cross-sectional area of the fins, the HV FinFET manifests an ON-state resistance $R_{DS,on} = 2.27$ mΩ-mm^2, which is relatively higher than that of the planar technology. This $R_{DS,on}$ can be mitigated by optimizing the fin structure of the extended drain region [39]. The current gain of the device has been calculated as Mag(H_{21}). The modified BSIM-CMG model is able to capture the current gain of the device accurately as shown in Fig. 15(a). The f_T has been estimated from the

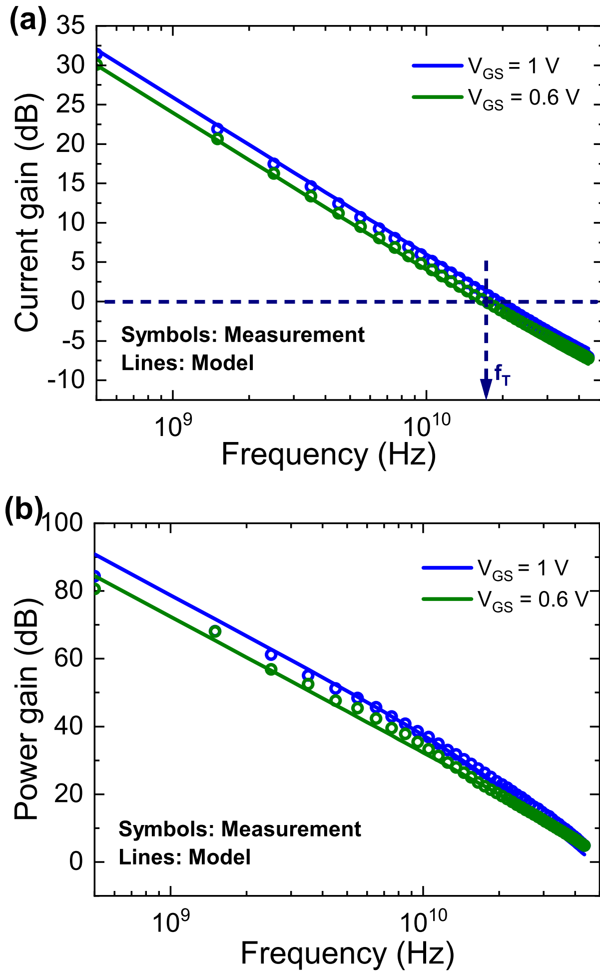

FIGURE 15. RF performance of the HV FinFET (a) Current gain [Mag(H_{21})] (b) Power gain (U) as defined using (8)at V_{DS} = 3.5 V.

TABLE 2. Comparison of different HV technologies.

Parameters	Definition	Unit	14 nm/16 nm Fin-LDMOS	22 nm planar LDMOS [19]
V_{TH}	I_{DS} = 100 nA*(W/L)	V	0.41	0.59
$I_{DS,sat}$	V_{GS} = 1.8 V & V_{DS} = 5.5 V	$\mu A - \mu m^{-1}$	647	533
$I_{DS,lin}$	V_{GS} = 1.8 V & V_{DS} = 50 mV	$\mu A - \mu m^{-1}$	11.7	36
$R_{DS,on}$	($V_{DS,lin}/I_{DS,lin}$)*W*L	$m\Omega - mm^2$	2.27	1.16
f_T	Unity current gain	GHz	19	42
f_{MAX}	Unity power gain	GHz	50	66

plot as 19 GHz. The power gain (U) has been calculated as per (8) [40]. To estimate the f_{MAX}, we have calculated the frequency at which the power gain (extrapolated) becomes unity. From Fig. 15 (b), it can be estimated that the f_{MAX} of the device is approximately around 50 GHz. Table 2 provides a comparative overview of key performance metrics for SoC-based applications for Fin-LDMOS devices at the 14/16 nm technology node (this work) in contrast to the 22 nm planar LDMOS devices.

$$U = \frac{|Y_{21} - Y_{12}|^2}{4 \cdot [Real(Y_{11}) \cdot Real(Y_{22}) - Real(Y_{21}) \cdot Real(Y_{12})]}. \tag{8}$$

VI. CONCLUSION

We have introduced advanced characterization, modeling, and parameter extraction techniques for state-of-the-art 14/16 nm LV and HV FinFETs. Notably, the industry-standard BSIM-CMG model is enhanced to incorporate HV FinFETs' drift region effects. Using the modified BSIM-CMG model, we have presented a meticulous step-by-step process for capturing the device's accurate DC and RF characteristics useful for Process Development Kit (PDK) development. We have also analyzed the device's key DC, RF, and large-signal performance indicators compared to contemporary technologies.

ACKNOWLEDGMENT

The authors would like to thank Dr. Praveen Dwivedi of Nanolab, Department of Electrical Engineering, Indian Institute of Technology Kanpur, for his help in carrying out the characterization.

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