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Compatibility of the BSIM-CMG to the Low-Frequency Noise Simulation in Subthreshold and Linear Regions of Amorphous InZnO TFTs

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ABSTRACT The compatibility of the advanced BSIM-CMG to the low frequency noise (LFN) simulation in amorphous IZO TFTs is evaluated over subthreshold and linear regions. Two kinds of devices with SiO_2-SiN_x and Al_2O_3 gate insulators are studied. In these devices, the 1/f noise is confirmed as the main component of LFN. Then the dominated origin of the 1/f noise is explained by the ΔN model in devices with SiO_2-SiN_x layers, and by the ΔN-$\Delta\mu$ model in devices with Al_2O_3 layers, respectively. Based on these models, the interficial traps density and the Hooge's parameters are further calculated, and then applied to the extraction of noise parameters ($NOIA_{eff}$, NOIB and NOIC) in BSIM-CMG. Compared to the measured data, the simulated results indicate that the noise can be well simulated by the improved BSIM-CMG both in the subthreshold and linear regions of IZO TFTs. It provides a comprehensive evaluation on the suitability of the BSIM-CMG for 1/f noise modelling in amorphous metal oxide TFTs.

INDEX TERMS InZnO, thin film transistors, low frequency noise, BSIM-CMG.

I. INTRODUCTION

Amorphous InZnO thin-film-transistors (IZO TFTs) have shown great potential to apply in flexible integrated circuits (ICs) for their low preparation temperature, reasonable electrical properties and high flexibility [1], [2]. Nevertheless, the low frequency noise (LFN) in these devices limits the functionality of the analog and even digital ICs [3]. It is necessary to study and simulate the LFN behaviors of IZO TFTs in the design process of flexible ICs.

The LFN in semiconductor devices primarily consists of thermal noise and flicker noise (1/f noise) [4], [5]. Recently, the 1/f noise has been reported as the dominant component of LFN in IZO TFTs [6], [7]. Several models are applied to simulate the 1/f noise performance in planar devices, in which the BSIM-CMG has been regarded as the industrial standard and widely used for advanced MOSFETs [8], [9], [10].

Some researchers have modeled the 1/f noise in the linear region of IZO TFTs through the BSIM3 model [6], [11]. Noise performances are in good agreement with the modeled ones in these devices. However, the suitability of the BSIM-CMG to IZO TFTs has not been studied. Additionally, 1/f noise behaviors in the subthreshold region of amorphous metal oxide TFTs are obviously different with those in c-Si MOSFETs for their structure differences [12], which has not been carefully investigated and estimated yet.

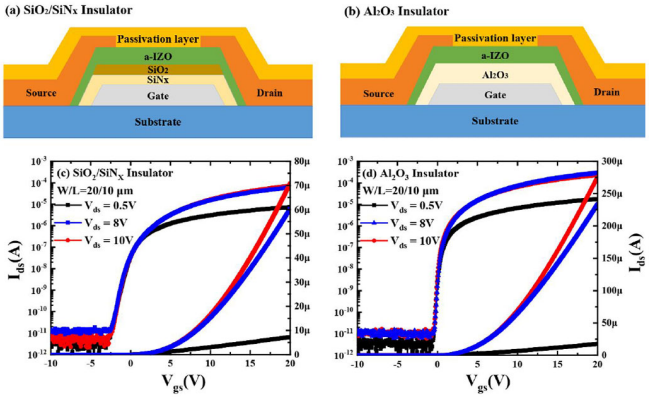

FIGURE 1. Schematic cross-sectional views of IZO TFTs with (a) SiO_2-SiN_x and (b) Al_2O_3 gate insulators, and transfer curves of IZO TFTs with (c) SiO_2-SiN_x and (d) Al_2O_3 gate insulators.

In this work, the compatibility of the BSIM-CMG on 1/f noise in IZO TFTs with different gate insulators is studied and estimated over the subthreshold and linear regions. Devices with SiO_2-SiN_x gate insulators and Al_2O_3 gate insulators are focused and marked as devices A and B, respectively. The dominated mechanism of 1/f noise is analyzed, and the noise parameters ($NOIA_{eff}$, NOIB, NOIC) in BSIM-CMG are extracted for the simulation of the noise. Finally, the noise behaviors are simulated by the BSIM-CMG, and the simulated results show good agreement with the measured ones in the subthreshold and linear regions.

II. EXPERIMENT AND I-V CHARACTERISTICS

The bottom-gate IZO TFTs with different gate insulators are shown in Fig. 1 (a)-(b). An Al layer of 300 nm was sputtered on a glass substrate and served as the gate electrode. The SiO_2-SiN_x gate insulator consisted of 50 nm SiO_2 and 250 nm SiN_x deposited by the plasma-enhanced chemical vapor deposition (PECVD) at 310°C, while the Al_2O_3 gate insulator was deposited by the anodization method with a thickness of 140 nm. Then a IZO film with the thickness of 30 nm was sputtered as the active layer. A stacked layer of Mo /Al /Mo (25 nm /100 nm/ 25nm) was deposited by the vacuum evaporation and patterned as the source or drain electrode. Finally, all devices were passivized by 300-nm-thick SiO_2 layers using the PECVD. The width and length ratio (W/L) of channels in all devices was 20 μm /10 μm.

The electrical performances and LFN of IZO TFTs were measured by the FS-pro multifunctional semiconductor parameter analyzer in a dark condition at the room temperature. The bandwidth of the noise test is 1 Hz-10 kHz and the background noise is as low as 1.0×10^{-28} A^2/Hz. Noise measurements were performed as a function of the gate voltage at V_{ds} = 0.5V. Finally, the unified model in BSIM-BULK was applied for the 1/f noise simulation in this work.

Fig. 1(c)-(d) describe the transfer curves of devices A and B with log and linear scales, and key electrical parameters are listed in Table 1. It is shown that devices B exhibit

TABLE 1. Summary of electrical parameters for IZO TFTs with different gate insulators.

Gate Insulator	V_{th} (V)	μ_{eff} ($cm^2V^{-1}s^{-1}$)	SS (V/dec)
SiO_2-SiN_x	1.2	12.13	0.605
Al_2O_3	0.8	40.29	0.184

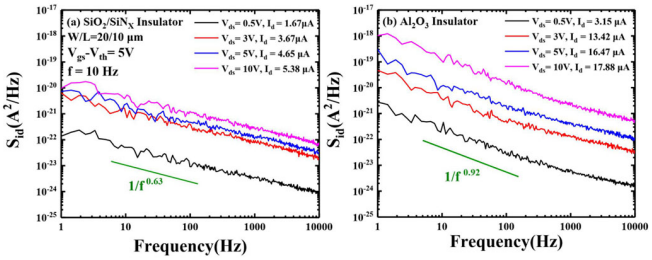

FIGURE 2. The drain current noise power spectral densities (S_{id}) versus the frequency (f) at various V_{ds} and a fixed $V_{gs}-V_{th}$ of 5V in (a) devices A and (b) devices B.

significantly higher field-effect mobility (μ_{eff}) and steeper subthreshold swing (SS) compared with devices A, indicating that the density of trap states near the IZO/SiO_2 interface is larger than that near the IZO/Al_2O_3 interface.

III. RESULTS AND DISCUSSION

A. LFN ANALYSIS IN IZO TFTS

The LFN properties in two devices are illustrated in Fig. 2. The drain current noise power spectral densities (S_{id}) versus the frequency were measured at different V_{ds} with a fixed effective gate voltage ($V_{gs}-V_{th}$ = 5V). It can be seen that S_{id} follows a 1/f $^{\gamma}$ law, indicating that the 1/f noise is the main component of LFN in IZO TFTs [13], [14]. Note that the value of γ in devices A is extracted as 0.63, while that in devices B is 0.92. The deviation of γ from 1 indicates the non-uniform oxide-trap density in energy spaces of devices A and B [6], [15]. The larger deviation of γ to 1 in devices A indicates a more non-uniform trap density in the SiO_2-SiN_x insulator compared with that in Al_2O_3 insulators.

The normalized drain current noise (S_{id}/I_d^2) versus $V_{gs}-V_{th}$ is subsequently analyzed to verify the main origin of the 1/f noise in two devices, as shown in Fig. 3. The drain voltage (V_{ds}) was set to 0.5 V, and the sampling frequency was set to 10 Hz. Theoretically, three basic models are applied to explain the 1/f noise properties in TFTs, including the carrier number fluctuation (ΔN) model [16], the mobility fluctuation ($\Delta\mu$) model [17] and the carrier number with correlated mobility fluctuation ($\Delta N-\Delta\mu$) model [16]. In the linear region of devices, the relation between S_{id}/I_d^2 and $V_{gs}-V_{th}$ is described by the ΔN model as:

$$\frac{S_{id}}{I_d^2} = \frac{k^*}{f^{\gamma} C_{ox}^2 WL\left(V_{gs}-V_{th}\right)^2} \tag{1}$$

For devices following the $\Delta\mu$ model, this relation is given by:

$$\frac{S_{id}}{I_d^2} = \frac{\alpha_H q}{f^{\gamma} C_{ox} WL\left(V_{gs}-V_{th}\right)} \tag{2}$$

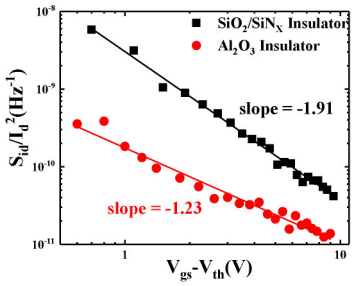

FIGURE 3. S_{id}/I_d^2 versus the effective gate voltage ($V_{gs}-V_{th}$) in devices A and devices B (V_{ds} = 0.5V, f = 10Hz).

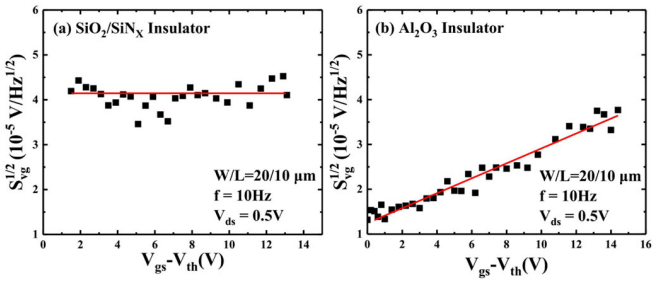

FIGURE 4. $S_{Vg}^{1/2}$ versus $V_{gs}-V_{th}$ in (a) devices A and (b) devices B in the linear region (V_{ds} = 0.5V, f = 10Hz).

TABLE 2. Summary of 1/f noise parameters for IZO TFTs with different gate insulators.

Gate Insulator	S_{Vfb}(V^2/Hz)	α_s (Vs/C)	N_t($cm^{-3}eV^{-1}$)
SiO_2-SiN_x	1.75×10^{-9}	-	3.26×10^{18}
Al_2O_3	1.78×10^{-10}	1.04×10^{5}	3.55×10^{17}

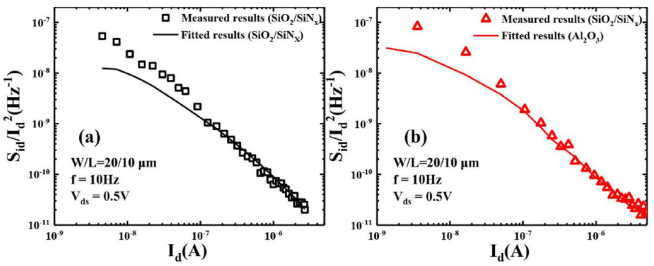

FIGURE 5. The measured and fitted results of S_{id}/I_d^2 versus I_{ds} in (a) devices A and (b) devices B (V_{ds} = 0.5V, f = 10Hz).

where k* is a constant related to the electron tunneling between traps in gate insulator and the channel, and α_H is the Hooge's parameter. Therefore, the main origin of 1/f noise can be confirmed by the slope of S_{id}/I_d^2 on $V_{gs}-V_{th}$. The 1/f noise is dominated by the ΔN model when the slope is -2, and dominated by the $\Delta\mu$ model with the slope of -1. In the middle slope range, the noise is attributed to the $\Delta N-\Delta\mu$ model [16]. In Fig. 3, the slope of S_{id}/I_d^2 on $V_{gs}-V_{th}$ approaches to -2 in devices A, which follows the ΔN model. Additionally, this slope in devices B is -1.23, closer to the prediction of $\Delta N-\Delta\mu$ model.

In devices A, the gate voltage noise spectral density (S_{Vg}) is independent on $V_{gs}-V_{th}$ and determined by the ΔN model as [16]:

$$S_{Vg} = S_{Vfb} \tag{3}$$

where S_{Vfb} is the flat band voltage spectral density. In devices B, the dependence of S_{Vg} on $V_{gs}-V_{th}$ is given by the ΔN-$\Delta\mu$ model as [16], [18]:

$$S_{Vg} = S_{Vfb}\left[1 \pm \alpha_s \mu_0 C_{ox}\left(V_{gs} - V_{th}\right)\right]^2 \tag{4}$$

where μ_0 is the low field mobility and close to μ_{eff} in the linear region, C_{ox} is the gate capacitance per unit area, and α_s is the Coulomb scattering coefficient which represents the sensibility of the mobility to the interface charges [16]. If the mobility is closely related to interface charges with a large value of α_s, the second term between brackets in Eq. (4) cannot be neglected.

For devices A following the ΔN model, the value of S_{Vfb} is determined by Eq. (3). For devices B, the plot of $S_{Vg}^{1/2}$ against $V_{gs}-V_{th}$ allows the extraction of S_{Vfb} and α_s based on Eq. (4). Fig. 4(a)-(b) depicts the plot of $S_{Vg}^{1/2}$ against $V_{gs}-V_{th}$. The intercepts of $S_{Vg}^{1/2}$ versus $V_{gs}-V_{th}$ are used to calculated the value of S_{Vfb}, while the slopes are used to calculated the value of α_s. These noise parameters in two devices are summarized in Table 2.

In devices A, the dependence of S_{id}/I_d^2 on the drain current (I_{ds}) is obtained by ΔN model as [16]:

$$S_{id}/I_d^2 = \left[g_m/I_{ds}\right]^2 S_{Vg} = \left[g_m/I_{ds}\right]^2 S_{Vfb} \tag{5}$$

While that in devices B is obtained combining Eq. (4) and Eq. (5). Fig. 5 illustrates the measured and modeled results of S_{id}/I_d^2 versus I_{ds} in devices A and B. In linear regions, the measured S_{id}/I_d^2 of devices A are well fitted by the ΔN model, while those of devices B are in good agreement with the prediction of the ΔN-$\Delta\mu$ model. which verifies the accuracy of the extraction for S_{Vfb} and α_s. Deviation occurs between the measured and modeled results in the sub-threshold regions, which may be related to the non-uniformity of trap states at the IZO/gate oxide interface.

As reported, S_{Vfb} in IZO TFTs is closely related to the density of traps (N_t) near the IZO/insulator interface and expressed as [13]:

$$S_{V_{fb}} = q^2 KTN_t\lambda / WLC_{ox}^2 f^{\gamma} \tag{6}$$

where f is the frequency, and λ is the tunneling attenuation coefficient in the gate insulators ($\sim$0.1 nm in SiO_2 and $\sim$0.11nm in Al_2O_3). Using Eq. (6), the value of N_t in these deices can be extracted. The N_t is 3.26×10^{18} $cm^{-3}eV^{-1}$ in devices A and 3.55×10^{17} $cm^{-3}eV^{-1}$ in devices B. The results depict that N_t in devices B is one order of magnitude lower than that in devices A. This result is consistent with the better electrical properties in devices B compared to devices A, including the steeper SS and high μ_{eff}.

B. NOISE PARAMETER EXTRACTION AND SIMULATION

The 1/f noise parameter in devices A and B is further simulated by the BSIM-CMG. It provides models for the 1/f

noise in the sub- and above-threshold regions of MOSFETs. The noise behaviors are commonly simulated by three noise parameters, i.e., NOIA, NOIB and NOIC [22].

i) In the subthreshold region ($V_{gs} < V_{th}$), 1/f noise is described by:

$$S_{id,sub}(f) = \frac{NOIA}{N^{*2}} \frac{kT}{\theta WLf^{\gamma}} {I_{ds}}^2 \tag{7}$$

where $N^* = \eta C_{ox}(kT/q^2)$, NOIA= N_t, and $\theta = 1/\lambda$. η is related to the SS of devices as follows [23]:

$$\eta = \frac{qSS}{ln(10)kT} = \frac{C_{ox} + C_D + C_{it}}{C_{ox}} \tag{8}$$

where C_D and C_{it} is the depletion capacitance and the interface trap capacitance per unit area, respectively. N_t in devices A and B has been listed in Table 2, and the values of NOIA in devices A and B are 3.26×10^{14} V^{-1} m^{-2} and 3.55×10^{13} V^{-1} m^{-2}, respectively.

Accounting for the non-uniform distribution of the trap states at the interface, the effective trap density parameter $NOIA_{eff}$ is obtained by [10]:

$$NOIA_{eff} = NOIA * \max\left(1, f_{eff}\right) \tag{9}$$

where f_{eff} is the non-uniform distribution function and given as:

$$f_{eff} = \frac{NOIA2/NOIA}{1 + (Q_{ch}/QSREF)^{MPOWER}} \tag{10}$$

where Q_{ch} is the charge in the channel. QSREF and MPOWER are charge and slope parameters at the threshold condition, which govern the shape of f_{eff} [10]. The value of Q_{ch} is extracted as follows. In the subthreshold region, I_{ds} can be modeled as [24], [25]:

$$I_{ds} = I_{ds0} \exp\left(\frac{|V_{gs} - V_{th}|}{m(V_{gs})V_T}\right) \tag{11}$$

where V_T is the thermal voltage, I_{ds0} is the threshold drain current at $V_{gs} = V_{th}$, and $m(V_{gs})$ is the ideality factor experimentally obtained by [24]:

$$m(V_{gs}) = \left(\frac{V_{gs2} - V_{gs1}}{V_T}\right) \Big/ \ln\left(\frac{I_{ds2}}{I_{ds1}}\right) \tag{12}$$

where I_{ds1} and I_{ds2} are the drain currents corresponding to two similar gate voltages (V_{gs1} and V_{gs2}). Referred to [24], [25], the $m(V_{gs})$ under subthreshold operation can also be described as:

$$m(V_{gs}) = 1 + \frac{1}{\psi_s(V_{gs})} \cdot \frac{Q_{ch}}{C_{ox}} \tag{13}$$

where ψ_s is the surface potential and given by:

$$\psi_s(V_{gs}) = \frac{1}{V_{gs2} - V_{gs1}} \int V_T \ln\left(\frac{I_{ds2}}{I_{ds1}}\right) dV_{gs} \tag{14}$$

Using Eq. (14) and (15), the Q_{ch} in the subthreshold region can be obtained, as shown in Fig. 6.

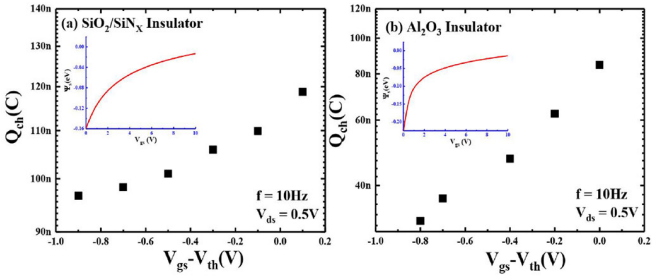

FIGURE 6. The extracted Q_{ch} and ψ_s (inset figure) versus $V_{gs}-V_{th}$ in (a) devices A and (b) devices B (V_{ds} = 0.5V, f = 10Hz).

TABLE 3. Summary of noise parameters in BSIM-CMG for IZO TFTs with different gate insulators.

Gate Insulator	NOIA ($cm^{-3}eV^{-1}$)	NOIA2 ($cm^{-3}eV^{-1}$)	QSREF(C)	MPOWER
SiO_2-SiN_x	3.26×10^{18}	4.96×10^{19}	7.6×10^{-8}	8.9
Al_2O_3	3.55×10^{17}	7.81×10^{18}	2.9×10^{-8}	6.0

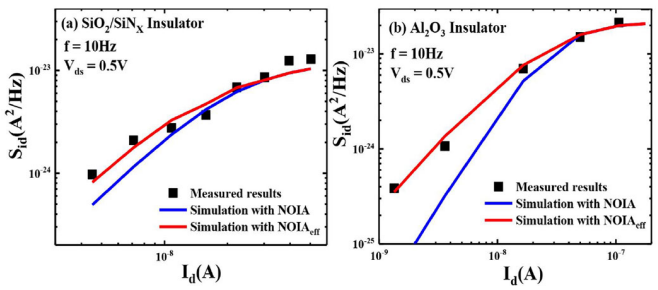

FIGURE 7. Measured and simulated results of S_{id} in the sub-threshold region of (a) devices A and (b) devices B (V_{ds} = 0.5V, f = 10Hz).

To ensure the continuity between the simulated results in sub- and above threshold region, 1/f noise is expressed as:

$$S_{id}(f) = \frac{S_{id,sub}(f)S_{\lim}(f)}{S_{id,sub}(f) + S_{\lim}(f)} \tag{15}$$

where $S_{lim}(f)$ is the 1/f noise calculated at $V_{gs}-V_{th} = 0.1V$.

According to Eq. (8), (10) and (16), the 1/f noise behaviors in the subthreshold region of devices A and B have been simulated using the NOIA and $NOIA_{eff}$. All BSIM-CMG parameters in this region are listed in Table 3 for two devices.

Fig. 7 depicts the experimental and simulated results of two devices at V_{ds}=0.5V in the subthreshold region. The simulated noise using NOIA is smaller than the measured data in all devices, while that using $NOIA_{eff}$ is in good agreement with the measured one. This indicates that the extra noise under the subthreshold operation is closely related to the non-uniform trap distribution near the IZO/gate insulators interface [10]. In this case, the improved BSIM-CMG is suitable for the simulation of 1/f noise in IZO TFTs.

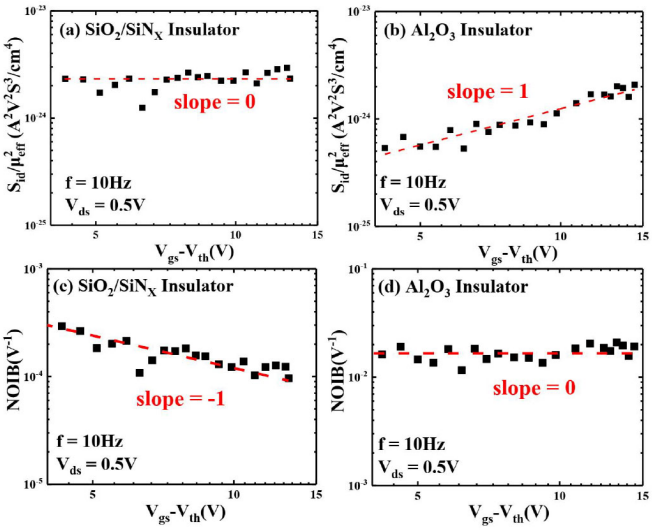

FIGURE 8. The dependence of S_{id}/μ_{eff}^2 on $V_{gs}-V_{th}$ in (a) devices A and (b) devices B, and variation of the parameter NOIB versus $V_{gs}-V_{th}$ in (c) devices A and (d) devices B in the deep linear region (V_{ds} = 0.5V, f = 10Hz).

ii) Above threshold ($V_{gs}-V_{th}$>0.1 V), 1/f noise can be expressed as:

$$S_{id}(f) = \frac{qkT\mu_{eff}I_{ds}}{C_{ox}L^2f^{\gamma}}\left[NOIA_{eff}\log\left(\frac{N_0+N^*}{N_L+N^*}\right) + NOIB(N_0-N_L) + \frac{NOIC}{2}\left(N_0^2-N_L^2\right)\right] + \Delta L_{clm}\frac{kTI_{ds}^2}{qWL^2f^{\gamma}}\frac{NOIA_{eff}+NOIBN_L+NOICN_L^2}{(N_L+N^*)^2} \quad (16)$$

with $qN_0 = C_{ox}(V_{gs}-V_{th})$, $qN_L = C_{ox}(V_{gs}-V_{th}-\min(V_{ds}, V_{dsat}))$.

As reported, the value of NOIC is negligible in all biases of CMOS transistors [26] and ΔL_{clm} is the channel length reduction due to channel length modulation in the saturation region.

In the linear region ($V_{gs}-V_{th}>V_{ds}$), $N_0-N_L=(C_{ox}/q)V_{ds}$ and $\Delta L_{clm}=0$. Additionally, Eq. (17) can be modified as:

$$S_{id}(f) = \frac{qkT\mu_{eff}I_{ds}}{C_{ox}L^2f^{\gamma}}\left[NOIA_{eff}\log\frac{C_{ox}(V_{gs}-V_{th})+qN^*}{C_{ox}(V_{gs}-V_{th}-V_{ds})+qN^*} + NOIB\frac{C_{ox}}{q}V_{ds}\right] \quad (17)$$

In the deep linear region of $V_{gs}-V_{th} >> V_{ds}$, Eq. (18) can be approximated as:

$$S_{id}(f) = \frac{kT\mu_{eff}^2W}{L^3f^{\gamma}}C_{ox}V_{ds}^2\cdot NOIB\cdot\left(V_{gs}-V_{th}\right) \quad (18)$$

The value of NOIB is estimated by:
For devices following the $\Delta\mu$ model,

$$NOIB = \frac{q}{kT}\alpha_H \quad (19)$$

For devices following the ΔN model,

$$NOIB = \frac{k^*}{kTC_{ox}}\frac{1}{\left(V_{gs}-V_{th}\right)} \quad (20)$$

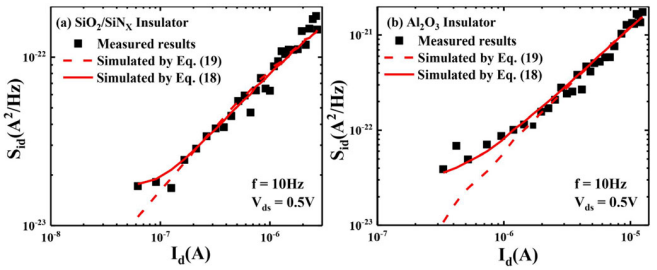

FIGURE 9. Measured and simulated results of S_{id} in the linear region of (a) devices A and (b) devices B (V_{ds} = 0.5V, f = 10Hz).

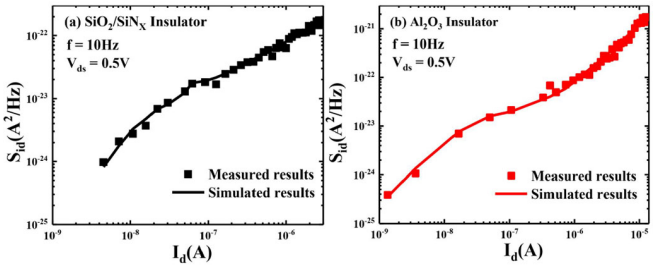

FIGURE 10. Measured and simulated results of S_{id} in the subthreshold and linear regions of (a) devices A and (b) devices B (V_{ds} = 0.5V, f = 10Hz).

Hence, the value of NOIB can be confirmed by the dependence of S_{id}/μ_{eff}^2 and $V_{gs}-V_{th}$ in the deep linear region, which is illustrated in Fig. 8.

In devices A, S_{id}/μ_{eff}^2 is independent on the $V_{gs}-V_{th}$ and follows the prediction of the ΔN theory. Consequently, NOIB parameters are described by Eq. 20 and vary as $(V_{gs}-V_{th})^{-1}$. Results are depicted in Fig. 8(c), and the constant k* in Eq. 20 is calculated as 1.96×10^{-29} $A^2V\cdot S^2/cm^2$. In devices B, S_{id}/μ_{eff}^2 is proportional to $V_{gs}-V_{th}$, showing a $\Delta\mu$ origin of the 1/f noise. The NOIB parameters are obtained by Eq. (20) and exhibit in Fig. 8(d). The average value of α_H is extracted as 4.78×10^{-4} using the method reported in [11]. It shows that NOIB is independent on $V_{gs}-V_{th}$ with a value of $0.017V^{-1}$. These results are consistent with the analysis in Section III-A.

Using the extracted NOIA and NOIB, the 1/f noise in devices A and B is simulated by the BSIM-CMG and compared with measured data in the linear region, as shown in Fig. 9. It can be seen that the measured noise is well simulated by Eq. (18) and (19) in the linear region, which indicates the great compatibility of BSIM-CMG on the 1/f noise simulation in IZO TFTs whether the noise follows the ΔN model or the $\Delta\mu$ model.

Finally, the simulated and measured S_{id} versus I_{ds} has been illustrated in Fig. (10). Simulation results are in good agreement with measured data, showing the possibility to predict 1/f noise in metal oxide TFTs by the BSIM-CMG model under the subthreshold and linear operations.

IV. CONCLUSION

Herein, the compatibility of the advanced BSIM-CMG to LFN in amorphous IZO TFTs was evaluated in all

operation regions. Two kind of devices which have SiO_2-SiN_x or Al_2O_3 gate insulators are studied. Firstly, the main component of LFN in these devices was confirmed to be the 1/f noise. Subsequently, the dominated mechanism of the 1/f noise in the linear region was explained by the ΔN model in devices A, and by the ΔN-$\Delta\mu$ model in devices B. Some key noise parameters, such as the interficial traps density (N_t) and the Hooge's parameters (α_H), were further calculated. These results were applied for the extraction of NOIA and NOIB parameters. Simulated noise was then compared to the measured one in all operating regions. We found that deviations occurred in the subthreshold region in two devices simply using a NOIA parameter due to the extra noise induced by the non-uniform trap distribution near the IZO/gate insulators interface. Based on an improved BSIM-CMG, the measured results can be well simulated by the NOIA and a non-uniform distribution function f_{eff}. Additionally, good agreements between the simulated and measured results are observed in the linear region of two devices. As a consequence, the BSIM-CMG noise model is suitable for amorphous IZO TFTs in the subthreshold and linear regions.

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