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OLED Microdisplay With Monolithically Integrated CAAC-OS FET and Si CMOS Achieved by Two-Dimensionally Arranged Silicon Display Drivers

MUNEHIRO KOZUMA[1], YUSUKE KOMURA[1], SHOKI MIYATA[1], YUKI OKAMOTO[1], YUKI TAMATSUKURI[1], HIROKI INOUE[1], TOSHIHIKO SAITO[1], HIDETOMO KOBAYASHI[1], TATSUYA ONUKI[2], YUICHI YANAGISAWA[2], TOSHIHIKO TAKEUCHI[2], YUTAKA OKAZAKI[2], HITOSHI KUNITAKE[3] (Member, IEEE), DAIKI NAKAMURA[3], TAKAAKI NAGATA[4], YASUMASA YAMANE[4], MAKOTO IKEDA[5] (Senior Member, IEEE), AND SHUNPEI YAMAZAKI[6] (Life Fellow, IEEE)

1 CAD Division, Semiconductor Energy Laboratory Company Ltd., Atsugi 243-0036, Japan
2 NOS Development Division, Semiconductor Energy Laboratory Company Ltd., Atsugi 243-0036, Japan
3 Equipment Division, Semiconductor Energy Laboratory Company Ltd., Atsugi 243-0036, Japan
4 OEL Division, Semiconductor Energy Laboratory Company Ltd., Atsugi 243-0036, Japan
5 Systems Design Lab, School of Engineering, The University of Tokyo, Tokyo 113-0032, Japan
6 Semiconductor Energy Laboratory Company Ltd., Atsugi 243-0036, Japan

CORRESPONDING AUTHOR: M. KOZUMA (e-mail: mk0920@sel.co.jp)

ABSTRACT We developed an organic light-emitting diode (OLED)/oxide semiconductor (OS)/silicon (Si) display in which Si CMOS display drivers can be arranged two-dimensionally by monolithically stacking *c*-axis-aligned crystalline oxide semiconductor (CAAC-OS) FETs over Si CMOS. A CAAC-OS FET exhibits a higher withstand voltage than a SiFET of the same size, enabling considerable pixel area reduction. The CAAC-OS FET can be driven even at a low refresh rate owing to its extremely low off-state current, making it an ideal choice for constructing pixel circuits. This integration of CAAC-OS FETs empowers our display system to offer enhanced resolution and reduced power consumption. The two-dimensionally arranged drivers have two features. (1) Si drivers can be arranged in two-dimensional driver blocks with a desired size, which provides flexibility to increase the number of driver stages and adjust resolution and frame rates for each driver block via logic processing. (2) The circuit performance of the system can be changed to prioritize frame rate and power consumption, which have a trade-off relation, of the driver by providing a redundant circuit in the driver. To demonstrate these features, we fabricated a prototype display and confirmed that our driver had a power consumption of 1,094.96 mW at 30 Gbps in a normal mode and 524.55 mW at 3.75 Gbps in a foveated rendering (FR) mode, revealing a 52% reduction in power consumption in the FR mode. This technology is expected to achieve high-frame-rate performance, which has been difficult to achieve in conventional microdisplays.

INDEX TERMS CAAC-OS, Si CMOS, driver, microdisplay, high frame rate, and foveated rendering.

I. INTRODUCTION

As technology advances, extended reality (XR) expands its application range into diverse fields, such as gaming and medicine. This dynamic growth is anticipated to drive the market of XR displays. In virtual reality (VR) displays used as head-mounted devices, phenomena that cause discomfort to users, such as a screen-door effect, have been reported [1], [2]. To relieve such discomfort and deliver more realistic images, the demand for high resolution and frame rates have surged. However, the pursuit of enhanced performance in displays is not without its challenges, as it often comes at the cost of performance degradation and increased power consumption, which are caused by the high resolution of displays [3]. General microdisplays have an

organic light-emitting diode (OLED)/silicon (Si) structure, where pixel arrays and display drivers are embedded within a Si layer, placing the display drivers at the periphery of the pixel arrays [4], [5]. Thus, this pixel circuit configuration has been designed for high resolutions [6], [7], [8]. However, high resolutions require many parallel amplifiers because of the inherent limitations in amplifier response speed, while the area restriction of the Si layer limits the number of source lines that can be simultaneously driven. This creates a problem, as amplifier response speed cannot keep up with increasingly demanding frame rates [9]. Moreover, VR display systems encounter another problem: an enormous amount of video data required for 360° streaming at high resolutions and frame rates [10]. This places a heavy load on the drawing processing IC such as a GPU, ultimately reducing frame rate of the drivers. In response, a solution has emerged as foveated rendering (FR) using human visual characteristics to reduce the load on drawing processing software [10], [11], [12], [13], [14].

Employing *c*-axis-aligned crystalline oxide semiconductor (CAAC-OS) FETs in a pixel circuit is also known as a method for increasing display resolution. For example, a display with a resolution of 5,000 ppi or more has been achieved using CAAC-OS FETs [15]. Furthermore, an OLED display has been proposed, incorporating an OLED/oxide semiconductor (OS)/Si structure, where a pixel circuit formed using CAAC-OS FETs is monolithically stacked over a driver circuit built using SiFETs. These propositions take an advantage of the superior withstand voltage of CAAC-OS FETs over SiFETs, which enables performance suitable for fine pixels [16], [17], [18].

II. OS/SI MONOLITHIC ARCHITECTURE

Fig. 1 is a cross-sectional image of an OS/Si stacked process structure. A CAAC-OS FET formed using a CAAC-OS process with a minimum process feature size of 360 nm is monolithically stacked over a wiring and SiFET formed using a Si CMOS high-voltage (HV) process with a minimum process feature size of 55 nm.

Fig. 2(A) is a circuit diagram of a subpixel formed using CAAC-OS FETs with the minimum size of channel width (W)/channel length (L) = 360 nm/360 nm. Fig. 2(B) is a timing chart of the subpixel. Video potentials of 2.5–4 V supplied from a source driver output SL are written to a gate (N1) of a transistor M2 through a transistor M1. Gate selection signals of 6 and 0 V supplied from a gate driver output GL control the writing of transistors M1 and M3. The ability to modulate the current supply (I_d) for the OLED through the transistor M2 provides precise control over OLED luminance. Thus, the I_d–drain voltage (V_d) saturation characteristics of the transistor M2 are important to maintain consistent luminance of the OLED, even when source–drain voltage (V_{ds}) of the transistor M2 fluctuates owing to variation or degradation of the OLED characteristics. At the time of light emission, the potential of a node N2 between M2 and the OLED increases in response to a current flowing through M2. In proportion to this potential increase of N2, the potential of N1 increases owing to capacitive coupling through a storage capacitor C1 between N1 and N2. Notably,

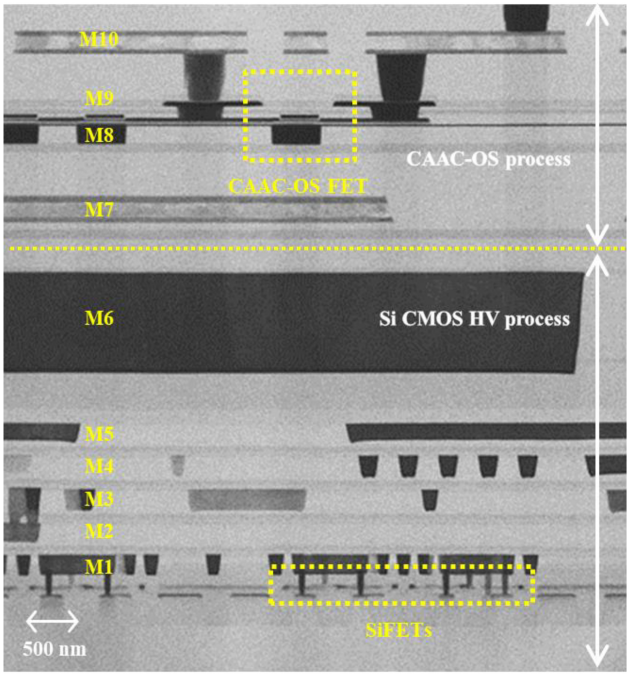

FIGURE 1. Cross-sectional scanning transmission electron microscope image of OS/Si monolithic stack.

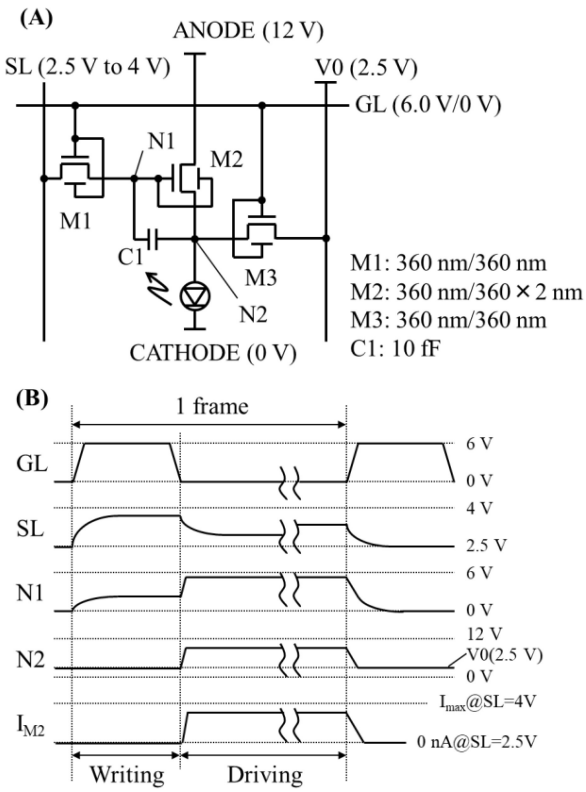

FIGURE 2. (A) Schematic representation and (B) timing chart of the pixel circuit (three CAAC-OS FETs and one capacitor).

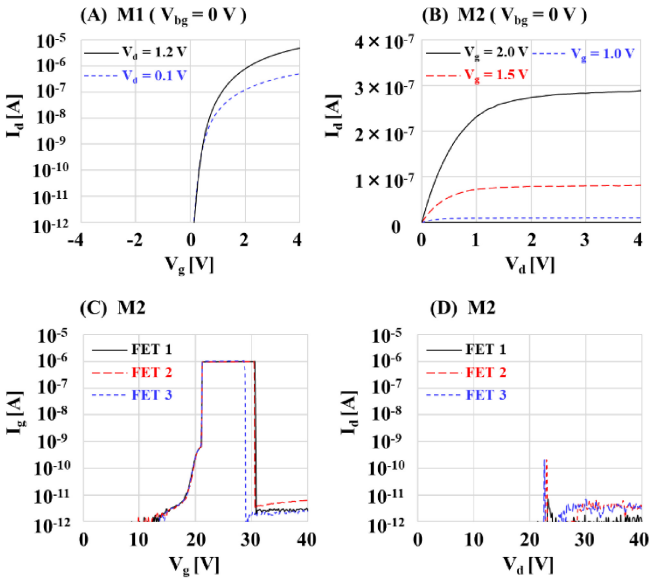

FIGURE 3. Characteristics of CAAC-OS FET: (A) I_d–V_g, (B) I_d–V_d, (C) V_g withstand voltages of three FETs, and (D) V_d withstand voltages of three FETs.

the transistor M3 supplies a reset voltage (V0) of 2.5 V in writing a video signal. The pixel circuit composed of three subpixels has a size of 7.92 × 7.92 μm^2. To display an image of D65 white light at 5,000 cd/m^2 on the prototyped OLED display, a voltage difference of ∼12 V must be applied between the anode and the cathode, where the driving transistor M2 of the pixel circuit is connected in series.

Figs. 3(A)–(D) show the characteristics of the CAAC-OS FET with W/L = 360 nm/360 nm during monolithic stacking of the Si CMOS. As shown in Figs. 3(C) and (D), the CAAC-OS FET exhibits a withstand voltage of ≥10 V in gate voltage (V_g) and V_d. Additionally, the CAAC-OS FET has excellent charge retention characteristics [19]. The use of a write transistor capable of retaining a video potential can reduce the refresh rate of the driver, even with a pixel capacity of 10 fF (a designed value). For example, achieving a refresh rate as low as 1 fps while ensuring potential fluctuations remain within a range of 1 mV or lower requires an off-leakage current of ≤10 aA (= 1 × 10^{-17} A). A SiFET cannot satisfy such a small off-leakage current, making it unable to reduce the refresh rate like the CAAC-OS FET.

As shown in Fig. 4, the monolithic OS/Si stack introduces a novel structure and function different from conventional configurations.

Conventional microdisplays with the OLED/Si structure necessitate the integration of pixel arrays and display drivers within a Si CMOS layer. In such a structure, the display drivers can be formed only at the periphery of the pixel arrays, consequently limiting the potential for increased resolution and frame rates owing to circuit area constraints.

In contrast, microdisplays with the OS/Si structure only house display drivers in the Si CMOS layer, allowing pixel arrays to be formed in a CAAC-OS layer positioned over

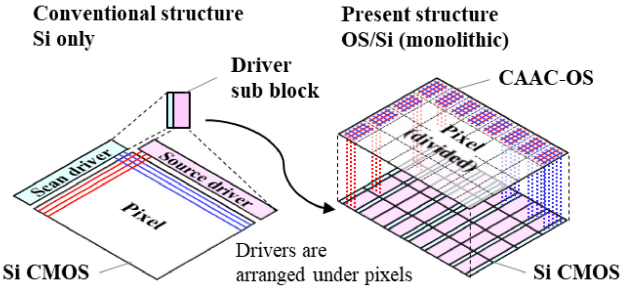

FIGURE 4. Schematic representation of display drivers in OS/Si structure.

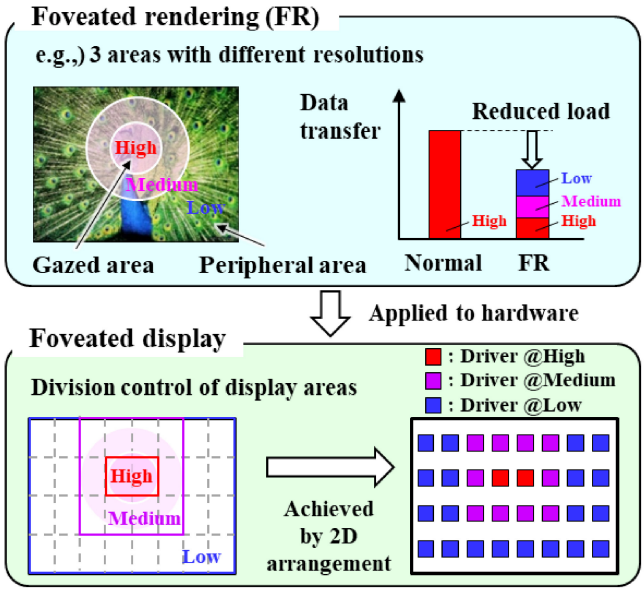

FIGURE 5. The schematic representation of 2D drivers for foveated rendering.

the Si CMOS layer. The arrangement of the two-dimensional display drivers below the pixel arrays enables designing functionalities such as independent control of multiple driver sub blocks, taking advantage of the large-area Si CMOS layer. This design improves the driver performance required for achieving high resolutions and frame rates.

III. OS/SI DISPLAY DRIVER ARCHITECTURE

The display with the OS/Si structure has the following two features:

A. CONTROLLABILITY OF RESOLUTION AND FRAME RATE FOR EACH DRIVER

Fig. 5 shows that foveated rendering (FR) is a method that processes drawing at a high resolution in the gazed area and a low resolution in the peripheral area. A VR system can detect a gazed area in real time using eye tracking, which reduces the amount of data processed by the system without compromising the display quality [20]. To introduce an FR-like function into hardware, we propose a structure where a display control area is divided using the two-dimensionally arranged display drivers. This arrangement reduces the resolution in areas other than the gazed area,

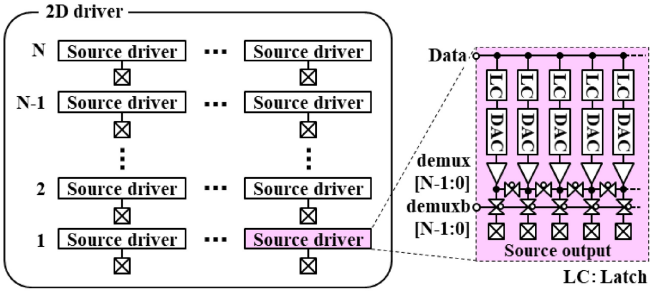

FIGURE 6. 2D driver example.

which does not affect visual recognition by the user, thereby reducing the data requirements for display. In other words, this approach reduces the processing load on the entire display system, including drivers and control ICs such as the GPU. Although only the resolution is a processing target in a general FR, our structure is designed to allow real-time alteration of resolution and frame rate in any divided area on a frame basis. This adaptability is enabled through the low off-state current of the CAAC-OS FET.

B. CHANGEABILITY OF THE DRIVER CIRCUIT PERFORMANCE

Fig. 6 shows the proposed source driver that can switch its circuit performance when divided into N segments along the source line. When the number of output signals is constant, the circuit performance of the proposed driver is determined based on the priority between frame rate and power consumption, recognizing their trade-off relation.

Fig. 7 shows an example of the driver divided into four segments ($N = 4$). With reference to a nondivided Si driver, when a high frame rate is prioritized over power consumption, increasing the total number of amplifiers by N times can increase the frame rate by N times while increasing the power consumption by N times. In contrast, when low power consumption is prioritized, an output signal from one amplifier is distributed across N source lines using a demultiplexer (demux) without changing the total number of amplifiers. In this step, the source line is divided into N segments, reducing gate scanning by a scan driver in one frame to $1/N$, consequently extending the gate selection period by N times. At this time, the writing time for one source line is equal to that of the case of the nondivided Si driver, which allows operation with substantially the same power consumption of the amplifier and frame rate as when the source line is not divided.

Dividing the driver along the gate line to increase the number of scan drivers enables independent control of the resolution and frame rate of the driver. The scan driver, which has a simple circuit configuration, has much lower power consumption and a much smaller circuit area than the source driver. As a result, even when divided, the scan driver has a minimal impact on the circuit performance of the entire display driver.

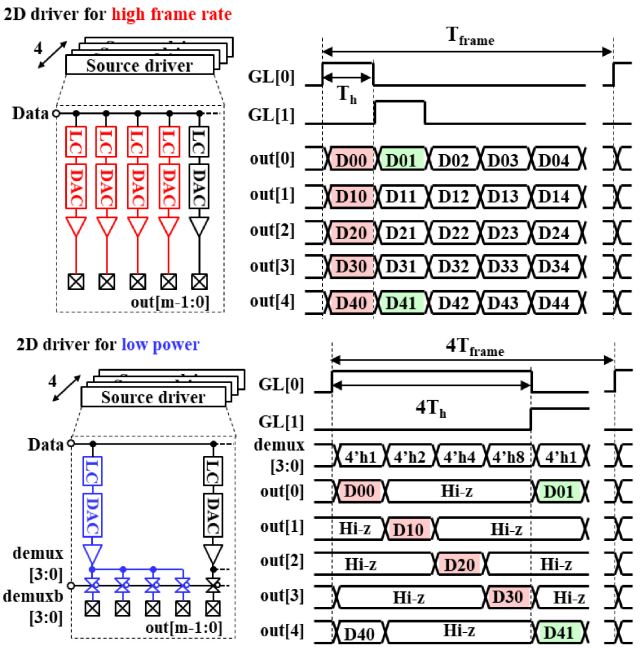

FIGURE 7. 2D driver configurations and timing charts ($N = 4$, high frame rate and low power consumption).

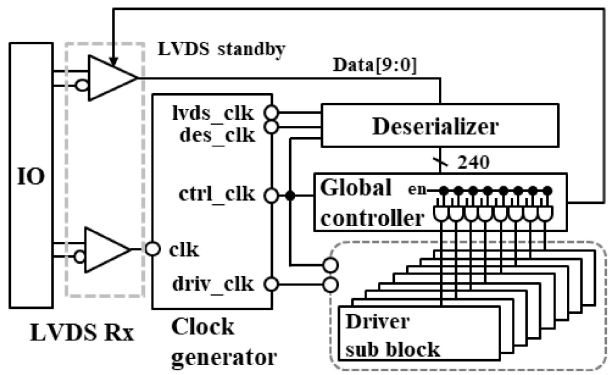

FIGURE 8. Schematic representation of a Si driver block.

IV. DISPLAY DRIVER DESIGN

The circuit configuration of a display driver incorporating the proposed structure is shown below.

A. DISPLAY DRIVER CONFIGURATION

Fig. 8 is the circuit diagram of a Si driver block, while Fig. 9 is a circuit diagram of a driver sub block. The Si driver block mainly comprises an input/output interface (IO), a low-voltage differential signaling receiver (LVDS Rx), a clock generator, a deserializer, a global controller, and eight driver sub blocks. The driver sub block shown in Fig. 9 includes a source driver, a scan driver, an SRAM, and a local controller for controlling them to allow adjustable resolutions and frame rates.

As shown in Fig. 10, the incorporated SRAM functions as a buffer memory for adjusting the timing of image data input to the driver and the timing of image data output to

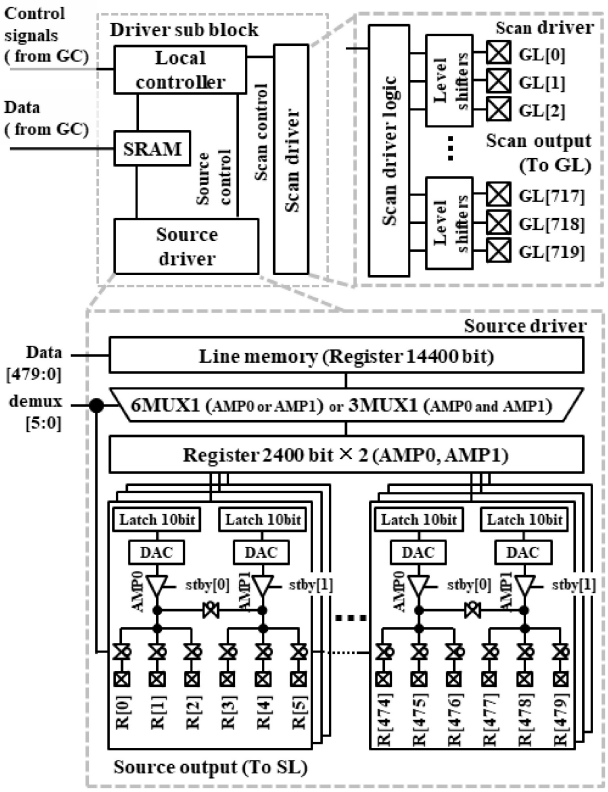

FIGURE 9. Schematic representation of a driver sub block.

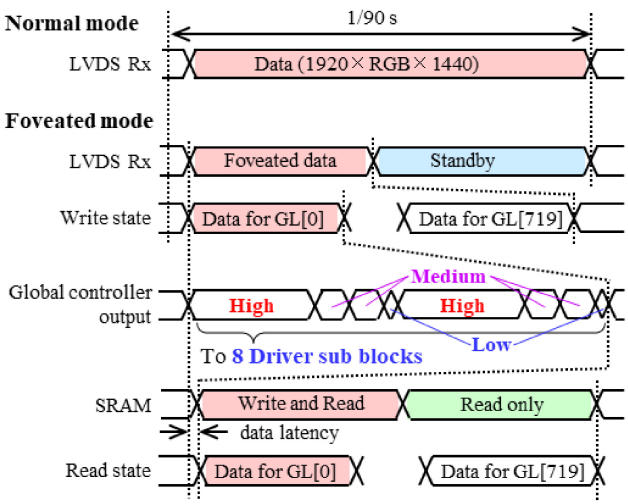

FIGURE 10. Timing chart for Si driver block.

the pixel circuit when data transfer is reduced in the FR mode. In this setup, the source and gate drivers are controlled synchronously using a local controller for each divided display area. The data for one horizontal period is initially stored in a line memory of 14,400 bits and subsequently output to the source line with configurations of 4,800 bits in a 3MUX1 mode and 2,400 bits in a 6MUX1 mode, following demux selection. Given the sequential transfer of data for one horizontal period to the eight driver sub blocks by the

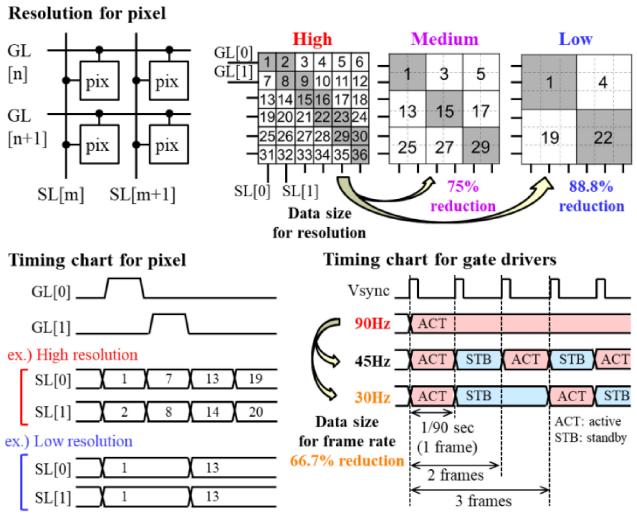

FIGURE 11. Methods for controlling resolution and frame rate.

global controller, gate lines experience a time lag relative to data transfer completion.

B. OPERATION FOR CONTROLLING RESOLUTION AND FRAME RATE

Fig. 11 shows a method for controlling the resolution and frame rate of the display driver. The resolution can be changed to three levels: high, medium, and low. A low resolution is achieved by supplying the same source data to adjacent pixels of the same color. In practical terms, this means that data for one pixel in a normal operation (high resolution) is distributed to 2 × 2 pixels (medium resolution) or 3 × 3 pixels (low resolution). This method effectively reduces the data volume by 75% and 88.8% for the medium and low resolutions, respectively. This reduction in incoming data allows the LVDS Rx to enter a standby mode, consequently reducing its constant current consumption.

In addition, reducing the frame rate and resolution effectively reduces data volume. When the frame rate of the scan driver is reduced from 90 to 45 and 30 Hz, the amount of data transfer can be reduced to 50% and 33.3%, respectively. The ability of CAAC-OS FET to retain data potential written to the pixel circuit owing to the extremely low off-state current characteristics ensures that the display remains stable even when the rewriting frequency is reduced. Moreover, during a period with no rewriting, the output of the source driver is unnecessary, enabling the suspension of data processing circuits such as the LVDS Rx and the amplifier, thus saving power. These control operations can be achieved by rewriting register parameters during a retrace period just before the beginning of a frame. On each of the 32 divided areas, real-time control can be performed in each frame with a combination of any of the three-level resolutions and a freely set frame rate.

Such a display function with changeable resolution and frame rate facilitates the FR mode operation, where a gazed

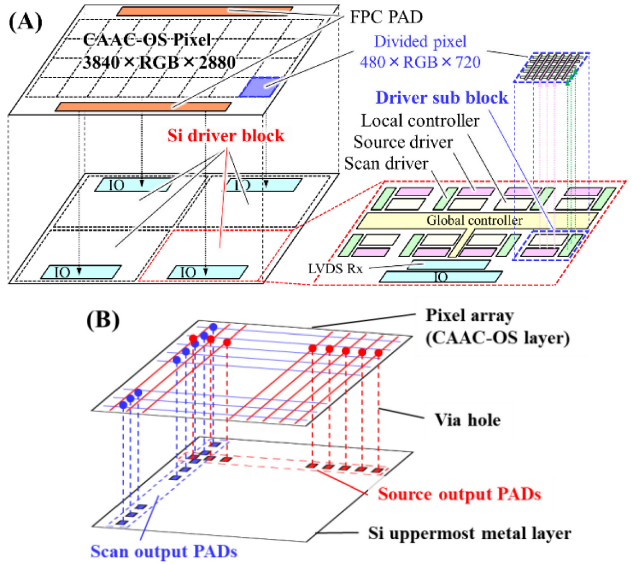

FIGURE 12. **(A) Circuit configuration of a prototype display (B) diagram showing connection of driver outputs and control signal lines in divided pixels (480 × 720).**

(fovea) area operates at a high resolution, while a nongazed (peripheral visual field) area operates at a low resolution, optimizing both performance and energy efficiency.

V. DISPLAY DESIGN

To confirm the display function achieved by the OS/Si structure, we prototyped an OLED/OS/Si display (Fig. 12(A)). Using the shot size of the Si process, we fabricated a 1.5-inch microdisplay with a resolution of 3,840 × RGB × 2,880 and a pixel density of 3,207 ppi. For independent control by two-dimensionally arranged driver sub blocks, a pixel array of the prototype display is divided into 32 blocks (four blocks arranged along the source line and eight blocks arranged along the gate line), each including 480 × RGB × 720 pixels. A control signal line of the pixel is connected to an output signal line of the corresponding driver sub block in the lower layer through a via hole (Fig. 12(B)). This structure eliminates the need for routing control signals from an end of the pixel array, effectively reducing the load on the signal line of the pixel. Table 1 shows the specifications of the OLED/OS/Si display.

Fig. 13 shows a die photograph of the Si driver, measuring 32 × 24 mm^2, corresponding to the shot size of the Si process. It includes four Si driver blocks, each sized at 16 × 12 mm^2. The 1.5-inch display is driven with the Si driver with a size of 32 × 24 mm^2.

VI. MEASUREMENT RESULTS

Fig. 14 shows the performance results of the prototype display. Under a normal mode, the entire display (all 32 driver sub blocks) was driven at a high resolution of 90 Hz. In the FR mode, assuming a user's gazed area, resolution and frame rate progressively decreased in three levels toward

TABLE 1. **Specifications.**

Two-dimensionally arranged display drivers	
Si CMOS process	55 nm HV Logic: 1.2 V , analog: 6.0 V
Input clock	381 MHz
Data transfer	30 Gbps@381 MHz
Number of drivers	32 source and scan drivers
SRAM	Integrated: 45 MB
Number of gates	Logic: 5 million
OLED/OS/Si display	
Structure	OLED / OS / Si
CAAC-OS process	360 nm
Screen diagonal	1.5 inch
Display size	30.41 mm × 22.81 mm
Resolution	3840 × RGB × 2880
Pixel density	3207 ppi
Pixel size	7.92 μm × 7.92 μm
Refresh rate	90 Hz@30 Gbps
Coloring method	Side-by-side with photolithography
Emission type	Top emission

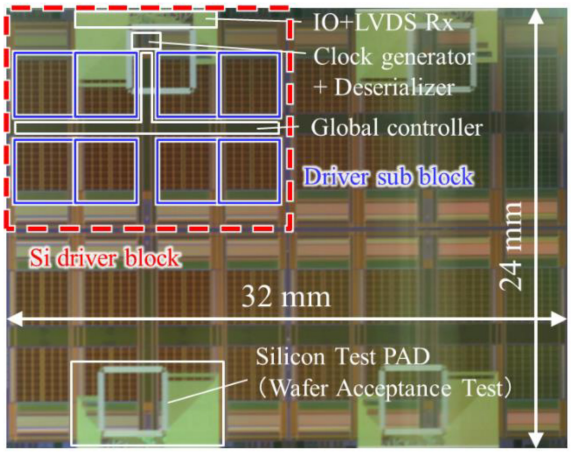

FIGURE 13. **Die photograph of 55-nm HV CMOS Si driver chip.**

TABLE 2. **Power consumption.**

	Driver power				Refresh rate	Data transfer	OLED power
	LVDS	Logic	Analog	Total			
Normal	84.83	360.6	649.53	1094.96	90	30	277.2
FR	20.81	212.01	291.73	524.55	90,45,30	3.75	268.8
unit	mW	mW	mW	mW	Hz	Gbps	mW

the edge of the display. Note that the display conditions in the FR mode shown in Fig. 14 are just examples, and any of the three-level resolutions and a given frame rate can be set for each of the 32 areas by register parameters. As shown in Fig. 15, the transition from the high resolution at 90 Hz to the low resolution at 30 Hz is visually evident.

Table 2 shows the power consumption during the display operation shown in Fig. 14. The total power consumption of the proposed driver is 1,094.96 mW at 30 Gbps in the normal mode and 524.55 mW at 3.75 Gbps in the FR mode. In the FR mode, where data transfer is notably reduced by

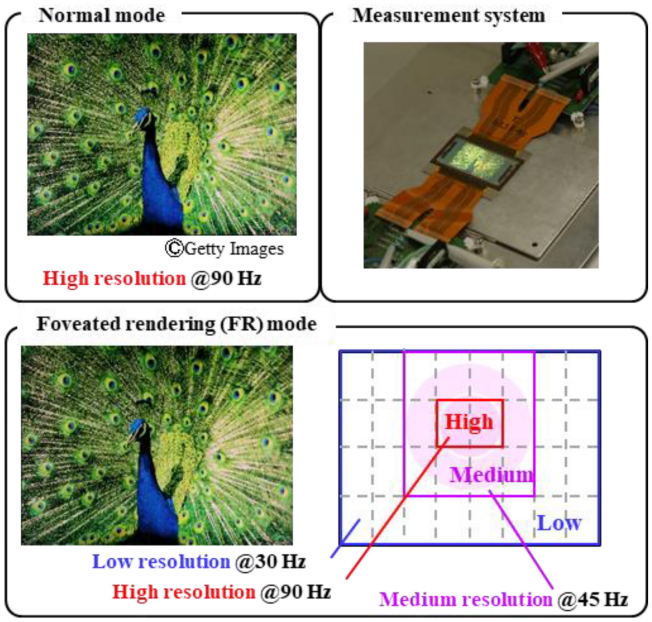

FIGURE 14. Photographs of display in normal and FR modes.

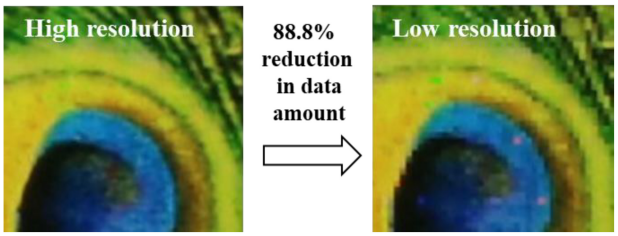

FIGURE 15. Enlarged views of high-resolution and low-resolution images.

87.5% on average across 90 frames compared to the normal mode, power savings are prominent. At this time, the power consumption of the LVDS Rx is reduced by 75.4%, owing to standby operation during non-data-transfer periods. Logic power usage is reduced by 41.2% by not switching data paths and arithmetic circuits during these idling periods, while analog power drops by 55.0% through the cessation of the amplifier constant currents in low-frame-rate areas. These results reveal a 52% reduction in total power consumption, demonstrating the successful functionality of LVDS Rx and the amplifier during standby operation in the FR mode. This evaluation was conducted in a power-saving mode, featuring half the number of amplifiers in a standby mode and doubled source lines selected by the demux in one amplifier.

As shown in Fig. 16, the LVDS Rx (40 data lanes, 750 Mbps/lane at 90 Hz, and 1 Gbps/lane at the maximum) and the amplifiers can return to an active state from a standby state in ∼100 ns. This rapid transition time is sufficiently shorter than an on-frame display period of 11.111 ms at a refresh rate of 90 Hz, confirming that switching between active and standby states does not adversely affect circuit operations. As shown in Fig. 17,

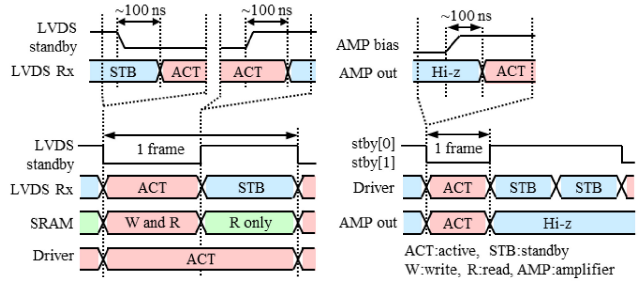

FIGURE 16. Control of standby operation of LVDS Rx and amplifiers.

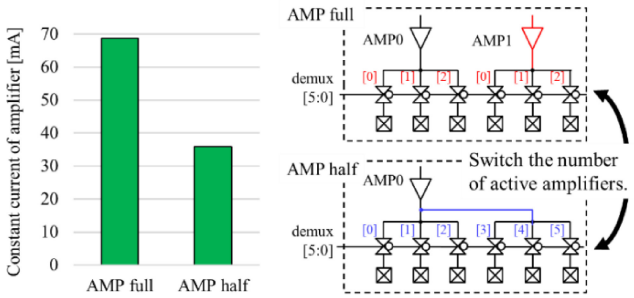

FIGURE 17. Constant current of amplifiers in eight driver sub blocks.

the total power consumption of amplifiers in the eight driver sub blocks is proportional to the number of active amplifiers. This demonstrates the successful implementation of a function enabling circuit performance adjustment based on the priority between operation speed and power consumption.

VII. CONCLUSION

We fabricated an OLED display using an OS/Si structure employing two-dimensionally arranged drivers. The proposed driver has two features: controllability of the resolution and frame rate for each driver and the changeability of the driver circuit performance. Our structure, developing the idea of FR, can reduce data transfer by enabling high-performance and low-performance settings for gazed and peripheral areas, respectively. From actual measurement results, we confirmed the achievement of the FR mode, where resolution and frame rate are controlled for each driver sub block. In the measurement, the power consumption of the proposed driver is 1,094.96 mW in the normal mode and 524.55 mW in the FR mode, revealing a 52% reduction in power consumption during the FR mode compared with the normal mode. In this manner, the two features of the OS/Si monolithic structure are validated by the measurement evaluation. Meanwhile, the image quality might be degraded due to borders generated by area division when there is a variation in the amplifier output potential.

As a comparative achievement, there is a report of a microdisplay formed using only Si CMOS which extends its function by an on-chip frame buffer [21]. The proposed display using the OS/Si structure includes a 45 MB on-chip frame buffer, but can avoid area overhead because the

Si circuit (frame buffer) can be formed under the CAAC-OS pixel circuits. Moreover, the bezel can be kept narrow even when a Si circuit is additionally provided for higher performance and higher definition, offering an advantage of a larger display area in the chip. Furthermore, the OS/Si structure possibly enables comparable performance even with a legacy process node prior to the 28 nm Si CMOS. However, unlike the microdisplay using only Si CMOS, the mass production process of our OS/Si display has not been established. Thus, the launch of the mass production process remains as an important issue in technical and economic aspects.

The proposed structure can reduce the load on the entire system, thereby minimizing data load in applications with high data demand. For example, in a gaming application necessitating high resolution and frame rate, our structure can facilitate 8 K at 180 Hz in a high-resolution area with two blocks, 4 K at 120 Hz in a medium-resolution area with ten blocks, and 1 K at 60 Hz in a low-resolution area with 20 blocks. This approach allows users to experience 8 K at 180 Hz comfortably. At this time, data transfer operates at ∼25.16 Gbps, indicating that a similar effect can be obtained with approximately one-tenth of the data load required for 240 Gbps for 8K at 180 Hz. As previously described, our developed VR system has the potential to enable users to have a viewing experience with a high resolution and frame rate, which has been difficult to achieve with conventional structures.

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