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A Performance Optimized Operational Amplifier Using Transconductance Enhancement Topology Based on a-IGZO TFTs

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ABSTRACT This paper reports a performance optimized operational amplifier (OPAMP) using transconductance enhancement topology based on the amorphous indium- gallium-zinc-oxide (a-IGZO) thin-film transistors (TFTs). The performance of TFTs is enhanced by N_2O plasma treatment that presents electrical characteristics suitable for accomplishing an OPAMP. The circuit consists of 19 TFTs with measured phase margin (PM) and unity-gain frequency (UGF) of 35.8° and 200 kHz, respectively. The DC power consumption (PDC) is 0.68 mW. Notably, it exhibits a high voltage gain (Av) of 32.67 dB and bandwidth (BW) of 15 kHz with 15 V DC supply voltage. Scarcely any work was reported with such a high gain while having a sufficient BW. The OPAMP demonstrates excellent performance among all a-IGZO literature and provides substantial support for the future development of TFT-based integrated circuits (ICs).

INDEX TERMS Amorphous InGaZnO (a-IGZO), thin film transistors (TFTs), N_2O plasma treatment, operational amplifier (OPAMP), positive feedback, transconductance enhancement topology.

I. INTRODUCTION

Thin-film transistor (TFT) technology occupies an important place in large-area and flexible electronics. The amorphous indium-gallium-zinc-oxide (a-IGZO) TFTs spark a boom in the field of metal oxide TFTs by virtue of high field effect mobility, room temperature process, excellent stability, and low production cost [1], [2]. Hence, researchers devote to applying a-IGZO TFTs to integrated circuits (ICs), such as radio frequency identification (RFID) [3], analog-to-digital converter (ADC) [4], and operational amplifiers (OPAMP) [5], [6], [7], [8]. OPAMP plays a dominant role in analog and mixed-signal systems which is the basics of the circuit in particular.

Due to the technological limitations of a-IGZO TFT technology, only n-type device is available for integration which leads to various design challenges such as poor device mobility, insufficient intrinsic gain, and insufficient load impedance [9], [10], [11], [12]. The threshold voltage (V_{TH}) drift also has a great impact on the design of OPAMP which affects the setting of the quiescent operation point. OPAMP with insufficient gain and bandwidth leads to the inability to meet the specific requirements in analog and mixed-signal systems which directly affects the signal acquisition, amplification, and transmission quality. Therefore, for a-IGZO TFT technology, systematical studying with high gain and wide BW OPAMP is necessary for future applications of low cost and low power, which shows its enormous potential.

To overcome the challenges, several design methods and circuit designs have been presented to improve the performance of OPAMP [13], [14]. The work reported in [15] adopted the method of cascade inverters to obtain 76 dB gain that resulted in terrible frequency response. It is feasible to improve the equivalent load of OPAMP by using the two-stage common-source amplifier as the positive feedback [16]. Pseudo-CMOS configuration was realized with only n-type a-IGZO TFTs in [17], meanwhile, the drawback is the need for more TFTs and additional high voltage supply. In addition, optimizing the electrical characteristics of the a-IGZO TFTs is another efficient solution to improve the performance of the OPAMP. One way is to introduce a Schottky contact barrier enlarging the intrinsic impedance of the a-IGZO TFTs [18], [19].

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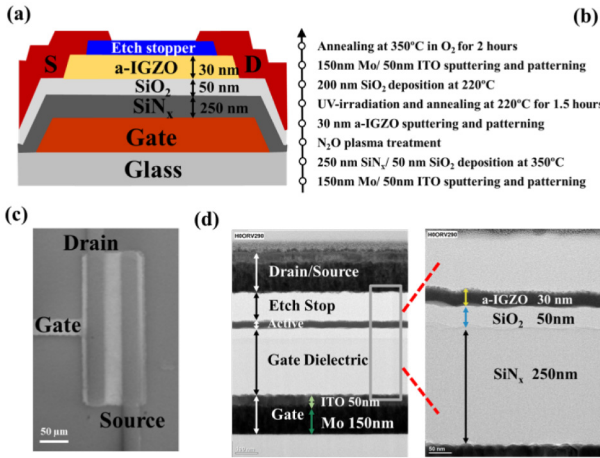

FIGURE 1. **(a) Schematic cross-section view, (b) major processing steps, (c) top-view SEM image, and (d) cross-sectional FIB-TEM image of the fabricated device.**

The other way is to increase the mobility of the channel materials which is equivalent to enlarging transconductance such as via plasma treatment [20]. However, improvement methods compatible with the existing manufacturing process is another challenge.

In this paper, we improved the performance of a-IGZO TFT by N_2O plasma treatment and verified the positive bias voltage stability. To explore the promising solution to TFT-based circuits, we proposed a performance optimized OPAMP integrated by the fabricated TFT. To increase gain, the transconductance enhancement topology is adapted to the circuit. Furthermore, the measurement nearly accords with the simulated characteristics that present high performance with high gain and sufficient bandwidth. We describe the fabrication process of our device in Section II. The electrical characteristics of the device and the performance of the OPAMP circuit are discussed in Section III. Conclusion is drawn in Section IV.

II. EXPERIMENTS

Fig. 1(a) and Fig. 1(d) show the schematic cross-section view image and cross-section FIB-TEM image of the fabricated a-IGZO TFTs. The fabrication process shown in Fig. 1(b) is conducted as follows. A 150 nm thick layer of molybdenum (Mo) and a 50 nm thick layer of Indium tin oxide (ITO) were sputtered by a sputtering machine (ULVAC SME-200E, Japan) and patterned as gate electrodes (G). ITO is used to protect Mo from being destroyed by the subsequent dry-etching process, meanwhile, the adhesion ability of ITO to connect different layers is better than Mo [21]. A 50 nm thick SiO_2 and 250 nm thick SiN_x were deposited by PECVD (ULVAC SME-200E, Japan) at 350 °C as the gate-insulator (GI). After that, used N_2O plasma treatment for 30 seconds to reduce the interface state between the GI and the active layer (AL). Then, a 30 nm thick layer of a-IGZO was formed as the AL by sputtering and lift-off process. After that, annealed it at 220 °C for 90 minutes before 3 minutes of UV irradiation. To protect the AL from water and oxygen, a 200 nm thick SiO_2 was deposited on the top of the a-IGZO by PECVD and patterned as an etch-stop layer (ES) by dry-etching equipment (DES-206E, Japan). Then the source and drain electrodes were sputtered with 150 nm thick Mo nd 50 nm thick ITO. Finally, the devices were annealed at 350 °C in O_2 for 2 hours to improve the performance. Then the device shown in Fig. 1 (c) was completed. The electrical properties of the TFTs were tested by the semiconductor parameter analyzer (Keithley 4200A-SCS) and probe stage in a dark room.

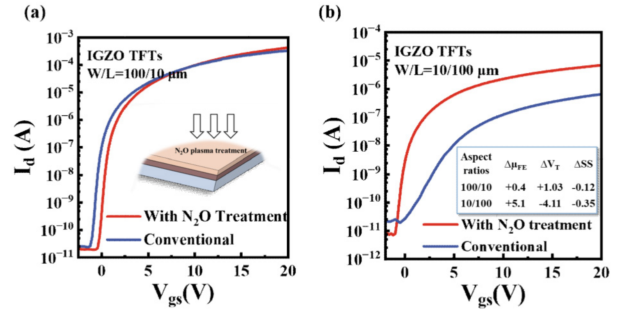

FIGURE 2. **Transfer characteristics of conventional IGZO TFTs and IGZO TFTs with N_2O plasma treated SiN_x insulator, with W/L = 100 μm/10 μm in (a) and W/L = 10 μm/100 μm in (b).**

III. RESULTS AND DISCUSSION

A. DEVICE ELECTRICAL CHARACTERISTICS AND SPICE SIMULATION FITTING

The transfer characteristics of conventional a-IGZO TFTs and a-IGZO TFTs with N_2O plasma treated GI are shown in Fig. 2. The N_2O plasma treatment was used to effectively reduce the defect states between the GI layer and the AL layer [22], [23]. Compared to the conventional device, the device with N_2O plasma treatment can be clearly observed that the subthreshold swing (SS), the field effect mobility (μ_{FE}), and V_{TH} have improved. According to the a-IGZO TFTs with W/L=10/100 μm, the V_{TH} of drifts reached 4.11 V, and the SS reduction is 0.35 V/decade. For TFTs with varying W/L ratios, performance differences are inherent. As the channel length decreases, carriers are more prone to being captured by interface states during the migration process and the V_{TH} becomes larger [24]. The variation in μ_{FE} is attributed to overestimation caused by source-drain contact resistance and edge-field effects [25]. The impact of changes in interface states varies with different channel lengths which following the patterns mentioned earlier. The fabricated TFTs present electrical characteristics suitable for accomplishing an OPAMP.

Fig. 3(a) shows the measured transfer characteristics of the fabricated a-IGZO TFTs with different aspect ratios, which provides the basis for the subsequent circuit design. Extracted from the transfer characteristic, the trend of SS, μ_{FE} and V_{TH} are shown in Fig. 3(b), which demonstrate the difference in the close range. To be clear, the parameters presented in Fig. 3(b) represent average results of several devices with

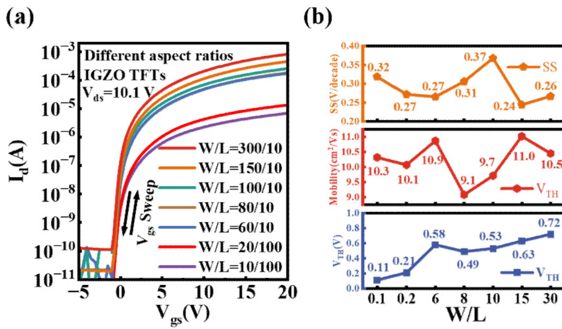

FIGURE 3. (a) Transfer characteristics of a-IGZO TFTs with different aspect ratios, and (b) SS, μ_{FE}, and V_{TH} of the devices. The parameters are the average of several devices.

TABLE 1. Shows the key electrical parameters of a-IGZO TFTs.

Aspect ratios (W/L)	μ_{FE} (cm^2/Vs)	V_{TH} (V)	SS (V/decade)	I_{ON}/I_{OFF}
300/10	10.5	0.72	0.26	6.85×10^6
150/10	11.0	0.63	0.24	2.13×10^7
100/10	9.7	0.53	0.37	1.12×10^7
80/10	9.1	0.49	0.31	1.47×10^7
60/10	10.9	0.58	0.27	1.43×10^7
20/100	10.1	0.21	0.27	4.45×10^6
10/100	10.3	0.11	0.32	7.26×10^6

varying W/L ratios. In addition, the ratio of I_{ON}/I_{OFF} stays above 10^6. In order to verify the stability of the device, a positive bias stability (PBS) test was performed on the a-IGZO TFTs, as shown in Fig. 4. The gate bias voltage of 20 V was applied for 1200 seconds at room temperature in atmosphere. The fabricated TFTs based on different aspect ratios present different degrees of drift under the PBS test. The V_{TH} drifts under bias voltage stress is attributed to electron trapping between interface of the AL layer and GI layer. The V_{TH} drifts of the TFTs were 0.21 V and 0.37 V, which demonstrates excellent stability under bias voltage stress.

For circuit simulation, the a-IGZO TFTs' characteristic is fit by McMaster University's compact model [26], [27]. Combined with the I-V characteristic of the a-IGZO TFTs, the unknown parameters of the device are extracted. Then the parameters are substituted into the model for further optimization. The measured characteristics with the SPICE simulation fitting data for the a-IGZO TFTs are shown in Fig. 5. The discrete points plot represents the measurement, while the solid line is the fitted data, the former and the latter coincide distinctly. The average percentage error between measured curve and fitted data is less than 5%. According to the standard, the compact model is accurate enough to be used for circuit simulation.

B. CIRCUIT DESIGN AND SIMULATION

The proposed OPAMP is shown in Fig. 6(a). Considering the fabrication process, adopt the 10 μm design rule. TABLE 2 shows the geometry of the TFTs used for the OPAMP. The

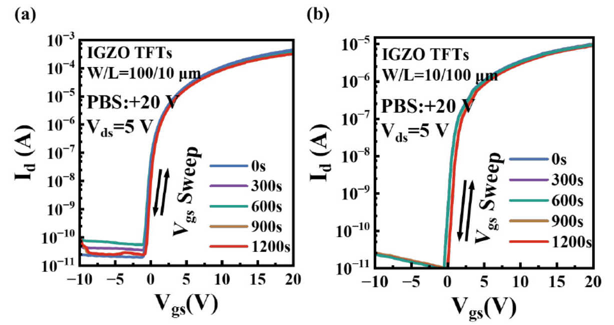

FIGURE 4. Transfer characteristics of a-IGZO TFTs under PBS test with W/L = 100 μm/10 μm in (a) and W/L = 10 μm/100 μm in (b), respectively. The Vgs was applied to +20 V for a duration of 1200 s.

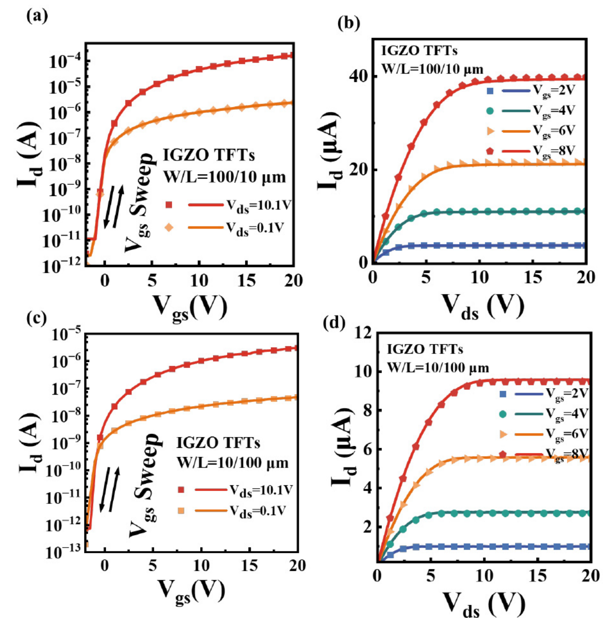

FIGURE 5. Measured and SPICE simulation fitting transfer characteristics in (a, c) and output characteristics in (b, d) of a-IGZO TFT with W/L = 100 μm/10 μm and W/L = 10 μm/100 μm, respectively. The solid line represents the fitted data while the discrete points are experimental data.

proposed OPAMP can be broadly divided into three stages. The first stage consists of input terminals and current mirrors. As a current mirror, T1 and T2 provide a stable bias voltage to T6 for the tail current. Then T4 and T8 are transistors for differential input which reduce the effect of noise. T10-T13 is a differential-to-single-ended converter with a current mirror that delivers the signal through the second stage. Due to the low mobility and low intrinsic gain of the TFTs, the transconductance enhancement topology is an effective method to improve the open-loop gain of the TFT OPAMP circuit. To increase the gain, T5 and T7 are connected to the source of the input transistors by introducing positive feedback to the source of the input terminals. Neglecting the channel length modulation, the equivalent transconductance of the input terminals is given by

$$G_m = \frac{g_{m4,8}}{1 - \frac{g_{m4,8}}{g_{m5,7}}} \tag{1}$$

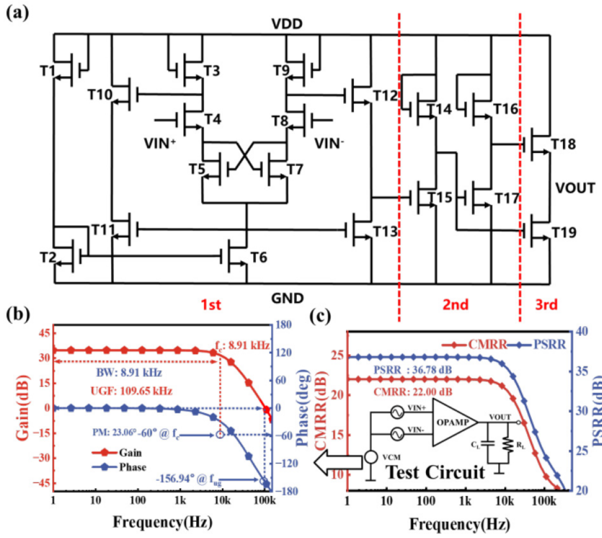

FIGURE 6. (a) Circuit schematic of the proposed OPAMP. (b) Simulated frequency response and (c) CMRR and PSRR of the proposed OPAMP.

TABLE 2. Geometry of the TFTs used for the OP-AMP.

TFT	W/L[μm]	TFT	W/L[μm]	TFT	W/L[μm]
T1	300/10	T8	300/10	T15	200/30
T2	300/10	T9	20/200	T16	50/50
T3	20/200	T10	50/20	T17	200/30
T4	300/10	T11	20/100	T18	300/30
T5	240/10	T12	50/20	T19	200/30
T6	300/10	T13	20/100		
T7	240/10	T14	50/50		

The equivalent transconductance has been increased, meanwhile, the gain of the amplifier circuit is improved. The gain of the first stage is given by

$$A_{1st} = \frac{g_{m4}g_{m10}\left[g_{m10}^{-1}\|r_{o10}\|r_{o11}\right]}{g_{m3}\left(g_{m4} - g_{m5} + r_{o4}^{-1} + r_{o5}^{-1}\right)} \quad (2)$$

The second stage consists of two common-source amplifiers which are adopted to obtain high gain and high input impedance. The calculated gain of the second stage can be given by

$$A_{2nd} = \frac{g_{m15}}{g_{m14}}\frac{g_{m17}}{g_{m16}} \quad (3)$$

Finally, the third stage acts as an output buffer to obtain low output impedance. The calculated gains of the third stage are as follows

$$A_{3rd} = \frac{g_{m18}r_{o19}}{1 + g_{m19}r_{o19}} \quad (4)$$

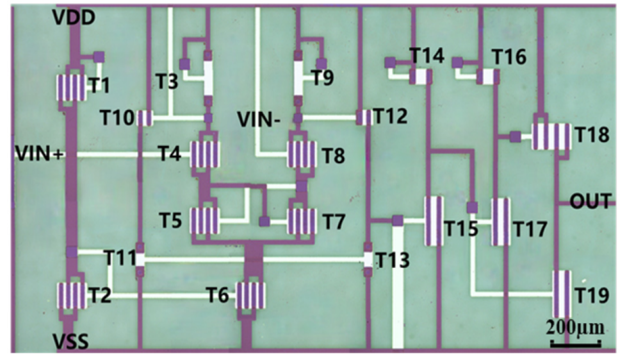

FIGURE 7. Microscope diagram of the proposed OPAMP.

Assuming no gain reduction caused by the current mirror in the first stage and A_{3rd} approaches to 1, the overall voltage gain of the proposed OPAMP can be given by:

$$A_v \approx \frac{g_{m4}g_{m15}g_{m17}}{g_{m3}g_{m14}g_{m16}(g_{m4} - g_{m5} + r_{o4} + r_{o5})} \quad (5)$$

where G_m shows the equivalent transconductance of input terminals, g_m represents the transconductance of transistors while r_o shows the output resistance, respectively.

The proposed OPAMP is verified and optimized by SPICE simulation. Fig. 6(b) shows the simulated frequency response of the proposed OPAMP. With a 15 V supply voltage, the gain can reach 34.73 dB. The simulated −3 dB bandwidth is 8.91 kHz and the phase margin is 23.06°. Verified by simulation, the DC power consumption (P_{DC}) is 0.68 mW. The common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) are illustrated by simulation calculation in Fig. 6(c). The PSRR is 36.78 dB, and the CMRR is 22.00 dB which approaches the value of CMRR in [28] and indicates the proposed OPAMP has strong anti-interference ability. The key factor to improve CMRR and PSRR is to make the circuit more symmetric. Then by reducing unnecessary routing around the matching device and placing the matched devices consistently and close in the physical layout, the transistors of the OPAMP match better. In addition, adopt multiple fingers structure instead of the large size transistor is an effective way to reduce the mismatch of the OPAMP.

C. EXPERIMENTAL RESULTS OF OPAMP CIRCUIT

The proposed OPAMP is integrally fabricated on glass substrates. The area of the circuit shown in Fig. 7 is 2.76 mm × 1.6 mm. To reduce the V_{TH} mismatch and power consumption, symmetry design and multiple fingers design were employed for layout design. The measurement equipment is a semiconductor parameter analyzer (Keithley 4200A-SCS), an oscilloscope (Tektronix MSO22), and a signal generator (RIGOL DG821). To bias the OPAMP, the VDD and VSS are set as 15 V and ground. And 7 V is applied to VIN+ and VIN- for common mode voltage (VCM). Besides, to reach the purpose of differential input, an extra small sinusoidal signal is provided to VIN+.

TABLE 3. Comparison of the parameters between different OPAMP.

Parameter	This work	[8]	[28]	[29]	[30]	[31]	[32]
Year	2023	2017	2021	2019	2021	2015	2023
TFT	a-IGZO	a-IGZO	IZO	a-IGZO	IZO	a-IGZO	a-IGZO
VDD [V]	15	20	10	±10	±15	±15	5
Av [dB]	32.67	30	27	23.52	29.54	26.8	36
BW [Hz]	15k	150	8.4k	500k	9.33k	8.15k	-
UGF [Hz]	200k	5.5k	119.4k	2370k	180.2k	47.3k	4
PM [deg]	35.8	-	36	102	-21.5	-	-
Topology	Positive Feedback	NMOS Diode	Positive Feedback	NMOS Diode	NMOS Diode	NMOS Diode	Zero V_{gs}
P_{DC} [mW]	0.68	0.4	0.96	51	5.07	-	-

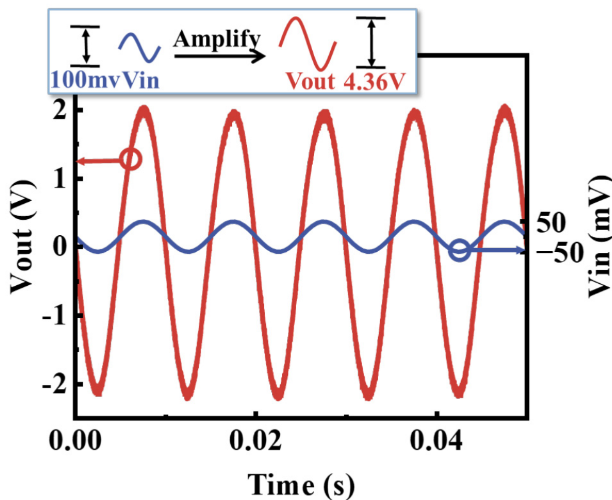

FIGURE 8. Measured input and output signal waveform for a frequency of 100 Hz.

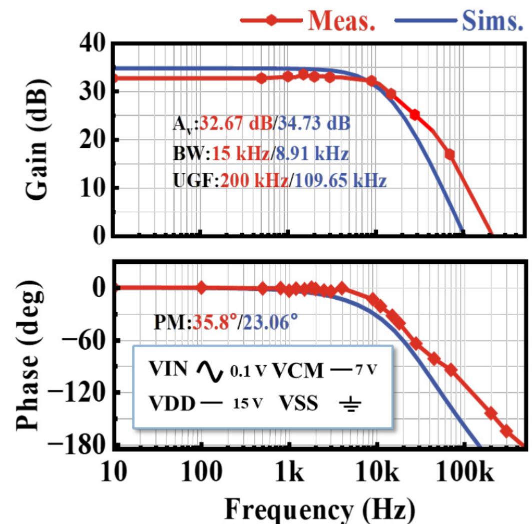

FIGURE 9. Measured frequency response of the proposed OPAMP with 15V DC supply voltage.

The measured waveforms of the proposed OPAMP with a sinusoidal differential input of 100 Hz and 10 mV_{pp} (peak to peak) are plotted in Fig. 8. The waveform of VOUT is 4.36 V_{pp} indicating that the AC gain of the proposed OPAMP reached 32.67 dB. It is worth mentioning that, due to one of the original intentions of the design is to reduce noise interference, compared with [15], [28], [29], [30], the burred feature on the output waveform is relatively slight. Fig. 9 shows the measured results of the frequency response of the proposed OPAMP and provides a comparison to simulation results. The AC gain is 32.67 dB with 15 kHz of BW and the UGF is around 200 kHz. The value of measured PM is 35.8° showing a 12° of difference with simulation. The layout generates parasitic capacitance, resulting in the measurement of unity-gain frequency and phase margin being higher.

TABLE 3 provides a comparison of the proposed OPAMP with other a-IGZO-based OPAMP reported recently. Compared to the other designs by only n-type TFTs, the voltage gain of the proposed OPAMP is higher than the other designs reported in [8], [28], [30], [31]. It is worth mentioning that the OPAMP in [29] obtains wider BW and phase margin by virtue of dual gate (DG) TFTs that the DG TFT has stable transfer and high output current which is almost 2.5 times that of the conventional TFT. But the lack of compensating for the insufficient intrinsic gain leads to the magnification is inferior which is only 40 percent of our work. To further improve the lack of phase margin and BW, miller compensation and threshold voltage compensation techniques are effective methods in subsequent studies. Nonetheless, compared to the design in [8], [32], the BW of the proposed OPAMP has an absolute advantage. From the work in [32], it is obvious that the load of Zero-V_{gs} can effectively improve the gain, the accompanying problem is lack of bandwidth. In terms of power consumption, the proposed OPAMP is slightly higher than the work in [8] with

novel topology which bring low current consumption. In the light of gain and bandwidth, the proposed OPAMP affirms its high superiority with other metal oxide TFT OPAMP designs, shows the potential for future low cost and low power applications.

IV. CONCLUSION

This paper presents a design of a performance optimized OPAMP based on the a-IGZO TFTs with excellent electrical characteristics, conquers almost all the other designs among a-IGZO-based in literature. The OPAMP exhibits a high gain of 32.67 dB with −3 dB bandwidth of 15 kHz at a DC supply voltage of 15 V. The PM and UGF are derived as 35.8° and 200 kHz, respectively. The P_{DC} is 0.68 mW. Verified by simulation, PSRR and CMRR are 22 dB and 36.78 dB which shows strong anti-interference ability to against noise. As a result, the OPAMP with high gain and sufficient BW not only demonstrates the reliability and superiority of the design but also provides a promising solution to TFT-based circuits.

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