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Design of Fast Response Back-Illuminated 3-D Composite Electrode Silicon Detector Utilizing the RIE-Lag Phenomenon

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ABSTRACT In this paper, a back-incidence 3D Composite Electrode Silicon Detector (3DCESD) is proposed and simulated. The electrode structure comprises 70% trench-like and 30% column-like features, achieved through a single etching step utilizing the RIE-lag phenomenon of the Bosch process. The performance of the 3DCESD device is influenced by the structural parameter *S*. Comparative simulations were conducted using TCAD. The overall electric field and weighting potential of 3DCESD are significantly optimized. MIP and continuous pulse laser were performed separately under bias voltages of –50V and –5V. The 3DCESD exhibits notable advantages, including rapid response speed, high charge collection efficiency, minimal inhomogeneity, and low power consumption.

INDEX TERMS 3DCESD, RIE-lag phenomenon, composite electrode, TCAD simulation, MIP, pulsed laser.

I. INTRODUCTION

In 1997, Parker et al. proposed the first three-dimensional (3D) detector [1]. In contrast to two-dimensional (2D) planar detectors, the electrodes of a 3D detector are vertically fabricated in the silicon substrate using deep reactive ion etching (DRIE) technology, allowing for a significant reduction in electrode spacing. The 3D detector has garnered considerable attention due to its advantages in radiation hardness. Research institutions such as CNM, FBK, SINTEF MiNaLab, and BNL have proposed various designs of 3D silicon detectors. These designs encompass single-sided column electrode detector [2], [3], [4], double-sided column electrode detector [5], [6], [7], [8], annular trench electrode detector [9], [10], and plate trench electrode detector [11], [12]. Recently, detectors based on the principles of 3D detection, such as perovskite detectors [13] and silicon carbide detectors [14], have also been proposed.

In this paper, a 3D Composite Electrode Silicon Detector (3DCESD) with back incidence is proposed, as show in Fig. 1(a) to (c). The composite electrode was fabricated by RIE-lag phenomenon of Bosch process. The bottom of the 3DCESD faces the signal source. It can be used as a direct detector, or combined with a scintillator as an indirect detector, or combined with a lobster eye as a pulsar navigation detector. When high-energy particles penetrate the silicon detector, uniform electron-hole (*e-h*) pairs are generated along the incident trajectory, as illustrated on the left of Fig. 1(d). However, when X-rays or scintillators convert high-energy particles into photons, *e-h* pairs can be produced on the surface in large numbers. Therefore, optimizing the electric field and weighting potential on the backside of the 3D detector is crucial.

Initially, we conducted a feasibility evaluation experiment to fabricate composite electrodes. Subsequently, we analyzed the electric field and weighting potential distribution of 3D detectors with various structures using TCAD. In this study, we simulated Minimum Ionizing Particle (MIP) incidents using a heavy ion model and pulse light incidents using a

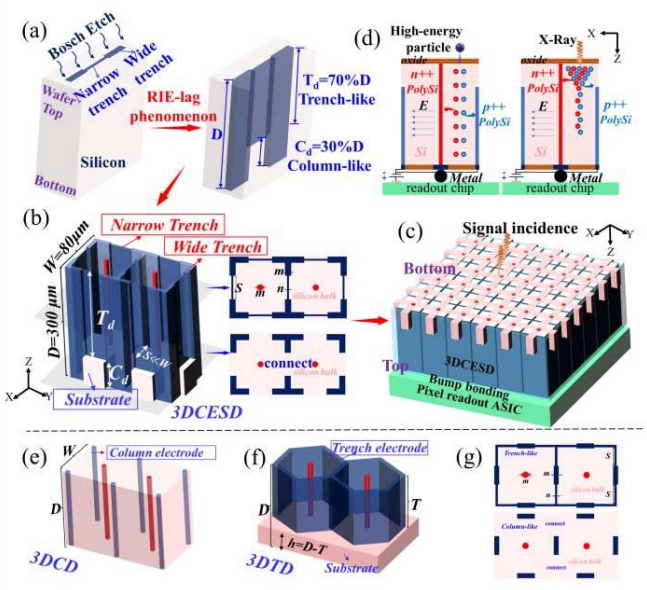

FIGURE 1. **(a) RIE-lag phenomenon of Bosch etch. (b) 3D composite electrode silicon detector, 3DCESD. (c) Diagram of the array. (d) Schematic diagram of carrier collection for back incident 3DCESD. (e) 3D column electrode silicon detector,3DCD. (f) 3D trench electrode silicon detector,3DTD. (g) Schematic diagram of 3DCESD-3, its narrow trench are located at the four corners of the pixel.**

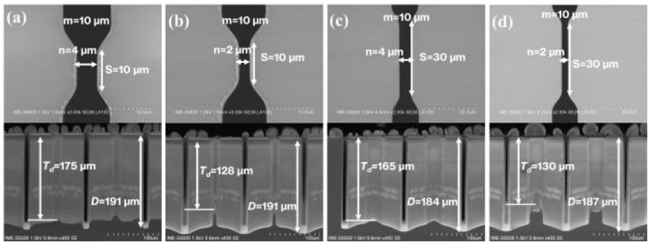

FIGURE 2. **SEM image of bosch etching experiment: (a) n = 4 μm, S = 10 μm; (b) n = 2 μm, S = 10 μm; (c) n = 4 μm, S = 30 μm; (d) n = 2 μm, S = 30 μm.**

TABLE 1. **Structural parameters.**

Structure (μm)	S	m	n	T	T_d	C_d
3DCD	-	10	-	-	-	-
3DTD-210	-	10	-	210	-	-
3DTD-270	-	10	-	270	-	-
3DCESD-1	10	10	2	-	210	90
3DCESD-2	30	10	2	-	210	90
3DCESD-3	25	10	2	-	210	90

The parameter S represents the length of the narrow trench, m denotes the width of the wide trench, and n signifies the width of the narrow trench. T and T_d represents the depth of the trench and trench-like electrode, respectively. C_d represents the depth of the column-like electrode.

ray tracing model. In both simulations, the signals penetrated the detector, resulting in the generation of uniform carriers along the incident trajectory.

II. EXPERIMENTS AND RESULTS

The Bosch process [15], [16] is commonly employed in the fabrication of 3D detectors. When the number of cycles is constant, the etching depth is influenced by the area of the etching mask pattern. A larger mask pattern area results in a greater etching depth, which is a characteristic known as the reactive ion etching lag (RIE-lag) phenomenon [17], [18], [19]. Fig. 2 illustrates the experiment of the composite electrode etching process. Due to the contamination limit of the chip front-end process, aluminum cannot serve as a hard mask for deep silicon etching. Considering the overall process flow, the hard mask is configured as a SiO_2-Si_3N_4-SiO_2 (ONO) structure. The wide trench width (m) is 10 μm, and the etching depth D is approximately 190 μm, meeting the requirements of ATLAS for detector thickness [20], [21]. The difference in etching depth between wide and narrow trenches is primarily associated with the width n of the narrow trench. The ratio remains relatively stable as S increases from 10 μm to 30 μm. However, for the 3DCESD structure, it is essential to ensure that the width of the substrate beneath the narrow trench is sufficiently large to guarantee mutual connection between adjacent detection units. Therefore, the experimental result in Fig. 2(d) aligns closely with our requirements, with 70% of the detector consisting of trench-like electrodes and 30% comprising column-like electrodes.

In Fig. 2, it can also be observed that there is uneven etching depth at the bottom of the electrode, with the etching depth gradually decreasing from the bottom of the wide trench to the bottom of the narrow trench. Chamfering was performed on the layout to avoid excessively high electric fields at the right angles where wide and narrow trench intersect. Therefore, there is a transition region of 5 μm at the junction of narrow and wide trench in the actual device. Changes in width will result in variations in gas flow rate, with the lowest gas flow rate at the narrow trench and the highest at the junction of the wide trench, leading to uneven etching at the bottom of the composite electrode. As a back-illuminated detector, it is ultimately necessary to thin the wafer, and a slight increase in the thickness of thinning can address the unevenness issue.

The structure of 1×2 device array is simulated in this study to estimate the device performance. 3DCESD-1 and 3DCESD-2 are composite electrode detectors with a narrow trench located in the center, as depicted in Fig. 1(b), with lengths S of 10 μm (3DCESD-1) and 30 μm (3DCESD-2), respectively. 3DCESD-3, shown in Fig. 1(g), features the narrow trench positioned at the four corners. The width m of wide trench is set to 10 μm, and the width n of narrow trench is set to 2 μm. In TCAD simulation, the oxide layer is set on the top and bottom surfaces of the device, and the Si-SiO_2 interface is set with fixed positive charge of 4×10^{11} cm^{-2}. The polysilicon is completely filled, disregarding the influence of the unknown cavity shape after polysilicon LPCVD on device performance. The structural dimensions in the simulation are as shown in Table 1.

The parameter S represents the length of the narrow trench, m denotes the width of the wide trench, and n signifies the width of the narrow trench. T and T_d represents the depth of the trench and trench-like electrode, respectively. C_d represents the depth of the column-like electrode.

As described in the analysis of Fig. 2, parameters m and n are mainly structural parameters that affect the etching results of the composite electrode. Assuming the depth of the narrow trench remains unchanged, the impact of increasing n from 2 to 4 μm on the electrical performance is relatively minor compared to S. However, when n further increases, it becomes impossible to realize the composite electrode structure, thereby losing the significance of simulation. For 3D detectors, typical areas include 50 μm $\times$ 250 μm (2E), 25 μm $\times$ 100 μm (2E) and 50 μm $\times$ 50 μm (1E), etc. The design in this paper has a size of $W \times W = 80$ μm$\times$80 μm, with an electrode spacing of 30 μm, which conforms to the characteristic of small electrode spacing in 3D detectors. When W increases: 1) Increasing the electrode spacing leads to the detector losing its fast response and strong radiation resistance characteristics, deviating from the original design intention of the 3DCESD. 2) If W is slightly increased while parameters such as S remain unchanged, only an increase in voltage is needed, and the simulation results will not show significant changes. 3) If W is too large, the impact of the Si-SiO_2 interface on the device cannot be ignored. At this time, structures such as p-stop or floating ring need to be added to the surface to optimize the surface electric field. Similar work has been published in [22]. However, as W decreases further, the proportion of dead zones caused by the electrodes will significantly increase, following a trend similar to that shown in [9]. Therefore, since the electrical performance is mainly affected by S, the change of S was mainly simulated based on the experimental results.

According to the Shockley-Ramo theorem [23], [24], the induced current is correlated with the electric field and weighting potential (V_W) of the detector. Fig. 3 shows the electric field distribution of five different 3D detectors. As depicted in Fig. 3(a) and (b), we observe that the low electric field regions are situated between the column electrodes of the same doping in 3DCD (Fig. 1(e)) and in the bottom substrate of 3DTD-210 (The trench depth T=210 μm in Fig. 1(f)), respectively. The diffusion motion of carriers in this region results in a prolonged signal response time and increased signal loss. Fig. 3(c) (d) and (e) are the electric field distributions of 3DCESD. In profile *C1*, it is evident that the electrical performance of the detector remains relatively consistent from the top to the bottom. In the *C2* cross-section, the electric field distribution within the trench-like electrodes of the 3DCESD is similar to that of the trench electrodes in the 3DTD. In the *C3* cross-section, for 3DCESD-1 with a smaller value of S, its internal electric field distribution remains similar to that of the trench electrodes. When the value of S increases to 30 μm for 3DCESD-2, the saddle point in the column-like electrode

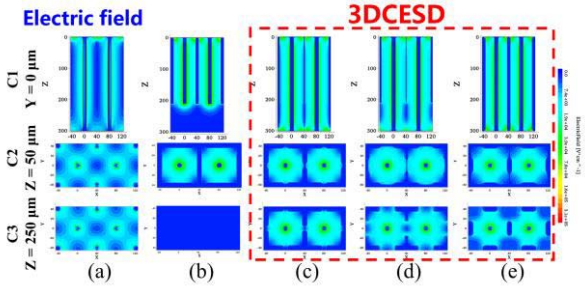

FIGURE 3. Electric field distribution with -50V reverse bias voltage applied: (a) 3DCD; (b) 3DTD; (c) 3DCESD-1; (d) 3DCESD-2; (e) 3DCESD-3.

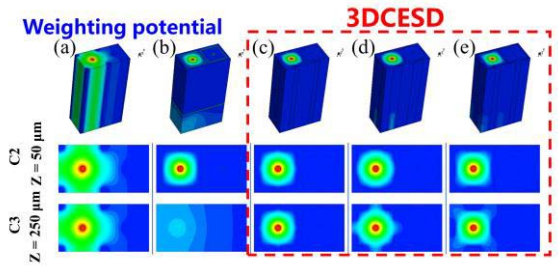

FIGURE 4. Weighting potential distribution: (a) 2DPD; (b) 3DCD; (c) 3DTD; (d) 3DCESD-1; (e) 3DCESD-2; (f) 3DCESD-3; (g) 2D cross section of weighting potential distribution at Z=50 μm and 250 μm.

became more obvious. It can be inferred that the electric field distribution in the column-like electrode will be more similar to 3DCD when S is further increased. The design of the 3DCESD-3 results in a large dead zone at all four corners.

Fig. 4 shows the distribution of weighting potential. The V_W is the potential distribution when 1 voltage is applied to the reading electrode and all other electrodes are under zero bias [25]. At Z=50 μm, for the V_W in the 3DTD and the 3DCESD, the lowest value is located at the inner boundary of the trench/trench-like electrode of Pixel-1. For 3DCD, V_W decreases at Pixel-1 but terminates within Pixel-2. Therefore, the weighting field (∇V_W) of 3DCD must be less than 1/30 μm with linear approximation. The trench and trench-like electrodes have stronger isolation than the column electrode. At Z=250 μm, the 3DTD becomes much less than 1, so the bottom weighting field can be approximately regarded as zero. For 3DCESD, an increase in S in the bottom column-like electrode results in the expansion of the V_W towards adjacent pixels but terminates quickly. The V_W in the column-like electrode will be closer to 3DCD if S is further increased.

The MIP is defined by the Bethe-Block [26] formula. When the MIP is vertically incident, uniform e-h pairs are generated on the incident trajectory, resulting in 76 e-h pairs per micron in silicon. Here we only focus on the electric field distribution and weighting potential distribution in the space charge region. We make the assumption that the electric field in the substrate at the bottom of the 3DTD is 0 V/cm. Then

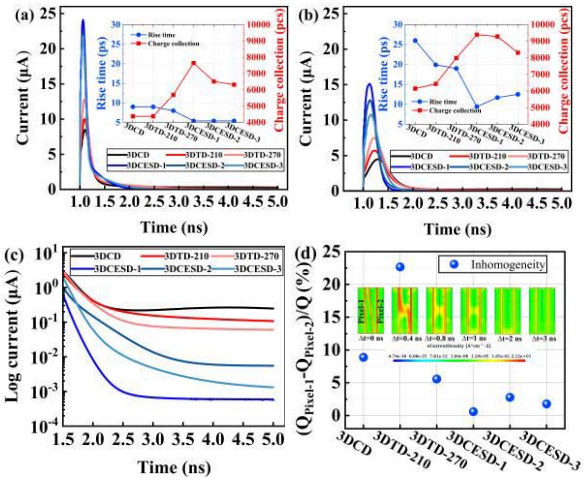

FIGURE 5. The *i-t* curves, rise time and charge collection (a) (15,0,0); (b) (25,0,0); (c) The log current after the 1.5 ns in (c); (d) 3DCESD-2 electron current density distribution from Δt=0 ns to 3 ns time range. The MIP incidence point and exit point are (25,0,0) and (55,0,300) respectively.

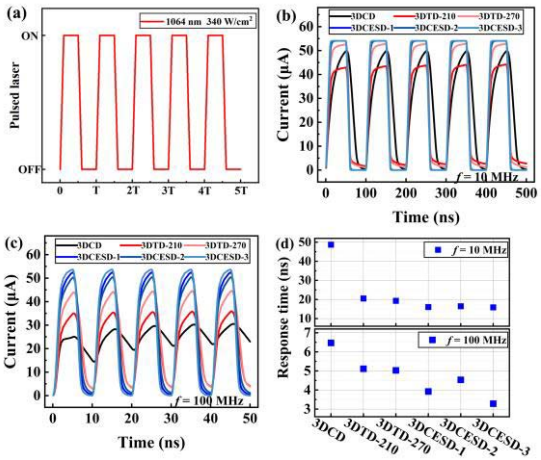

FIGURE 6. Pulsed laser. (a) Input pulse. (b) The output pulse at 10 MHz. (c) The output pulse at 100 MHz. (d) Response time at 10 MHz and 100 MHz. The sum of the rise time (10%-90%) and fall time (90%-10%).

the ratio of the induced current can be written as:

$$\frac{i(t)_{3DCESD}}{i(t)_{3DCD}} \approx 1 + \frac{7}{10}\left(\frac{\overrightarrow{E(x)}_{Tre-like}}{\overrightarrow{E(x)}_{3DCD}} \cdot \frac{\nabla V_{WTre-like}}{\nabla V_{W3DCD}} - 1\right) > 1 \tag{1}$$

$$\frac{i(t)_{3DCESD}}{i(t)_{3DTD}} \approx \frac{T_d + C_d}{T} = \frac{300}{T} = \begin{cases} 1.43 > 1, & T = 210 \\ 1.11 > 1, & T = 270 \end{cases} \tag{2}$$

The MIP vertical incidence simulation is done at (15,0,0) and (25,0,0).The applied voltage for all MIP simulations is –50 V, and the FinalTime is set to 5 ns. In a short period, carriers undergo lateral synchronous drift under the action of uniform electric field of 3DCESD, enhancing the response speed and avoiding long-term current tailing. As shown in Fig. 5 (a) and (b), the peak current of 3DCESD is 1.5–4.5 times that of other structures, and the full width at half maximum (FWHM) is significantly smaller. Without the influence of low electric field of saddle point and substrate, the rise time of 3DCESD is reduced by about 50%, and the charge collection is significantly improved.The electrical performance of 3DCESD is negatively correlated with its structural parameter *S*. For (25,0,0) incident, when *S* is increased by 3 times, the peak current decreases by 15.2%, the rise time increases by 19.7%, and the charge collection decreases by 1.2%. As shown in Fig. 5 (c), the current of 3DCESD-1 basically falls to the lowest value at 2.5 ns. But for 3DCESD-2, the enlargement of the saddle point within the column-like electrode has led to a slowing down of the descent time.

Simulations with MIP tilted incidence were performed to investigate the electrical inhomogeneity of the device from top to bottom. The inhomogeneity is affected not only by the 3D electrode structure but also by the presence of the film layer. To control variables, aluminum wiring identical to the trench electrode was also placed on the upper surface of the column electrode. This resulted in 8.9% inhomogeneity in 3DCD. To maintain control over variables, the surface metal wiring on the top of the 3DCD is set identical to the metal wiring on the square trench. Additionally, the difference in materials between the top and bottom of the 3DCD results in distinct electric fields at the top and bottom, as illustrated in Fig. 3(a). The difference in electric fields leads to increased inhomogeneity. The electron current density of 3DCESD-2 at different time points is depicted in Fig. 5(d). As time progresses, the electrons bifurcate into two groups, with the upper half and lower half drifting towards the central N+ electrode of Pixel-1 and Pixel-2, respectively. At Δt=2 ns, electrons in the bulk have mostly dissipated, but some electrons remain at the bottom. The relatively slower collection speed at the bottom results in a reduction in $Q_{pixel-2}$, leading to an increase in electrical inhomogeneity in 3DCESD-2 compared to 3DCESD-1 by 2.7%. But compared to 3DTD-270, 3DCESD decreased by 2.8%–5.0%. And compared to 3DTD-210, it decreased by 19.9%–22.1%.

A bias voltage of –5 V was employed in simulations to assess the 3D detector's performance at lower operating voltages, aiming for reduced power consumption. In this study, a penetrating infrared laser with a wavelength of 1064 nm and a light intensity of 340 W/cm^2 was utilized for simulation based on the ray tracing method. Fig. 6(a) illustrates the input of five pulse laser cycles, while Fig. 6(b) displays the output signal at 10 MHz. The waveform of 3DCESD closely matches the input laser pulse waveform. However, due to the significantly smaller carrier diffusion velocity in the non-depletion region compared to drift velocity, the waveforms of 3DCD and 3DTD are severely distorted. When the frequency is increased to 100 MHz, the simulation results in Fig. 6(c) reveal that the output signal of 3DCD is unable to drop to the low level before being triggered to rise again by the next pulse laser input, resulting in pulse pile-up. From Fig. 6(d), it can be observed that 3DCESD exhibits the fastest response speed, although it decreases with the increase of *S*.

III. CONCLUSION

This paper proposes a novel back-incident 3DCESD array. The fabrication of composite electrodes is achieved using the RIE-lag phenomenon. The optimization of the composite electrode improves the response speed, charge collection, and reduces electrical inhomogeneity by optimizing the backside electric field and weighting potential distribution. The simulation results also indicate that 3DCESD maintains a fast response time and low power consumption relative to the other 3D detector structures at high frequencies.

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