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Stability of GaN HEMT Device Under Static and Dynamic Gate Stress

LINFEI GAO[1,2,3,4,5], ZE ZHONG[1,2,3,4,5], QIYAN ZHANG[1,2,3,4,5], XIAOHUA LI[1,2,3,4,5], XINBO XIONG[1,2,3,4,5], SHAOJUN CHEN[1,2,3,4,5], LONGKOU CHEN[6], HUAIBAO YAN[7], ANLE ZHANG[7], JIAJUN HAN[8], WENRONG ZHUANG[8], FENG QIU[9], HSIEN-CHIN CHIU[10] (Senior Member, IEEE), SHUANGWU HUANG[1,2,3,4,5], AND XINKE LIU[1,3,4,5] (Senior Member, IEEE)

1 College of Materials Science and Engineering, Shenzhen University, Shenzhen 518060, China
2 College of Electronics and Information Engineering, Shenzhen University, Shenzhen 518060, China
3 Institute of Microelectronics, Shenzhen University, Shenzhen 518060, China
4 Guangdong Research Center for Interfacial Engineering of Functional Materials, Shenzhen University, Shenzhen 518060, China
5 State Key Laboratory of Radio Frequency Heterogeneous Integration, Shenzhen University, Shenzhen 518060, China
6 Shenzhen Baseus Technology Company Ltd., Shenzhen 518129, China
7 Jiangxi Yuhongjin Material Technology Company Ltd., Fuzhou 344100, China
8 Dongguan Sino Nitride Semiconductor Company Ltd., Dongguan 523270, China
9 Gensol (Shenzhen) Tech. Innovation Center Company Ltd., Shenzhen 518040, China
10 Department of Electronic Engineering, Chang Gung University, Taoyuan 333, Taiwan

CORRESPONDING AUTHOR: X. LIU (e-mail: xkliu@szu.edu.cn)

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(Linfei Gao and Ze Zhong contributed equally to this work.)

ABSTRACT In this work, we investigated the stability of a *p*-GaN gate with high electron mobility transistors (HEMTs) including an internal integrated gate circuit. A circuit was designed to improve *p*-GaN gate stability by using capacitance to release the hole into the *p*-GaN layer to mitigate the threshold voltage shift. Through pulse *I-V* measurement and positive bias temperature instability (PBTI) test, the carrier transporting behavior in the gate region achieved dynamic equilibrium at 5 V gate bias. The positive gate shift (ΔV_{TH}) of 0.4 V is observed with increasing voltage from 3 V to 8 V; ΔV_{TH} initially drops smoothly after release stresses by external capacitance discharge. Finally, integrated passive components and *p*-GaN gate HEMT circuit are recommended to mitigate the V_{TH} instability for E-mode HEMT.

INDEX TERMS *p*-GaN HEMT, pulse *I-V*, positive bias temperature instability (PBTI), threshold voltage, Stability, mechanism.

I. INTRODUCTION

Stability is one of the most critical characteristics needed for the adoption of power devices in areas of growing interest, such as the performance and lifetime of 5G base stations, new energy vehicles, satellite communication, fast charging source, and consumer electronics [1]. With the continuous improvement in the power density and efficiency of converters, wide bandgap semiconductor gallium nitride (GaN), and related technologies show highly competitive performance [2]. HEMTs have been widely studied since the 1990s due to their excellent electrical performance, including high operating temperature, high breakdown voltage, high electron mobility, wide band gap, high thermal conductivity, strong resistance to irradiation and so on. As the scope of the application continues to grow, extreme application conditions lead to a series of stability issues [3], which will restrict the application efficiency of GaN technology in high-power switching devices, thereby losing its unique advantages [4], [5]. It is therefore urgently necessary to analyse the stability issues of GaN power devices in applications, including cascode configuration, recessed gate structure, fluorine ion treatment, ultrathin barrier (UTB), and the p-type cap layer. Among them, the AlGaN/GaN HEMTs with *p*-GaN gate have been commercialized successfully and simultaneously

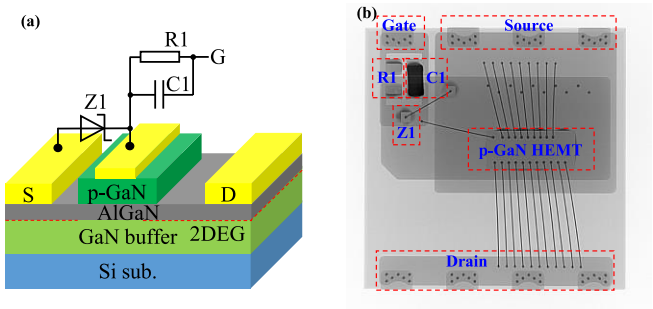

FIGURE 1. (a) Equivalent circuits of *p*-GaN HEMT/ Resistance/Capacitance/Zener diode. (b) HEMT X-ray.

demonstrate superior performance in practice. Previous work investigated the V_{TH} drift of *p*-GaN gate HEMTs with different gate structures [6], [7], [8], [9], [10], and both forward and negative V_{TH} drift has been observed which indicated different carrier injection and trapping behaviors at variable gate stress bias. P-type Schottky contacts may cause device degradation due to the presence of a high electric field at the metal/*p*-GaN interface [11], [12], [13], [14], [15]. The P-type gate also has ohmic contact [16]. In this case, the gate leakage may be slightly higher, but the absence of a depleted region (having a high peak field) at the metal/p-GaN interface can significantly improve stability. furthermore, there are still a few issues to resolve, such as the *p*-GaN gate HEMT which is most extensively used, and there was a discernible recovery from 1 to 10000 ms in the recovery phase. Switching off too fast will cause oscillation and burn the device. The instability of the working voltage will cause a change in power consumption, affect efficiency and increase the risk of failure.

In this work, a p-GaN gate HEMT circuit was used to improve gate steady-state characteristics. The use of a gate series capacitor alleviates the drastic changes in the turn-off and solves the problem of device failure caused by fast recovery. Resistance is used to limit current and prevent gate overcurrent. Diodes are used to stabilize the gate voltage and prevent breakdown. The V_{TH} instability would be investigated by pulse *I-V* measurement and PBTI tests. The I_{DS}-V_{GS} pulse test, V_{TH} shifting, and recovery process will all be precisely probed which achieved dynamic equilibrium at 5 V, and Slow recovery speed during the recovery process. This paper examined the gate dependability of *p*-GaN gate HEMTs at various voltages by temperature- and time-dependent gate V_{TH} instability (Section II). The gate deterioration behavior mechanisms under various voltages and temperatures are discussed in the discussion that follows (Section III), followed by a conclusion (Section IV).

II. DEVICE STATIC AND DYNAMIC PERFORMANCE

The devices under test (DUTs) are 650 V/10 A *p*-GaN gate HEMTs (Gannitride. China). The circuit composition is plotted in Fig. 1(a), A *p*-GaN HEMTs, 10 Ω resistor, 47 nF capacitance, and 6.5 V zener diode. The X-ray diagram of

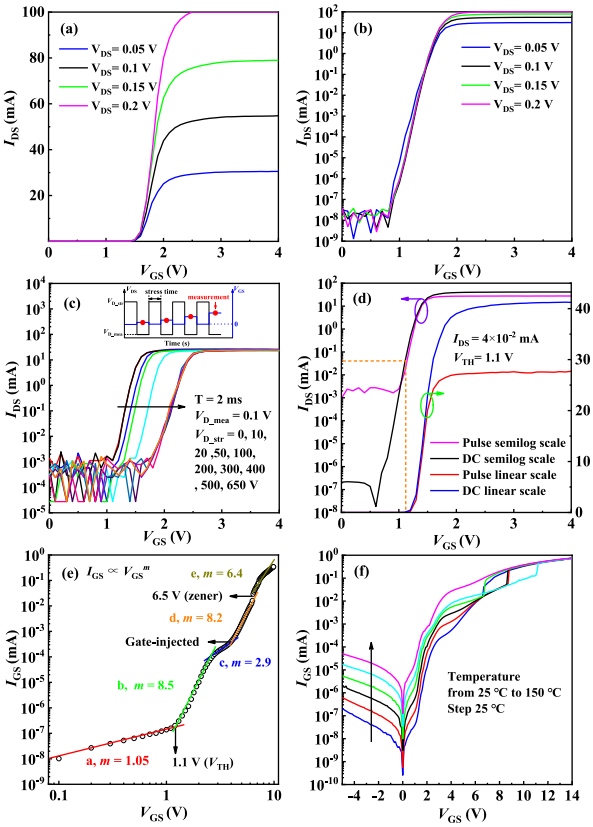

FIGURE 2. (a) Transfer I_{DS}-V_{GS} linear characteristics of *p*-GaN gate HEMT. (b) Transfer I_{DS}-V_{GS} semi-logarithmic characteristics of *p*-GaN gate HEMT. (c) Transfer I_{DS}-V_{GS} characteristics of *p*-GaN gate HEMT in different drain stress. (d) Characteristics of *p*-GaN gate HEMT DC I_{DS}-V_{GS} and Pulse I_{DS}-V_{GS} at semi-logarithmic and linear scales. (e) The *p*-GaN gate HEMT's I_G different rising slopes. (f) The *p*-GaN gate HEMT's I_G properties at various temperatures.

DUT is shown in Fig. 1(b). The *p*-GaN gate HEMT device circuits have been analyzed in detail. on-resistance (R_{ON}) of 150 mΩ at V_{GS} = 10 V, I_D = 5 A, T_J = 25 °C, Qg = 2.8 nC, Ciss = 80 pF, Coss = 50 pF, Crss = 1 pF. Series resistors can limit gate current, form RC circuits with HEMT parasitic capacitors to reduce the frequency response of the circuit, increase the circuit phase stability margin, and prevent the breakdown of HEMTs due to fast switching speed. The parallel Zener diode can eliminate the voltage mutation between the drain and source, which can be coupled to the gate through the interelectrode capacitance and resulting in a spike voltage. When the gate voltage exceeds the Zener diode reverse breakdown, the gate voltage is stabilized at about 6.5V. The capacitance is connected in parallel at the gate resistance to eliminate the noise coupled to the *p*-GaN HEMT circuit, increasing the drop time when the gate is turned off, and providing a delay to improve the stability of the device [17], [18], [19].

As shown in Fig. 2(a), 0.1 V drain voltage was selected to exclude trapping effects caused by drain side stress. Since the voltage of 0.05 V may be too low and the curve will be deformed, 0.05 V is excluded in Fig. 2(b). We have to test

the V_{TH} under different drain stress. The greater the drain stress voltage, the greater the V_{TH}, V_{DS} = 0.1 V is selected to exclude the influence of drain voltage on the threshold voltage in Fig. 2(c). The static and dynamic transfer curve characteristic was shown in Fig. 2(d), featuring both threshold voltages (V_{TH}) is 1.1 V defined at $I_{DS} = 4\times10^{-2}$ mA with V_{DS} = 0.1 V. Fig. 2(e) shows the lg I_{GS}–lg V_{GS} in positive V_{GS}. By fitting with $I_{GS} \propto V_{GS}^{m}$, the lg I_{GS}–lg V_{GS} curve can be divided into five sections (i.e., a, b, c, d e) with different power-law exponent m, which indicates different conduction mechanisms. The region a device is not turned on. The region b device is on at low voltage, Once V_{GS} > 1.2 V, I_{GS} exhibits a steep increase with m = 8.5. This saturation knee, at a gate bias of 3 V, m > 2 is typical for space-charge-limited conduction (SCLC) associated with trap filling [20]. Typically, due to the AlGaN lay electron mobility being low, the injected electrons are confined in traps leading to the generation of space charges that impede the subsequent transport of electrons across the AlGaN barrier [21]. By this means, the gate current will rise slowly in regions c. Meanwhile, electrons are accumulating in the 2DEG channel with increasing V_{GS}, resulting in an enhanced channel conductivity. When the positive gate bias is greater than 4 V in region d, the effective hole injection is triggered, which will result in a second rising slope of I_{GS} in the power law exponent m of 8.2. Subsequently, in region e, Zener diode voltage stabilization is triggered, the power-law exponent m decreases and current I_{GS} gradually tends to saturation. Fig. 1(f) illustrates the static temperature-dependent I_{GS} characterization gate current (I_{GS}–V_{GS}) through the *p*-GaN gate HEMT, the gate leakage current is proportional to temperature from 25 °C to 150 °C.

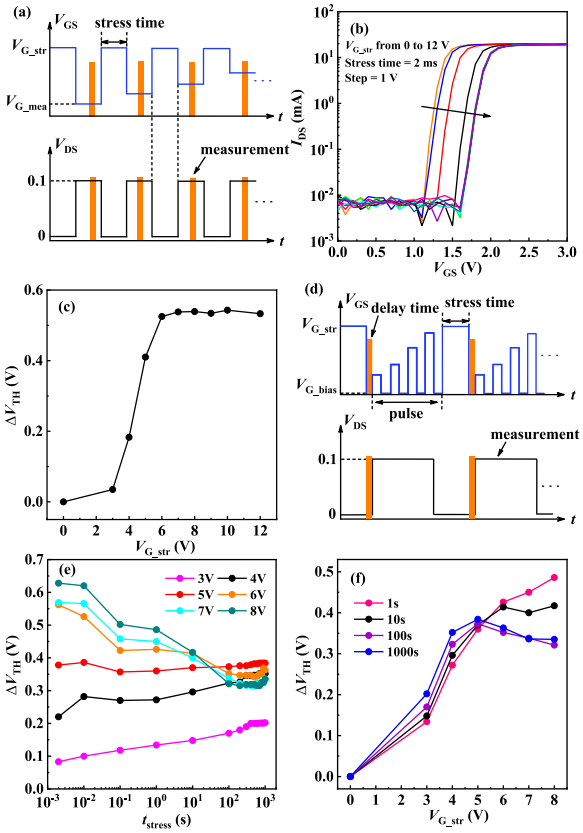

FIGURE 3. (a) B1500A set pulse *I-V* measurement waveform program. (b) The *p*-GaN gate HEMT pulsed transfer I_{DS}-V_{GS} characteristics under various gate stress biases. (c) Extracted ΔV_{TH} under various gate stress biases. (d) Waveform procedures for the PBTI test. ΔV_{TH} characteristics of *p*-GaN gate HEMT circuit under PBTI test with various (e) stress time and (f) gate stress biases.

III. MEASUREMENT AND ANALYSIS

The pulsed curve (I_{DS}–V_{GS}) measure was set by the power semiconductor parameter analyzer Keysight B1500A. The waveforms of drain and gate bias for this test are illustrated in Fig. 3(a). For the dynamic positive gate stress, apply a continuous square wave pulse of 500 Hz at the gate terminal. The stress time is 2 ms. The pulse duty cycle is 50% and the measure delay time is 1 ms. Use the static transfer method to determine V_{TH}. Use the V_{GS_m} measurement window of 0 ∼ 3 V to monitor different gate bias stresses (V_{G_str}). Fig. 3(b) reveals the pulsed *I-V* features of the DUT with V_{G_str} at 1 V steps from 0 to 12 V. The rising edge of transfer curves are nearly parallel to each other, with V_{G_str} increased V_{TH} of *p*-GaN gate HEMTs keeps shifting positively [see Fig. 3(c)]. At 6 V it becomes saturated and stable. The PBTI test is performed with a set of continuous on-state gate biases and a set of pulsed *I-V* measurements [22]. Fig. 3(d) shows the waveforms of the drain and gate voltages in the pulse delivery test. Continuous stress square wave pulse of 1KHz at the gate terminal. The stress time is 1 ms and the pulse duty cycle is 50%. The measured voltage is pulse 0 – 3 V step 0.1 V, and a delay time is 1 ms. Fig. 3(e) shows ΔV_{TH} vs. Stress time and gate biases curves of PBTI tests. When V_{GS} increased from 3 V to 4 V, the slope of the time-dependent ΔV_{TH} curve increased. When V_{GS} increased from 6 V to 8 V, the slope of the time-dependent ΔV_{TH} curve decreased obviously, and the dynamic equilibrium point is V_{GS} = 5 V (slope = 0 V/s) [21], [23], [24], [25]. Under long-term stress, an apparent stable ΔV_{TH} was observed in ΔV_{TH} of |0.4 V|, and positive V_{TH} instability of *p*-GaN gate HEMT remains well-confined. As shown in Fig. 3(f) the static equilibrium point of V_{GS} = 5 V is demonstrated more significantly.

Since power transistors usually operate at higher temperatures, the reliability of the gate is studied. The DC feature of I_{DS}-V_{DS} is characterized by the temperature range of 25 ∼ 150 °C [4], [27]. As shown in Fig. 4(a), at longer stress times and higher temperatures, there is still a negative temperature dependence [28]. Decremental ΔV_{TH} evolution of the DUT was carried out in the stress time interval of 25 ∼ 150 °C and 1 ∼ 1000 s. It is worth noticing that time-dependent V_{TH} began to decline with stress time when the temperature increased to 75 °C. Moreover, after 5 V gate stress, V_{TH} shows a distinctly stable recovery rate from 1 to 10000 ms [see Fig. 4(b)], this phenomenon was not found in traditional *p*-GaN gate HEMTs [29], [30], showing an additional stress-time dependence independent of pressure processes related to electron capture in the gate region of the six mechanisms. All repairs can be completed within 500 seconds.

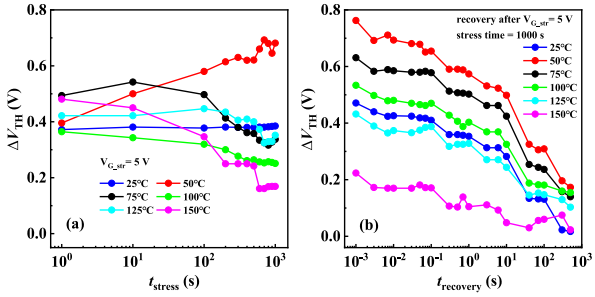

FIGURE 4. **(a) ΔV_{TH} evolution of *p*-GaN gate HEMT at various temperatures in PBTI experiments. (b) ΔV_{TH} recovery as a function of temperature after 1000 s of gate bias stress.**

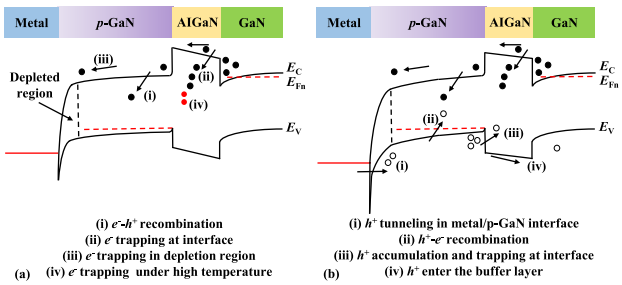

FIGURE 5. **The *p*-GaN gate HEMT gate's schematic band diagram shows (a) electron trapping as the dominating process at comparatively low V_{G_str} and (b) strengthen hole-related activities at high V_{G_str} or high temperatures. The holes tunnel from the metal/*p*-GaN contact to the *p*-GaN, AlGaN, and GaN buffer. Then, free holes appear in the *p*-GaN valence band.**

From the above observations of the bias voltage, temperature, and *I-V* characteristics, the carrier transport process of Schottky *p*-GaN gate HEMT under positive gate stress can be explained [31], [32]. The schematic electron trapping energy band diagram and the p-n heterojunction of the *p*-GaN gate HEMT's gate stack under positive gate stress is shown in Fig. 5(a). The metal/*p*-GaN Schottky junction is reverse-biased and the metal/*p*-GaN interface has a depletion layer, while the p-n heterojunction is forward-biased. The electrons in 2DEG will spill over and flow into the AlGaN layer due to the emission of hot electrons, some electrons are trapped by defects in this layer [process(ii)], and others injected electrons could arrive at the depleted *p*-GaN region and subsequently flows into the gate electrode in the strong electric field [9], [33]. The potential of the *p*-GaN gate will turn negative gradually and V_{TH} shifts positively [34]. Moreover, light emission should occur in the *p*-GaN layer due to the electrons which finally flow to depletion [process (iii)] area multiple-step transitions (Bremsstrahlung) [35], and the electrons may also recombine with the holes present in the *p*-GaN layer [process (i)] and recent studies show an intense yellow (2.25 eV) light [36], which coincides with the defect-assisted synthesis in the *p*-GaN layer. Lots of hot holes will release energy enter into the lattice and generate more defects as the temperature increases. These defects combined with electrons from 2DEG, lead to positive ΔV_{TH} [process (iv)]. With the increasing gate bias stress [37], the dependence of V_{TH} on V_{G_str} transforms from positive to negative with the prolongation of stress time [see Fig. 3(e)], electron capture mechanism of the process [38]. The positive V_{TH} can be alleviated via the metal/*p*-GaN interface tunnelling [process (i)], electrons and holes recombination [process (ii)], hole-assisted de-trapping and hole accumulation [process (iii)] at the *p*-GaN/AlGaN interface [see Fig. 5(b)], it reaches dynamic equilibrium at 5 V and remains stable [see Fig. 3(e) and Fig. 3(f)]. With the temperature going up, the actual thickness of the Schottky barrier reduces, and this hole injection process [process (i)] becomes significant [39], [40], [41]. During the recovery phase, the initially slow decline of ΔV_{TH} can be explained by the facts that capacitor C1 can be discharged to a low level through an RC circuit that consists of capacitor C1 and resistor R1 [17], [18], [19]. Capacitor C1 is connected in parallel to a 10ohm resistance leading to an RC time constant that is much smaller than 10 s, and a small number of holes are injected into the p-GaN layer [process (i)] [42]. It alleviates the rapid loss of holes caused by the shutdown and maintains for a short time. ΔV_{TH} shows that it gradually recovers below 0.3 V from 1 to 10000 ms [43]. After 10000 ms recovery, no external charge enters the *p*-GaN layer. Hole accumulation at the p-GaN/AlGaN interface, hole trapping in the AlGaN layer, and de-trapping of electrons via tunnelling, photon pumping, or hole recombination. The electrons and holes eventually return to their initial stability, and a full recovery can be obtained within more time.

IV. CONCLUSION

In summary, it has been investigated that temperature-dependent and time-resolved gate degradation induced by positive gate bias stress on a *p*-GaN gate HEMT with an internal integrated gate circuit. The positive ΔV_{TH} is 0.4 V when the V_{GS} is increased from 3 V to 8 V. The *p*-GaN gate HEMT circuit is suitable for long-term operation at V_{GS} = 5 V and high-temperature conditions. The significance of V_{TH} and the revealed mechanism in this work demonstrate the potential for the application of *p*-GaN gate HEMT devices.

REFERENCES

[1] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A Survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron*, vol. 29, no. 5, pp. 2155–2163, May 2014, doi: 10.1109/TPEL.2013.2268900.

[2] K. J. Chen et al., "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017, doi: 10.1109/TED.2017.2657579.

[3] M. Meneghini et al., "Reliability and failure analysis in power GaN-HEMTs: An overview," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Monterey, CA, USA, 2017, pp. 3B-2.1–3B-2.8, doi: 10.1109/IRPS.2017.7936282.

[4] H. Wu, X. Fu, J. Guo, Y. Wang, T. Liu, and S. Hu, "Time-resolved threshold voltage instability of 650-V Schottky type p-GaN gate HEMT under temperature-dependent forward and reverse gate bias conditions," *IEEE Trans. Electron Devices*, vol. 69, no. 2, pp. 531–535, Feb. 2022, doi: 10.1109/TED.2021.3140188.

[5] A. N. Tallarico et al., "Gate reliability of p-GaN HEMT with gate metal retraction," *IEEE Trans. Electron Devices*, vol. 66, no. 11, pp. 4829–4835, Nov. 2019, doi: 10.1109/TED.2019.2938598.

[6] K. Murukesan, L. Efthymiou, and F. Udrea, "Gate stress induced threshold voltage instability and its significance for reliable threshold voltage measurement in p-GaN HEMT," in *Proc. IEEE 7th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Raleigh, NC, USA, 2019, pp. 177–180, doi: 10.1109/WiPDA46397.2019.8998859.
[7] M. Hua, C. Wang, J. Chen, L. Zhang, Z. Zheng, and K. J. Chen, "Gate reliability and VTH stability investigations of p-GaN HEMTs," in *Proc. IEEE 15th Int. Conf. Solid-State Integr. Circuit Technol. (ICSICT)*, Kunming, China, 2020, pp. 1–4, doi: 10.1109/ICSICT49897.2020.9278305.
[8] R. Wang et al., "V-T shift and recovery mechanisms of p-GaN gate HEMTs under DC/AC gate stress investigated by fast sweeping characterization," *IEEE Electron Device Lett.*, vol. 42, no. 10, pp. 1508–1511, Oct. 2021, doi: 10.1109/LED.2021.3104852.
[9] J. He, J. Wei, S. Yang, Y. Wang, K. Zhong, and K. J. Chen, "Frequency- and temperature-dependent gate reliability of Schottky-type p-GaN gate HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3453–3458, Aug. 2019, doi: 10.1109/TED.2019.2924675.
[10] A. N. Tallarico, S. Stoffels, N. Posthuma, S. Decoutere, E. Sangiorgi, and C. Fiegna, "Threshold voltage instability in GaN HEMTs with p-type gate: Mg doping compensation," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 518–521, Apr. 2019, doi: 10.1109/LED.2019.2897911.
[11] Q. Bao, S. Yang, and K. Sheng, "UIS withstanding capability of GaN E-HEMTs with Schottky and Ohmic p-GaN contact," in *Proc. 32nd Int. Symp. Power Semicond. Devices ICs (ISPSD)*, Vienna, Austria, 2020, pp. 337–340, doi: 10.1109/ISPSD46842.2020.9170105.
[12] J. O. Gonzalez, B. Etoz, and O. Alatise, "Characterizing threshold voltage shifts and recovery in Schottky gate and Ohmic gate GaN HEMTs," in *Proc. IEEE Energy Convers. Congr. Expos. (ECCE)*, Detroit, MI, USA, 2020, pp. 217–224, doi: 10.1109/ECCE44975.2020.9235650.
[13] A. N. Tallarico et al., "Investigation of the p-GaN gate breakdown in forward-biased GaN-based power HEMTs," *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 99–102, Jan. 2017, doi: 10.1109/LED.2016.2631640.
[14] I. Rossetto et al., "Field- and current-driven degradation of GaN-based power HEMTs with p-GaN gate: Dependence on Mg-doping level," *Microelectron. Rel.*, vols. 76–77, pp. 298–303, Sep. 2017, doi: 10.1016/j.microrel.2017.06.061.
[15] Y. Uemoto et al., "Gate injection transistor (GIT)—A normally-off AlGaN/GaN power transistor using conductivity modulation," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3393–3399, Dec. 2007, doi: 10.1109/IEDM.2006.346930.
[16] K. Murukesan, L. Efthymiou, and F. Udrea, "On the challenges of reliable threshold voltage measurement in Ohmic and Schottky gate p-GaN HEMTs," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 831–838, 2021, doi: 10.1109/JEDS.2021.3111809.
[17] P.-C. Chuang, "Waveform conversion circuit for gate driver," U.S. Patent 10 498 324 B2, Dec. 2019.
[18] P.-C. Chuang, "Waveform conversion circuit for gate driver," U.S. Patent 10 348 286 B2, Jul. 2019.
[19] "Waveform conversion circuit and gate-drive circuit," Taiwanese Patent 170 279 8B, Aug. 2020.
[20] A. Rose, "Space-charge-limited currents in solids," *Phys. Rev*, vol. 97, no. 6, pp. 1538–1544, Mar. 1955, doi: 10.1103/PhysRev.97.1538.
[21] Y. Shi et al., "Carrier transport mechanisms underlying the bidirectional VTH shift in p-GaN gate HEMTs under forward gate stress," *IEEE Trans. Electron Devices*, vol. 66, no. 2, pp. 876–882, Feb. 2019, doi: 10.1109/TED.2018.2883573.
[22] A. N. Tallarico et al., "PBTI in GaN-HEMTs with p-type gate: Role of the aluminum content on ΔVTH and underlying degradation mechanisms," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 38–44, Jan. 2018, doi: 10.1109/TED.2017.2769167.
[23] X. Li et al., "Observation of dynamic V_{TH} of p-GaN gate HEMTs by fast sweeping characterization," *IEEE Electron Device Lett.*, vol. 41, no. 4, pp. 577–580, Apr. 2020, doi: 10.1109/LED.2020.2972971.
[24] Y. Sun, M. Wang, W. Lei, and C. Han "Dynamic gate leakage current of p-GaN gate AIGaN/GaN HEMT under positive bias conditions," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. Asia (WiPDA Asia)*, Wuhan, China, 2021, pp. 232–235, doi: 10.1109/WIPDAASIA51810.2021.9656087.
[25] B. Li, H. Li, J. Wang, and X. Tang, "Asymmetric bipolar injection in a Schottky-metal/p-GaN/AlGaN/GaN device under forward bias," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1389–1392, Sep. 2019, doi: 10.1109/LED.2019.2926503.
[26] F. Yang, C. Xu, and B. Akin, "Characterization of threshold voltage instability under off-state drain stress and its impact on p-GaN HEMT performance," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4026–4035, Aug. 2021, doi: 10.1109/JESTPE.2020.2970335.
[27] C.-T. Ma and Z.-H. Gu, "Review on driving circuits for wide-bandgap semiconductor switching devices for mid- to high-power applications," *Micromachines*, vol. 12, no. 1, p. 65, Jan. 2021, doi: 10.3390/mi12010065.
[28] X. Chen et al., "Influence of the carrier behaviors in p-GaN gate on the threshold voltage instability in the normally off high electron mobility transistor," *Appl. Phys. Lett.*, vol. 119, no. 6, Aug. 2021, Art. no. 63501, doi: 10.1063/5.0055530.
[29] J. He, G. Tang, and K. J. Chen, "VTH instability of p-GaN gate HEMTs under static and dynamic gate stress," *IEEE Electron Device Lett.*, vol. 39, no. 10, pp. 1576–1579, Oct. 2018, doi: 10.1109/LED.2018.2867938.
[30] X. Chao et al., "Analysis of VTH degradation and recovery behaviors of p-GaN gate HEMTs under forward gate bias," *IEEE Trans. Electron Devices*, vol. 70, no. 6, pp. 2970–2974, Jun. 2023, doi: 10.1109/TED.2023.3263819.
[31] A. Stockman and P. Moens, "ON-state gate stress induced threshold voltage instabilities in p-GaN gate AlGaN/GaN HEMTs," in *Proc. IEEE Int. Integr. Rel. Workshop (IIRW)*, South Lake Tahoe, CA, USA, 2020, pp. 1–4, doi: 10.1109/IIRW49815.2020.9312869.
[32] X. Tang, B. Li, H. A. Moghadam, P. Tanner, J. Han, and S. Dimitrijev, "Mechanism of threshold voltage shift in p-GaN gate AlGaN/GaN transistors," *IEEE Electron Device Lett.*, vol. 39, no. 8, pp. 1145–1148, Aug. 2018, doi: 10.1109/LED.2018.2847669.
[33] Z. Jiang, L. Li, C. Wang, J. Zhao, and M. Hua, "Gate-bias induced threshold voltage (VTH) instability in P-N junction/AlGaN/GaN HEMT," *IEEE Trans. Electron Devices*, vol. 69, no. 7, pp. 3654–3659, Jul. 2022, doi: 10.1109/TED.2022.3177397.
[34] L. Zhang, Z. Zheng, S. Yang, W. Song, J. He, and K. J. Chen, "p-GaN gate HEMT with surface reinforcement for enhanced gate reliability," *IEEE Electron Device Lett.*, vol. 42, no. 1, pp. 22–25, Jan. 2021, doi: 10.1109/LED.2020.3037186.
[35] M. Meneghini, O. Hilt, J. Wuerfl, and G. Meneghesso, "Technology and reliability of normally-off GaN HEMTs with p-type gate," *Energies*, vol. 10, no. 2, pp. 1–15, Feb. 2017, doi: 10.3390/en10020153.
[36] I. Rossetto et al., "Time-dependent failure of GaN-on-Si power HEMTs with p-GaN gate," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2334–2339, Jun. 2016, doi: 10.1109/TED.2016.2553721.
[37] X. Tang et al., "Demonstration of electron/hole injections in the gate of p-GaN/AlGaN/GaN power transistors and their effect on device dynamic performance," in *Proc. 31st Int. Symp. Power Semicond. Devices ICs (ISPSD)*, Shanghai, China, 2019, pp. 415–418, doi: 10.1109/ISPSD.2019.8757614.
[38] L. Efthymiou, K. Murukesan, G. Longobardi, F. Udrea, A. Shibib, and K. Terrill, "Understanding the threshold voltage instability during OFF-state stress in p-GaN HEMTs," *IEEE Electron Device Lett.*, vol. 40, no. 8, pp. 1253–1256, Aug. 2019, doi: 10.1109/LED.2019.2925776.
[39] L. Sayadi, G. Iannaccone, S. Sicre, O. Haberlen, and G. Curatola, "Threshold voltage instability in p-GaN gate AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2454–2460, Jun. 2018, doi: 10.1109/TED.2018.2828702.
[40] H. Xu, J. Wei, R. Xie, Z. Zheng, J. He, and K. J. Chen, "Incorporating the dynamic threshold voltage into the SPICE model of Schottky-type p-GaN gate power HEMTs," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5904–5914, May 2021, doi: 10.1109/TPEL.2020.3030708.
[41] A. Stockman et al., "Gate conduction mechanisms and lifetime modeling of p-gate AlGaN/GaN high-electron-mobility transistors," *IEEE Trans. Electron Devices*, vol. 65, no. 12, pp. 5365–5372, Dec. 2018, doi: 10.1109/TED.2018.2877262.
[42] W. Vandendaele et al., "A novel insight of pBTI degradation in GaN-on-Si E-mode MOSc-HEMT," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Burlingame, CA, USA. 2018, pp. 4B.2-1–4B.2-6, doi: 10.1109/IRPS.2018.8353580.
[43] M. Ruzzarin et al., "Degradation mechanisms of GaN HEMTs With p-type gate under forward gate bias overstress," *IEEE Trans. Electron Devices*, vol. 65, no. 7, pp. 2778–2783, Jul. 2018, doi: 10.1109/TED.2018.2836460.