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# High-Performance of InGaZnO TFTs With an Ultrathin 5-nm $Al_2O_3$ Gate Dielectric Enabled by a Novel Atomic Layer Deposition Method

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**ABSTRACT** $Al_2O_3$, as one of the gate dielectric materials for thin film transistors (TFTs), has been extensively investigated because of its large bandgap, high breakdown field, and good thermal stability. However, the further development of $Al_2O_3$ thin films is limited by the presence of defects such as oxygen vacancies, self-interstitial atoms, or impurity elements. To overcome this obstacle, we have developed a novel method for fabricating $Al_2O_3$ thin films by using the atomic layer deposition (ALD) technique. This method replaces the conventional Trimethylaluminium (TMA)/$H_2O$ cycles with TMA/TMA/$H_2O$/$H_2O$ cycles (referred to as 'double cycles'), to deposit the $Al_2O_3$. The 5-nm ultrathin $Al_2O_3$ film showed a high areal capacitance of 660 nF/cm$^2$ at 20 Hz, and a relatively low current density of $10^{-8}$ A/cm$^2$ at 1 MV/cm. InGaZnO (IGZO) TFTs with ultrathin $Al_2O_3$ gate dielectric grown by double cycles exhibited outstanding performances, such as a near theoretical limit subthreshold swing (*SS*) of 70 mV/decade, a higher on/off current ratio ($I_{on}/I_{off}$) of $10^6$, an increased field-effect mobility ($\mu$) of 6.5 cm$^2$/Vs, a lower threshold voltage ($V_{th}$) of 0.2 V, and a low operating voltage of 3 V. These results are superior to the IGZO TFTs with $Al_2O_3$ dielectrics deposited using the single TMA/$H_2O$ cycle. Therefore, the implementation of 'double cycles' in the fabrication of dielectrics through ALD demonstrates considerable potential for future application in low-power electronic devices.

**INDEX TERMS** Ultrathin $Al_2O_3$, atomic layer deposition, double cycles, thin film transistor.

## I. INTRODUCTION

In recent years, thin film transistors (TFTs) have found extensive applications in various domains, including wearable electronic devices, [1] sensors, [2] and integrated circuits [3]. With the rapid advancement of semiconductor technology, achieving low voltage operation and minimizing power consumption has become imperative for portable and battery-powered applications. Currently, there are two primary methods for reducing the operating voltage of TFTs: (1) utilizing high dielectric constant (high-*k*) materials; (2) diminishing the thickness of the gate dielectric layer. Both strategies would enhance the capacitance per unit, thereby lowering the voltage threshold for efficient operation.

Many researchers have attempted to lower the operating voltage of TFTs by using high-*k* materials, such as $ZrO_2$ [4], $Ta_2O_5$ [5], $Y_2O_3$ [6], and $HfO_2$ [7]. Yang et al. reported the utilization of a 5-nm $ZrO_2$ gate dielectric layer in low-voltage ZnO TFTs, which exhibits the lowest operating voltage of 1 V and a large field effect mobility of 36.8 cm$^2$/Vs [4]. Cheng et al. further demonstrated that the IGZO TFT with 15.5-nm $LaAlO_3$ dielectric exhibited excellent electrical performance, including a low $V_{th}$ of 0.42 V and a small *SS* of 68 mV/decade [8]. However, retaining an amorphous state at high temperatures poses a considerable challenge for numerous high-*k* materials, ultimately leading to an increase in gate leakage current. This phenomenon arises due to the

tendency of the leakage current to propagate along grain boundaries when the material undergoes amorphous structure degradation at elevated temperatures. [9], [10] Among the various high-$k$ materials, $Al_2O_3$ has gained considerable attention and utilization due to its high crystallization temperature, large bandgap, high breakdown field, good thermal stability, and ease of fabrication [11]. What's more, oxygen vacancies and impurity element defects have been identified as contributors to carrier scattering and trapping, thereby degrading the electrical performance of TFTs. These defects can also cause TFT bias stability issues, such as threshold voltage drift [12].

Up to now, common methods for preparing $Al_2O_3$ thin films include magnetron sputtering [13], sol-gel [14], and ALD [15]. However, thin films grown by magnetron sputtering can lead to surface scattering and deterioration of the device's stability. Meanwhile, it is challenging to control the film thickness accurately. The solution process has several drawbacks, including the requirement for high annealing temperatures, poor film roughness, and limited process repeatability. As a result, the thin films exhibit a higher density of lattice defects, leading to diminished performance compared to films prepared using alternative growth methods.

It is well-known that ALD enables precise control over the thickness and composition of grown films, offering advantages such as excellent uniformity, step coverage, minimal defect density, low deposition temperature, and excellent reproducibility [16]. In this study, we have proposed a novel deposition concept, wherein $Al_2O_3$ films are deposited using a modified sequence of TMA/TMA/$H_2O$/$H_2O$ cycles instead of the conventional TMA/$H_2O$ cycles. The 5-nm ultrathin $Al_2O_3$ film deposited by 'double cycles' showed a high areal capacitance of 660 nF/cm$^2$ at 20 Hz, and a relatively low current density of $10^{-8}$ A/cm$^2$ at 1 MV/cm. What's more, TFTs fabricated with $Al_2O_3$ thin films deposited using the 'double cycles' exhibit superior performance, such as a near theoretical limit $SS$ of 70 mV/decade, an enhanced $I_{on}/I_{off}$ of $10^6$, an increased $\mu$ of 6.5 cm$^2$/Vs, and a reduced $V_{th}$ of 0.2 V.

## II. EXPERIMENTS

The $Al_2O_3$ thin films were deposited using a thermal ALD reactor (TFS-200 BENEQ). TMA and deionized water were used as Al and oxygen sources, respectively. The conventional approach for $Al_2O_3$ fabrication involves alternating precursors, TMA/Purge/$H_2O$/Purge. In contrast, our approach utilizes a modified sequence of TMA/Purge/TMA/Purge/$H_2O$/Purge/$H_2O$/Purge to achieve a better quality of $Al_2O_3$ dielectrics, as shown in Figure 1. The deposition cycle is comprised of several sequential steps. First, a TMA pulse is applied for a duration of 200 ms. This is followed by a 10 second purge with nitrogen gas ($N_2$). Next, another TMA pulse is administered for an identical duration of 200 ms, which is subsequently succeeded by another 10 second $N_2$ purge. The subsequent

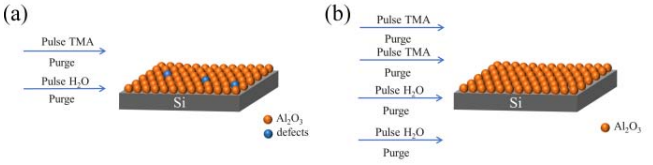


**FIGURE 1. (a) The conventional fabrication processes and (b) the 'double cycles' process for $Al_2O_3$ thin films.**

step involves introducing a pulse of water vapor ($H_2O$) for 200 ms, followed once again by a 10 second $N_2$ purge. Finally, a second $H_2O$ vapor pulse is introduced for 200 ms, culminating in a final 10 second $N_2$ purge. These sequential steps constitute a complete deposition cycle. Before the deposition process, the highly doped p-Si substrate is cleaned by sonication in acetone, alcohol, and deionized water for 15 min each, followed by drying with a nitrogen flow. Then, a thin layer of approximately 5-nm-thick $Al_2O_3$ is grown on the silicon substrate using ALD at 250 °C [17]. Next, a 22 nm IGZO active layer was deposited by RF sputtering at room temperature. Finally, TFT devices with a channel width ($W$) of 500 $\mu$m and a channel length ($L$) of 100 $\mu$m are defined using Al films deposited by thermal evaporation. These devices are then annealed in air at 300 °C on a hot plate for 15 min.

To investigate the electrical performance of $Al_2O_3$ dielectrics under different processes, two different types of IGZO TFTs were fabricated with $Al_2O_3$: one using the conventional fabrication cycles (TMA/$H_2O$, referred to as 'device A') and the other with twice the number of cycles (TMA/TMA/$H_2O$/$H_2O$, referred to as 'device B').

The $\mu$ and $SS$ are extracted using the following equations:

$$I_D = \left(\frac{W}{2L} C_i \mu\right)(V_G - V_{\text{th}})^2 \tag{1}$$

$$SS = \frac{dV_G}{d(\log I_D)} \tag{2}$$

here, $W$ and $L$ represent the channel width and length, respectively. $C_i$ denotes the capacitance per unit area of the dielectric, $V_{th}$ represents the threshold voltage, and $V_G$ corresponds to the gate voltage.

The fabricated samples were characterized using transmission electron microscopy (TEM, Talos F200S) and an atomic force microscope (AFM, nanonaviSPA-400 SPM, SII Nano Technology Inc. Chiba City, Japan) for structural and morphological analysis. The electrical performance of the samples was characterized using a semiconductor parameter analyzer (Keithley, 4200, Cleveland, OH, USA) and probe station (Lakeshore, TTP4, Carson, CA, USA).

## III. RESULTS AND DISCUSSION

The quality of the ultrathin $Al_2O_3$ film was assessed by examining 2×2 $\mu$m AFM images, as shown in Figures 2(a) and (b). The root-mean-square (RMS) roughness of the 5-nm $Al_2O_3$ film grown using 'double cycles' was measured to be as low as 1.06 nm, whereas that of thin film grown using

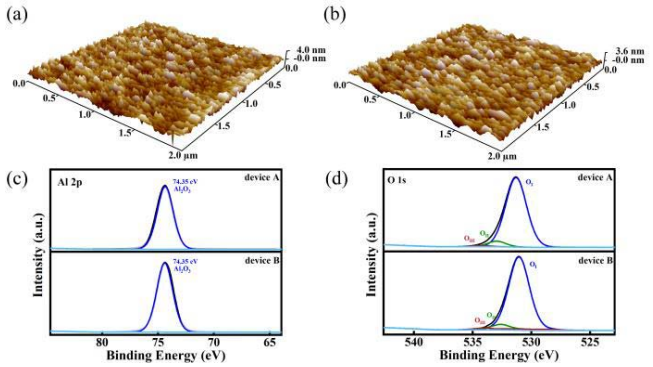


**FIGURE 2.** **AFM images of $Al_2O_3$ deposited with (a) the traditional cycles and (b) the novel cycles. XPS of (c) Al 2p, (d) O 1s for thin films.**

conventional cycles was found to be 1.15 nm. Compared with the conventional process, the surface morphology of film grown with the novel process was obviously improved. This improvement may be attributed to the use of a 'double cycles' process, which can reduce defects such as oxygen vacancies, interstitial atoms, or impurity elements in $Al_2O_3$. Additionally, XPS spectra were conducted to investigate the chemical states of the $Al_2O_3$ gate dielectrics, as illustrated in Figures 2(c) and (d). All peaks were calibrated with respect to C 1s. The corresponding Al narrow scans are presented in Figure 2(c). The O 1s spectra were subjected to fitting using three component peaks: $O_I$ (529.5 eV), $O_{II}$ (531.2 eV), and $O_{III}$ (532.8 eV). $O_I$ is associated with $O^{2-}$ within the crystal structure surrounded by $Al^{3+}$. $O_{II}$ is linked to oxygen vacancies in the $Al_2O_3$ film, while $O_{III}$ is attributed to adsorbed oxygen, such as $H_2O$. Analysis reveals that Device A indeed contains a higher concentration of oxygen vacancies (6.37%) compared to Device B (4.67%), indicating the efficacy of the new process in mitigating the presence of oxygen vacancies.

Figure 3 shows the cross-sectional TEM images and the energy dispersive spectroscopy mapping of Al, O, In, Ga, and Zn distributions in device B. Figures 3 (a) and (b) reveal that the ultrathin $Al_2O_3$ gate dielectric has a uniform interface with the IGZO layer and a physical thickness of 5-nm. Additionally, the energy mapping in Figures 3 (c) and (d) demonstrate that a homogeneous distribution of the thin film can be achieved using the ALD method. The IGZO composition is presented in Tab. 1.

It has been observed that ultrathin dielectrics exhibit properties distinct from those of thick dielectrics [18]. Before the fabrication of IGZO TFTs, p-Si/$Al_2O_3$/Al capacitors were fabricated to measure leakage current density, capacitance-frequency, and capacitance-voltage characteristics (Figure 4a). The leakage current characteristics of devices A and B are illustrated in Figure 4 (b). It is evident that the leakage current density of device B is approximately two orders of magnitude lower than that of device A. At the electric field of 1 MV/cm, device B demonstrates a leakage current of only $10^{-8}$ A/cm$^2$, which is notably lower than the leakage current of $10^{-7}$ A/cm$^2$ observed in device A.

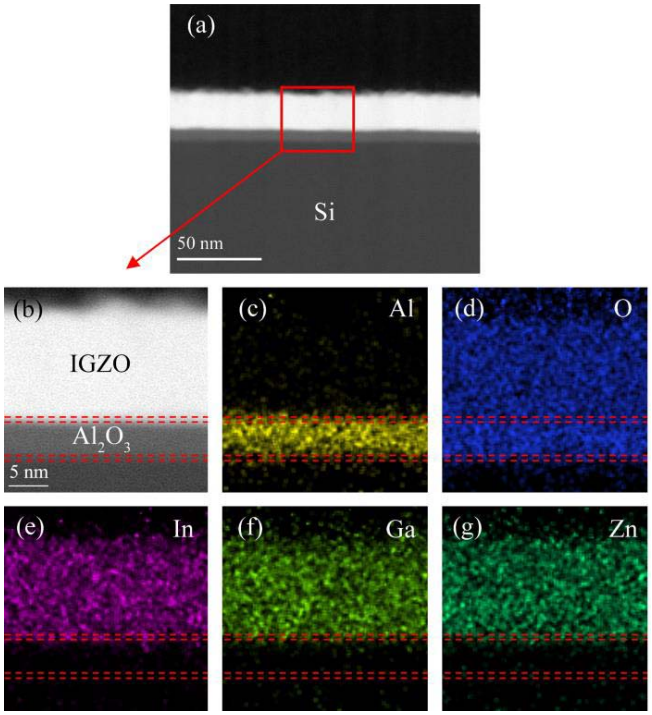


**FIGURE 3.** **(a) and (b) are cross-sectional TEM images of device B. Energy dispersive spectroscopy mapping shows the distribution of (c) Al, (d) O, (e) In, (f) Ga, and (g) Zn.**

**TABLE 1.** **Analysis of spectrum: Spectra from area.**

| Element | C | N | O | Al | Si | Zn | Ga | In |
|---|---|---|---|---|---|---|---|---|
| Atomic Fraction (%) | 19.3 | 2.8 | 35.0 | 6.1 | 13.5 | 8.7 | 8.2 | 6.1 |
| Atomic Error (%) | 2.2 | 0.6 | 8.0 | 1.4 | 3.02 | 1.5 | 1.4 | 0.9 |

The reduction in leakage current can be primarily attributed to the improved quality of the dielectric layer in device B. This enhanced dielectric quality enables better electric field withstand capability, resulting in lower leakage current levels even under high electric fields. A high areal capacitance of 660 nF/cm$^2$ was observed. Furthermore, the ultrathin $Al_2O_3$ film exhibits weak frequency and voltage dependence in capacitance as shown in Figures 4 (c) and (d). This indicates the formation of denser M-O bonds and lower trap density, such as hydroxyl groups, within the film [19].

Tab. 2 summarizes the characteristics of various dielectrics using different methods, where $d$ represents the thickness of the gate dielectric, $C_i$ denotes the areal capacitance in the low-frequency region, and $J_{leak}$ represents the leakage current density at 1 MV/cm. Theoretically, for a specific TFT structure, an ideal gate dielectric material would possess an infinite dielectric breakdown field and near-zero leakage current density, resulting in a high field-effect mobility [22].

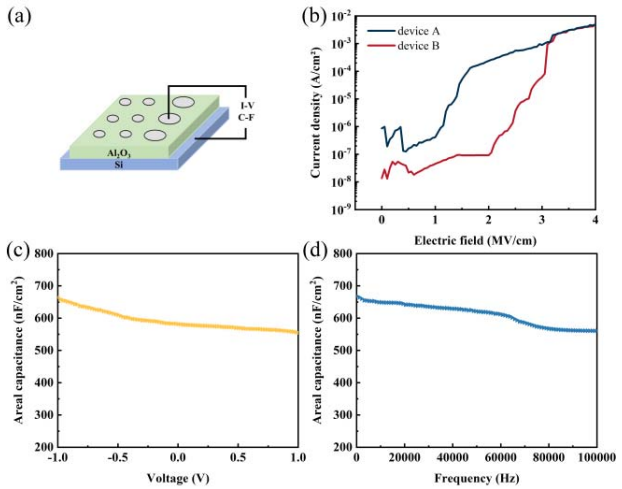


**FIGURE 4.** (a) Schematic of the capacitor. (b) Leakage current density characteristics of $Al_2O_3$. (c) Capacitance-frequency and (d) capacitance-voltage curves of p-Si/$Al_2O_3$/Al capacitor.

**TABLE 2.** Summary of dielectric properties for the inorganic dielectric.

| Material | Method | *d* (nm) | *Temp.* (°C) | $C_i$ (nF/cm) | $J_{leak}$ (A/cm²) | *Ref.* |
|---|---|---|---|---|---|---|
| $Al_2O_3$ | ALD | 43 | 33 | 201 | $10^{-7}$ | [15] |
| $Al_2O_3$ | PVD | 54 | RT | 117 | - | [13] |
| $Al_2O_3$ | PLD | 80 | RT | 59.8 | $10^{-8}$ | [20] |
| $Al_2O_3$ | PEALD | 140 | 150 | 57 | $10^{-9}$ | [21] |
| **$Al_2O_3$** | **ALD** | **5** | **250** | **660** | **$10^{-8}$** | **This work** |

In this regard, the ultrathin $Al_2O_3$ film used as the gate dielectric in electronic devices fabricated through ALD technology can be considered an excellent choice as it exhibits these desirable characteristics.

To verify the application of ultrathin $Al_2O_3$ in devices, we fabricated IGZO TFTs with a 5-nm $Al_2O_3$ gate dielectric. Figures 5 (a) and (b) illustrate the transfer characteristics of $I_D$ and $V_G$ for a fixed $V_D$ of 2 V, as well as the $I_D^{1/2}$–$V_G$ curves of device A and device B. The $I_{on}/I_{off}$ of devices A and B are approximately $10^5$ and $10^6$, respectively. Both devices exhibited a low operating voltage of 3 V. The high $I_{on}/I_{off}$ at low operating voltages is primarily attributed to the lower leakage current. Under the same operating voltage, the smaller leakage current leads to a higher $I_{on}/I_{off}$ [23].

The key electrical parameters of the TFTs are summarized in Tab. 3. The $\mu$ of devices A and B are 2.4 $cm^2$/Vs and 6.5 $cm^2$/Vs, respectively. The *SS* of device B is only 70 mV/decade, which is lower than that of device A (74 mV/decade). This should be ascribed to the much enlarged gate capacitance of the TFTs with the low interface defect of device B. Device B has a $V_{th}$ of 0.2 V, which is significantly lower than device A. The presence of a high-quality dielectric layer positively influences the threshold voltage of the transistor. This impact arises from the facilitation of electron channel formation, reduction in charge injection and drift, and mitigation of the influence of surface states. Collectively, these factors contribute to a notable reduction in the threshold voltage [26].

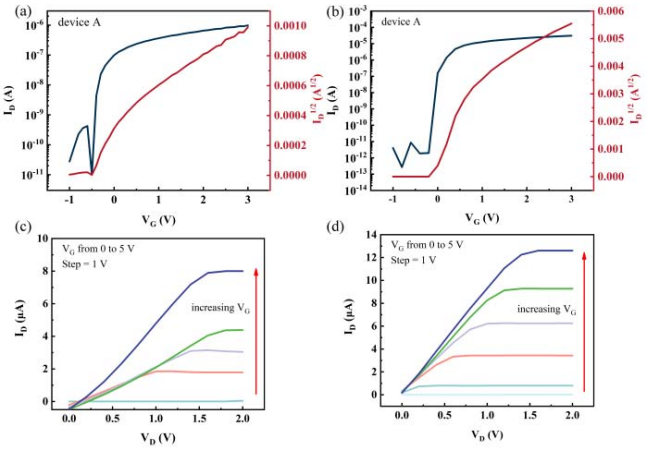


**FIGURE 5.** The corresponding transfer characteristic $I_D$ versus $V_G$ at a fixed $V_D$ of 2 V and the $I_D^{1/2}$ - $V_G$ curves of (a) device A and (b) device B. Output characteristics of (c) device A and (d) device B.

**TABLE 3.** Electrical performance of TFTs with various thicknesses of dielectric (C: Channel; D: dielectric; Vop: operation voltage).

| *C* | *D* | $V_{th}$ (V) | $\mu$ ($cm^2$/Vs) | $I_{on}/I_{off}$ | *SS* (V/dec.) | $V_{op}$ (V) | *Ref* |
|---|---|---|---|---|---|---|---|
| ZnO | $Al_2O_3$ (100 nm) | -0.5 | 27 | $10^6$ | 0.12 | 2 | [13] |
| IGZO | $Al_2O_3$ (5 nm) | 0.2 | 3.8 | $10^6$ | 0.1 | 0.6 | [18] |
| ZTO | $Al_2O_3$ (200 nm) | 0.5 | 11 | $10^7$ | 0.38 | 10 | [24] |
| IGZO | $Al_2O_3$ (100 nm) | 0.4 | 8 | $10^7$ | 0.1 | 5 | [25] |
| **IGZO** | **$Al_2O_3$ (5 nm)** | **0.2** | **6.5** | **$10^6$** | **0.07** | **3** | **This work** |

These satisfactory parameters indicate a low density of trapping states ($N_{trap}$) at the gate dielectric interface, which can be obtained using the following equation:

$$SS = \frac{k_B T \ln 10}{q}\left[1 + \frac{q^2}{C_{ox}} N_{trap}\right] \quad (3)$$

here, $k_B$ is Boltzmann's constant, $T$ is the temperature in Kelvin, and $q$ is the electron charge. The $N_{trap}$ is $4.5\times10^{12}$ $eV^{-1}$ $cm^{-2}$ for device A, and the $N_{trap}$ of device B is $2.8\times10^{12}$ $eV^{-1}$ $cm^{-2}$, which is among the lowest values in reported $Al_2O_3$ TFTs to date [18]. A reduced RMS surface roughness of $Al_2O_3$ corresponds to a lower number of charge traps being created at the IGZO/$Al_2O_3$ interface, resulting in superior performance in terms of suppressing charge capture at the channel/dielectric interface.

The output curves of device A and device B (drain-source current versus drain voltage, $I_D$-$V_D$) are shown in Figure 5 (c) and (d), respectively. Device B achieves a stable output current of up to 12.5 $\mu$A and exhibits well-defined cut-off behavior. in a distinct contrast to device A. There is no current jamming at the output characteristics of the device, indicating good ohmic contact between the channel layer and the source-drain metal.

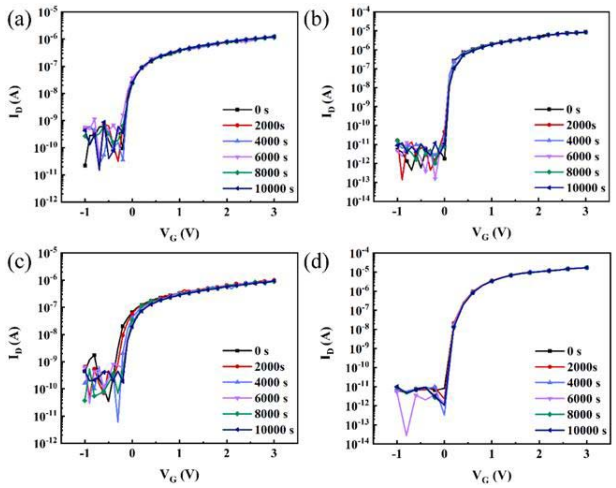


**FIGURE 6. Positive bias stress of (a) device A and (b) device B. Negative bias stress of (c) devices A and (d) device B.**

Figure 6 shows the stress time and gate voltage of device A and device B. The positive bias of 3 V was applied for 10000 s at room temperature in the atmosphere shown in Figures 6(a) and (b), all transfer curves show positive displacement under positive gate voltage stress and without subthreshold slope degradation, which is attributed to electron trapping in the interface layer or bulk dielectric layer without creating additional interface traps [18]. What's more, the negative bias of −3 V was applied for 10000 s at room temperature in the atmosphere are shown in Figures 6(c) and (d). After 10000 s of PBS and NBS testing, Device A exhibited $V_{th}$ shifts ($\Delta V_{th}$) of 0.56 V and 0.227 V, respectively, whereas Device B demonstrated $\Delta V_{th}$ of 0.038 V and 0.027 V, respectively. In semiconductor materials, particularly at the interface between the semiconductor and the insulating layer, charge trapping phenomena may occur. These traps, upon capturing or releasing charge carriers, can induce variations in the threshold voltage. This effect becomes especially pronounced under conditions of prolonged voltage application. Therefore, Device B exhibits fewer interface defects than Device A, indicating that novel fabrication process effectively mitigates interface imperfections.

## IV. CONCLUSION

In this study, a novel growth conception of $Al_2O_3$ thin films deposited by TMA/TMA/$H_2O$/$H_2O$ cycles via the ALD has been developed. The ultrathin $Al_2O_3$ gate dielectric deposited by 'double cycles' exhibited a low leakage current density of $10^{-8}$ A/cm$^2$ at 2 MV/cm and a high capacitance of 660 nF/cm$^2$. The IGZO TFTs operated at a minimum voltage of 3 V, with a higher $I_{on}/I_{off}$ of $10^6$, a large $\mu$ of 6.5 cm$^2$/Vs, and an *SS* approaching the theoretical limit of 70 mV/decade. The IGZO TFTs with a 5-nm $Al_2O_3$ prepared through 'double cycles' hold great promise for future low-power devices.

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