Optimization of Leaky Integrate-and-Fire Neuron Circuits Based on Nanoporous Graphene Memristors

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ABSTRACT Artificial neurons form the core of neuromorphic computing which is emerging as an alternative for the von Neumann computing architecture. However, existing neuron architectures still lack in area efficiency, especially considering the huge size of modern neural networks requiring millions of neurons. Here, we report on a compact leaky integrate and fire (LIF) neuron circuit based on graphene memristor device. The LIF circuit exhibits various biological properties like threshold control, leaky integration and reset behavior. Circuit parameters like the synaptic resistance and membrane capacitance act as additional control parameters whereby the spike frequency of the circuit can be effectively controlled. Uniquely, the circuit exhibits biologically realistic frequencies as low as 286 Hz. The results suggest the suitability of this compact and biorealistic LIF neuron circuit towards future bioinspired computing systems

INDEX TERMS Leaky integrate and fire, graphene, memristor, artificial neuron, SPICE, neuromorphic computing.

I. INTRODUCTION

Computationally intensive applications like big data analytics, machine learning and deep learning are receiving increasing attention both from academia and industry due to their enormous success in solving real world problems like image recognition [1], autonomous driving [2], text processing [3], protein structure prediction [4], drug discovery [5] etc. Large language models (LLMs) like the GPT-4 [6] and Llama 2 [7] have made tremendous strides in natural language processing, resulting in human like textual replies, text classification and semantic similarity assessment. Further research in generative artificial intelligence (AI) models are expected to open the path towards fully unsupervised and human-like general intelligence. However, these existing models are trained on vast amounts of data

using conventional CMOS based computing systems. Such systems often rely on huge clusters of graphical processing units for their training procedure, which consume hundreds of megawatts of power and require extended training periods. As future demand for raw computing power increases, existing CMOS based von Neumann computing architecture may not be able to scale adequately. This is because of the speed discrepancy between the memory and the processing units which is commonly referred to as the von Neumann bottleneck [8]. A suitable emerging alternative is the field of neuromorphic computing which is inspired by the functioning of the human brain [9].

The human brain is composed of a dense network of interconnected processing elements called neurons and storage nodes referred to as synapses. This network of
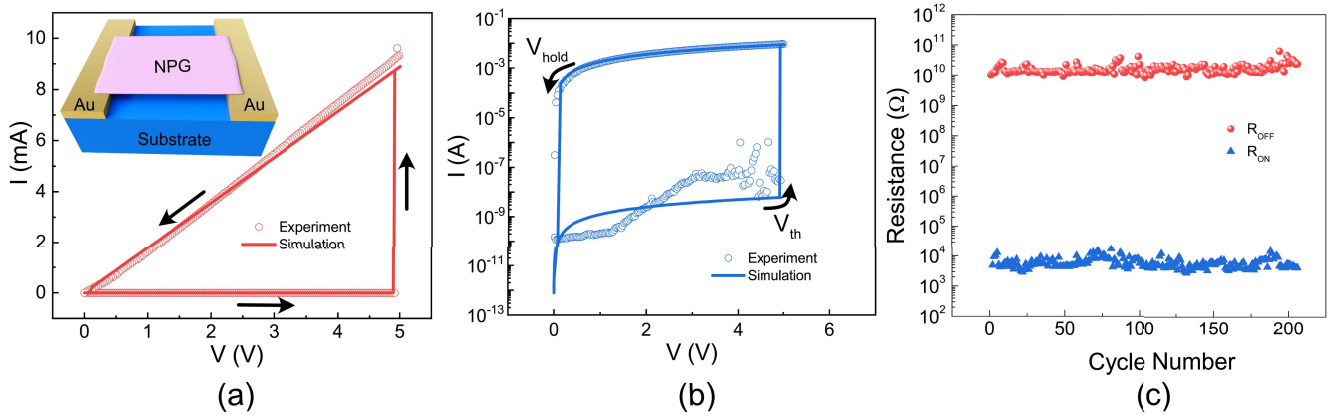
FIGURE 1. (a) Experimental data and SPICE simulation fit of the linear I-V plot for the NPG device. Inset shows the schematic of the device. (b) Experimental semilog *I-V* curve of the NPG device with the SPICE simulation fit. (c) Endurance characteristics on the NPG device showing stable ON and OFF states for 200 switching cycles. Adapted from supplementary data of [22].

approximately 10^{11} neurons and 10^{15} synapses exhibit high parallelism and extremely low energy operation (∼20 fJ per spike event) [10]. The biological neuron consists of the soma which processes the input information received from other neurons through the dendrites and generates spike potential to be transmitted to the output neuron through the axons. Since the process take place through asynchronous and sparse data transmission, the low energy expenditure is a major advantage. In addition to the innovations in hardware, an increasing attention has also been devoted to the development of bio-mimetic learning rules [11]. Spiking neural networks (SNN) have been developed in recent years as the third generation of artificial neural networks (ANNs) [12] which attempts to replace the floating point arithmetical abstractions of ANNs with spike based neuron architectures which are highly energy efficient and biologically plausible [13].

However, the realisation of efficient SNN models in hardware require compact and energy efficient circuits which can be scaled towards large scale applications. Several CMOS based neuron circuits have been reported in recent years wherein a single neuron circuit has been implemented using multiple transistors and capacitors with additional bias lines [14], [15], [16], [17]. These CMOS based designs suffer from lack of area efficiency and requires additional overhead circuitry. Memristors have recently emerged as a new category of devices which operate on the basis of internal resistance change due to the redistribution of filamentary metal ions or oxygen vacancies [18]. They are suitable alternatives as neuron circuit elements because of their low footprint, easy fabrication, scalability and fast switching speeds. Several reports have already been reported based on memristor based neuron circuits [19], [20]. However, they suffer from issues like the lack of biological frequency reproduction [16], high rest current [21] and lack of low frequency tunability [17].

In this work, we report an artificial Leaky-Integrate-and-Fire (LIF) neuron circuit and its spike frequency optimization

based on an experimentally fabricated nanoporous graphene (NPG) memristor device. A SPICE model for the NPG memristor device is developed and verified based on the experimental device characteristics. The simulated device characteristics are used to develop a compact LIF neuron circuit which exhibits leaky integration, threshold spiking and reset behavior with tunable spike response. The results demonstrate the feasibility of NPG neurons as compact neural processing units in neuromorphic computing systems. The main highlights of this paper are:

1) A scalable NPG device with a high ON/OFF ratio has been fabricated.
2) A simple SPICE model has been proposed for emulating the switching characteristics of the device.
3) A highly compact circuit architecture has been proposed for realizing the LIF behavior.
4) Spiking behavior of the LIF circuit could be tuned using a range of circuit and device specific parameters.
5) Biological spike frequency has been demonstrated which adds to the bioplausibility and energy efficiency of the system.

II. RESULTS AND DISCUSSION
A. DEVICE DESCRIPTION
The NPG graphene-based device was fabricated from sugar cane bagasse (Saccharum officinarum) using a dry transfer technique. The details of the fabrication procedure has been reported in our previous publication [22]. The NPG device has a lateral structure with Au/NPG/Au configuration deposited over an insulating substrate with a channel length of 100 μm. Inset of Fig. 1(a) shows the schematic of the NPG device. The measured electrical characteristics of the device are shown in linear scale in Fig. 1(a) and semilog I–V characteristics of the device are shown in Fig. 1(b). The threshold switching behavior of the device is clear from both the figures where the device switches from a high resistance state (HRS) to a low resistance

```
BEGIN
   SET Vt = [VCS Threshold voltage]
   SET Vh = [VCS Hysteresis voltage]
   SET RON = [VCS ON resistance]
   SET ROFF = [VCS OFF resistance]
   SET State = [VCS Initial state (OFF)]

   //define time dependent voltage sequence
   DEFINE InputVoltageSequence()

   FOR time step in total time steps DO
      //update input voltage
      CALL InputVoltageSequence()

      //check condition for VCS state
      IF state = OFF THEN
         SET Resistance = ROFF
         IF Vin > (Vt + Vh)THEN
            SET State = ON
            SET Resistance = RON
         ENDIF

      ELSE
         SET Resistance = RON
         IF Vin < (Vt - Vh)THEN
            SET State = OFF
            SET Resistance = ROFF
         ENDIF
      ENDIF

      // calculate current through VCS
      CALCULATE Current

      // update circuit parameters based on VCS state
      // modify nodal voltages, branch currents, etc.,
   ENDFOR

END
```

FIGURE 2. Pseudocode for the implementation of the VCS SPICE Model.

state (LRS) at a threshold voltage (V_{th}) of 4.9 V and a reverse switching from LRS to HRS at a hold voltage (V_{hold}) of 0.1 V. Such a volatile switching behavior can be attributed to the oxygen ion accumulation at the interface between the anode and NPG channel [22]. Interestingly, the V_{hold} is very close to 0 V and hence the LRS region spans a wider voltage range ($\sim$4.8 V) which is an added advantage of the NPG device and not seen in previous reports based on 2D material based memristors [20]. Fig. 1(c) shows the endurance characteristics of the NPG device for 200 switching cycles. These data support stable switching characteristics that are essential for the practical realisation of a LIF neuron circuit.

B. SPICE MODEL & CIRCUIT DESCRIPTION

In order to reproduce the electrical characteristics of the NPG device, we used SPICE simulations based on the open source software Ngspice [23]. We propose a voltage-controlled switch (VCS) element as a behavioral SPICE

model for the NPG device. The VCS model alternates between resistance states based on the combined effect of the threshold voltage (V_t) and hysteresis voltage (V_h). Here, V_t and V_h are SPICE model specific parameters and are different from the NPG device threshold voltage (V_{th}). The VCS switches from the OFF state to the ON state when the input voltage exceeds ($V_t + V_h$). Similarly, if the VCS is in the ON state, it switches back to the OFF state when the input voltage falls below ($V_t - V_h$). Hence, the hysteresis voltage is an added advantage of the VCS model which enables it to switch between resistance states when the ON and OFF voltage are different values. Here, we have chosen the V_t (2.5 V) and V_h (2.45 V) values of the VCS SPICE model such that their sum and difference yields the NPG device switching voltages (V_{th}) in the forward (4.9 V for HRS to LRS switching) and reverse (0.1 V for LRS to HRS switching) directions. A tolerance value of 0.05 V is applied to V_h for better convergence of the SPICE model fitting to the experimental data in Fig. 1(b). The ON and OFF resistance values for the VCS SPICE model are chosen as 561.79 Ω and 809.7 MΩ respectively which are determined from the experimental NPG device switching data (Fig. 1(b)) corresponding to a read voltage of 2 V. We also provide a detailed pseudo code to explain the working of the VCS model in Fig. 2. As depicted in Fig. 1(a) and Fig. 1(b), the SPICE model exhibited good agreement with the experimental switching characteristics with a negligible fitting error. Such a simple switch model is a good substitute for complex Verilog based approximations which have been reported previously [24], [25], [26]. These complex Verilog based models require special compilers for their SPICE based implementation. For a threshold switching memristor device, the voltage-controlled switch model is more realistic and simpler estimation which can be universally implemented in any SPICE based simulator.

Further, we proceed to demonstrate an artificial LIF neuron based on the Au/NPG/Au device using SPICE simulations. Fig. 3(a) depicts the schematic of a biological LIF neuron. A biological neuron receives input spike signals from the preneurons through its dendrites. The soma of the neuron then integrates the signals continuously. As a result of this signal integration, the potential of the interior of the neuron, commonly referred to as the membrane potential, increases.

When the membrane potential exceeds the threshold value, an output spike is generated which is transmitted through the axon to the postsynaptic neurons. Once the spike signal is generated, the membrane potential resets to the original potential (rest potential). Electrically, such a biological LIF model can be realized with the NPG device using a simple circuit as shown in Fig. 3(b) [19].

The NPG device is connected in parallel to a capacitance (C_m) which together acts as the membrane capacitance. C_m can be the internal capacitance of the NPG device or an externally connected capacitor. The membrane capacitance is serially connected to a resistor (R_s) which acts as the synaptic resistance. A voltage source V_{in} provides the input voltage
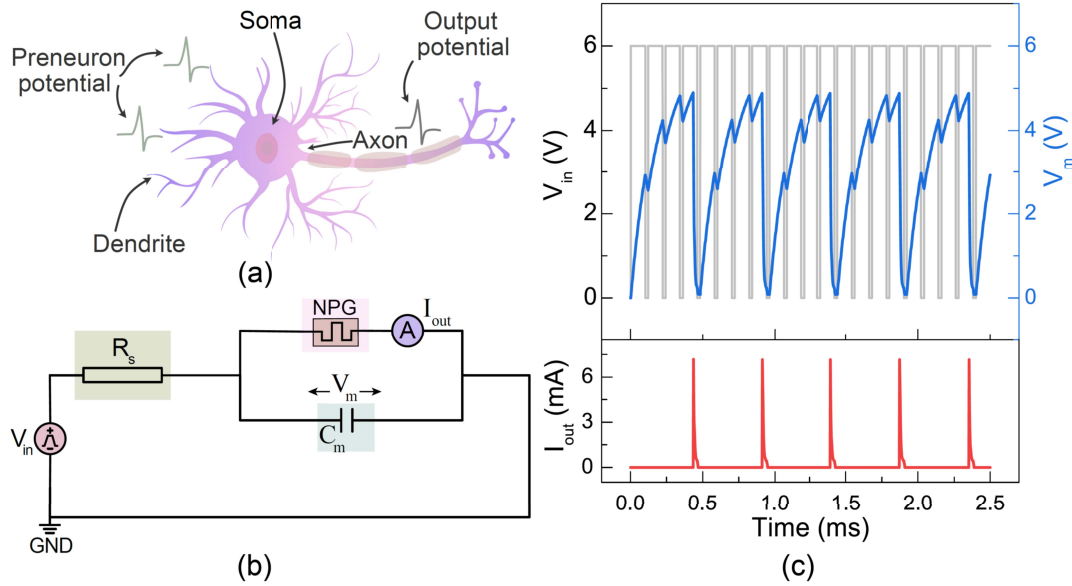
FIGURE 3. (a) Schematic of the biological neuron (b) LIF Neuron circuit based on the NPG device (c) Membrane voltage and corresponding Spike current (I_{out}) measured using current meter (R_s=15 kΩ, C_m=10 nF).

signal which is the electrical equivalent of the preneuron signal.

The mathematical description of the LIF neuron circuit can be expressed as follows:

$$\tau \frac{dV_m}{dt} = -\frac{R_s}{R_{NPG}}[V_m - V_{rest}] + V_{in} \qquad (1)$$

where τ is the time constant for charging the capacitor C_m, V_m is the membrane potential, R_{NPG} indicates the resistance of the NPG device and V_{rest} denotes the rest potential of the neuron membrane. Initially, the NPG device is in the HRS state. When repeated voltage pulses are applied at V_{in}, the current through the circuit charges the capacitor C_m such that V_m increases continuously. When V_m exceeds the threshold voltage (V_{th}) of the NPG device, the device switches to the LRS and the charge stored in C_m discharges through the NPG device. Such a discharge process generates a current spike or action potential at the output of the NPG device. As the C_m discharges, V_m falls below V_{hold} and hence the NPG device switches back to the HRS. Interestingly, the LIF neuron circuit achieves near zero rest voltage (V_{rest}) which is a characteristic feature of biological neurons.

Such a low V_{rest} is due to the V_{hold} of the NPG device being close to 0 V. Further, the reverse switching of the NPG device to the HRS state is accompanied by the capacitor C_m resuming its charging process. This continuous cycle of leaky integration, spike output and reset process is clearly demonstrated in Fig. 3(c) when the amplitude of V_{in} is 6 V and width is 100 μs. The values of R_s and C_m are 15 kΩ and 10 nF respectively. Here, we clearly observe the leaky integration behavior of the LIF circuit which has been missing in previous reports based on compact circuits [20]. We also observe a sharp spike response when V_m exceeds V_{th}. Such a sharp spike response with complete reset to the rest

potential (V_{rest}) has been rarely seen in previous memristor based LIF circuits [10], [19]. The fully reset response can be attributed to the low OFF current and large ON/OFF ratio of the NPG device leading to distinct spike and rest states. The total energy consumed per spike was calculated by integrating the power consumption over the time duration and averaging over the number of spikes. We obtained a relatively high energy per spike value of 408.42 nJ/spike for the LIF circuit in Fig. 1(b). This is relatively high as compared to the state of the art energy per spike reported for LIF circuits which is of the order of ∼pJ [27] reported for a 65 nm technology node circuit. However, we believe that the energy consumption can be further reduced by NPG channel length scaling and circuit capacitance scaling.

C. SPIKE FREQUENCY OPTIMIZATION
C.1. EFFECT OF R_S

The modulation of the spike characteristics of the LIF neuron using the R_s as a control parameter at a fixed C_m (10 nF) has been depicted in Fig. 4. In our LIF neuron circuit, R_s acts as a synaptic weight which modulates the strength of neuronal connection between the preneuron and postneuron. As the value of R_s increases, the time constant for the charging of C_m increases which results in longer integration times as can be seen in Fig. 4(a). This results in a longer time scale for membrane potential integration and thereby resulting in less number of output current spikes (see Fig. 4(b)).

Biologically, this is equivalent to a weak synaptic connection between two adjacent neurons leading to an attenuation in signal transmission. Similarly, for low R_s values, we observe a faster membrane integration due to the reduced time constant. This results in high spike rates leading to single step spiking as R_s approaches 5 kΩ. Fig. 4(c) shows
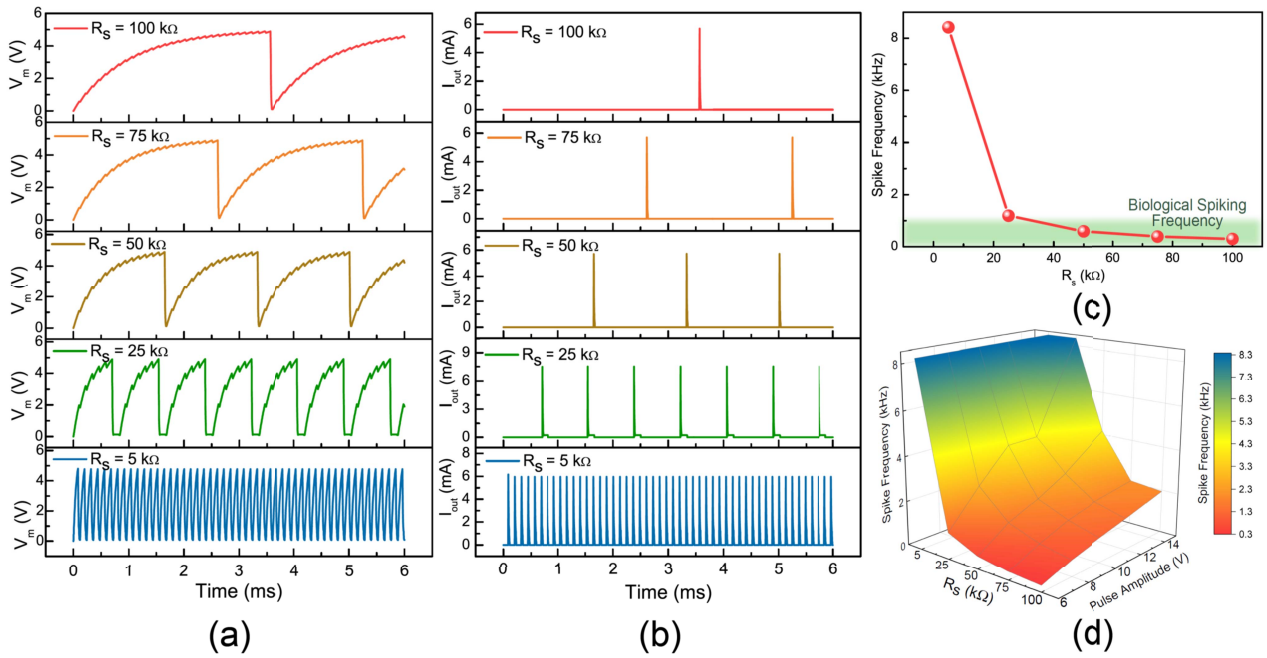
FIGURE 4. (a) Membrane potential of the LIF circuit for various R_s values (C_m=10 nF) and their corresponding (b) Spike currents. (c) Spike frequency as a function of the R_s value (d) 3D plot of Spike frequency as a function of the pulse amplitude and R_s.

the spike frequency variation with respect to the R_s values. The spike frequency of the LIF neuron circuit is found to vary from 8.42 kHz to 286.38 Hz as the R_s value varies from 5 kΩ to 100 kΩ respectively. It is interesting to note that the lower bound of the spike frequency (286 Hz) obtained by R_s variation is converging in the biological spike frequency region [21]. This is shown by the green highlighted region in Fig. 4(c). Such a biological spike frequency reproduction is highly significant for biorealistic neuron realization. In addition, low frequency spiking is also advantageous in terms of the overall energy efficiency of the circuit. Further, it is to be noted that the pulse amplitude of the input voltage V_{in} can also act as an additional control parameter for every single value of R_s chosen for spike frequency optimization in Fig. 4(c). Hence, a 3D ribbon plot of the spike frequency as a function of the R_s and pulse amplitude is constructed in Fig. 4(d). As the pulse amplitude increases, an increase in the rate of charge accumulation is expected in the capacitor C_m, which leads to increased spike frequency. A similar response is observed in Fig. 4(d) where the spike frequency increases linearly at lower pulse amplitudes and higher R_s values whereas saturates to higher frequencies at higher pulse amplitudes and lower R_s values. The figure clearly shows that a continuous range of frequency optimization is conceivable with appropriate choice of R_s and pulse amplitude values. Such a wide range of tunability of the spiking response can be beneficial for designing neuromorphic systems for custom biomimetic applications.

C.2. EFFECT OF C_M

In order to further investigate the role of the charging capacitor C_m in optimizing the spike frequency response, the membrane potential V_m (see Fig. 5(a)) and spike current I_{out} (see Fig. 5(b)) are plotted for C_m values –2 nF, 6 nF, 10 nF, 12 nF and 20 nF. Unlike in the case of R_s, the values of C_m are closely spaced but still provide adequate tunability to adapt to spike frequencies ranging from 8.345 kHz to 925.92 Hz for C_m values of 2 nF and 20 nF respectively. The biological frequency range can also be seen from Fig. 5(c) whereas the 3D ribbon plot of spike frequency dependence on C_m and pulse amplitude are shown in Fig. 5(d). From the 3D ribbon plot, we note that the C_m offers limited scope for tunability which is seen by the sharp rise in spike frequency as the capacitance and pulse amplitudes varies. Consequently, the spike frequency quickly saturates to the maximum value of 8.345 kHz for lower C_m values and higher pulse amplitudes.

In addition, we have attempted to further scale down the capacitance values to picofarad (pF) values, for better CMOS integration and compact footprint. Hence, we have studied the LIF response of the NPG based circuit for C_m = 200 pF, 100 pF, 50 pF & 25 pF as shown in Fig. 6. A pulse amplitude of 6 V, pulse width of 10 μs, pulse period of 12 μs and R_s of 100 kΩ was used for these simulations. From, the LIF membrane voltage and spike response in Fig. 6, we can confirm that the LIF circuit can be optimised further to function efficiently with smaller C_m values. Further, we have also calculated the energy per spike for the LIF circuit with C_m = 25 pF. We obtained a low energy consumption of 737.10 pJ/spike for this circuit which is more energy efficient than similar memristor based LIF circuits which are in the order of nJ [21]. Hence, we believe that the NPG based LIF circuit holds huge promise in further capacitance scaling and thereby energy efficiency.
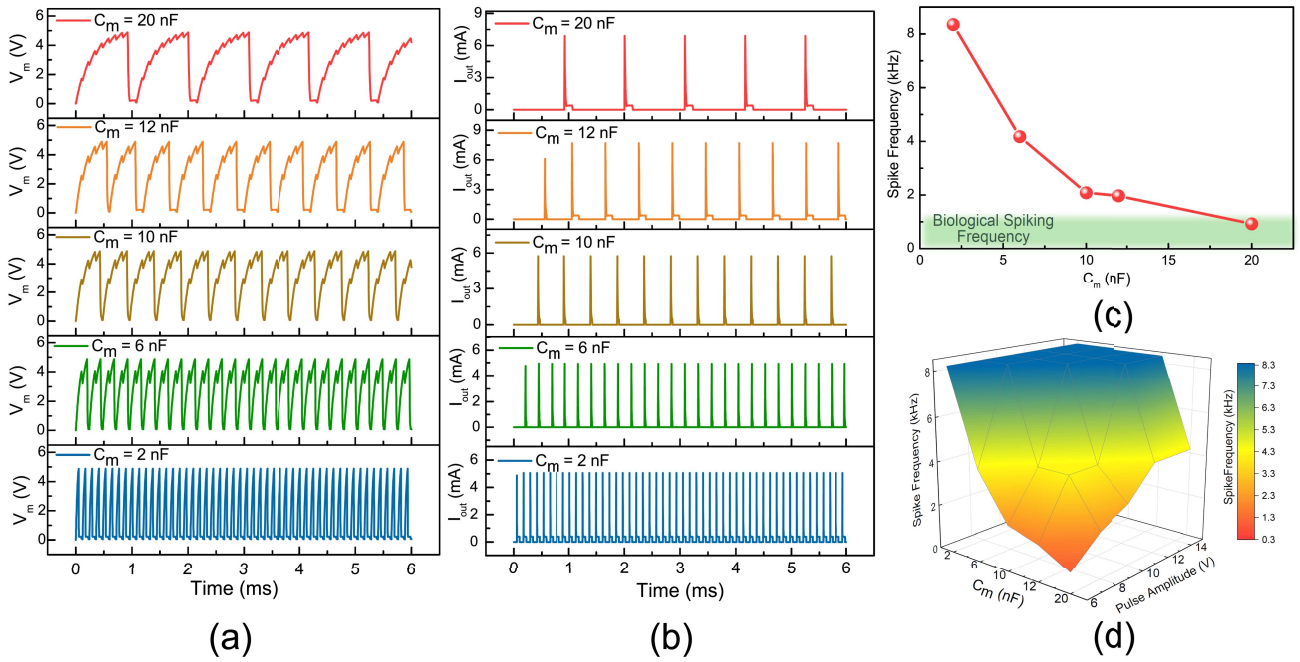
FIGURE 5. (a) Membrane potential of the LIF circuit for various C_m values (R_S=15 kΩ) and their corresponding (b) Spike currents. (c) Spike frequency as a function of the C_m value (d) 3D plot of the Spike frequency as a function of the pulse amplitude and C_m.
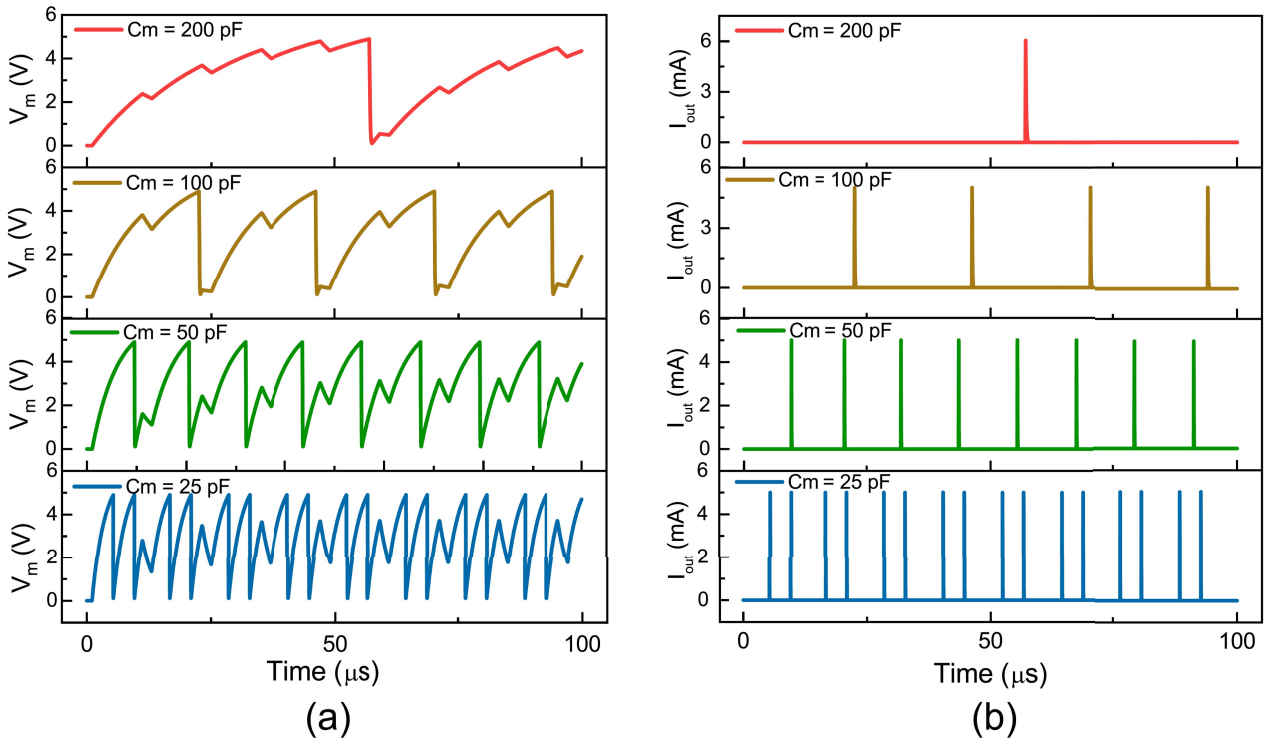

FIGURE 6. (a) Membrane potential (V_m) & corresponding (b) Spike currents of the LIF circuit for low C_m values. Pulse amplitude = 6 V, pulse width = 10 μs, pulse period = 12 μs and R_S = 100 kΩ was used for the simulations.

C.3. EFFECT OF L

Further, the channel length (L) of the device has been scaled to explore the effect of channel length variation on the spike response of the LIF neuron circuit. Fig. 7 shows the variation of V_m and I_{out} for the channel lengths 100 μm, 80 μm and 60 μm respectively. Although the variation of V_m and I_{out} does not follow a linear trend with channel length scaling, it can be observed that at lower channel length
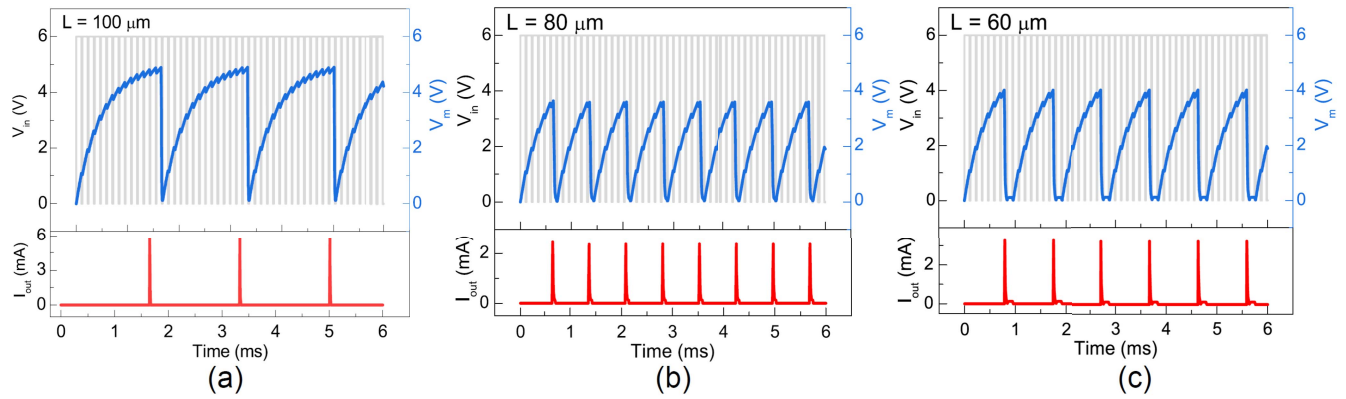
FIGURE 7. Input Voltage, Membrane potential and corresponding Spike current of the LIF neuron circuit for NPG channel lengths: (a) 100 μm (b) 80 μm and (c) 60 μm.

TABLE 1. Comparison of the present work with other reported LIF circuits.

Reference	Neuron Model	Device type	Physical Mechanism	Frequency	Number of components	Additional supply lines
[15]	Integrate & Fire	MOSFET	Field effect	100 Hz	22 transistors, 1 capacitor	7
[16]	Integrate & Fire	FBFET	Positive feedback	200kHz	9 transistors, 1 resistor, 1 capacitor	3
[17]	Integrate & Fire	p-n-p-n diode	Avalanche breakdown	8.1kHz−24kHz	3 transistors, 1 diode, 1 capacitor	0
[28]	Leaky Integrate & Fire	SCR	Voltage threshold	Variable	1 SCR, 3 transistors, 2 diodes, 1 capacitor &7 resistors	2
[29]	Integrate & Fire	MoS$_2$/ Graphene memristor	Threshold switching	-	1 memristor, 1 capacitor, 3 resistors	0
[30]	Leaky Integrate & Fire	Four terminal graphene nano-ribbon device	Interfacial charge trapping/detrapping	-	6 graphene nanoribbon devices	3
This Work	Leaky Integrate & Fire	Memristor	Threshold switching	286.38 Hz−8.42kHz	1 memristor, 1 capacitor, 1 resistor	0

values, the spike frequency increases in general. This might be due to the lower V_{th} value observed for lower channel length devices. This is in agreement with our previously reported results on NPG device [22], where we observed that the value of V_{th} for 80 μm and 60 μm devices are lower in comparison to the 100 μm channel length device. As discussed before, the threshold switching in NPG devices arises due to the accumulation of interfacial oxygen ions. As channel length decreases, the amount of oxygen ions at the interfaces decreases and hence the barrier at the interfaces decreases leading to a lower V_{th} value. Here, L acts as an additional device dependent control parameter for tuning the spike response of the LIF circuit. Overall, we demonstrate fully optimizable spike response of the LIF circuit using both circuit dependent and device dependent control parameters.

D. COMPARISON WITH PREVIOUS REPORTS
Finally, we present a comparison (see Table 1) of the salient features of the NPG device based LIF circuit in comparison with other recently published reports. From Table 1, it can be

seen that the CMOS MOSFET [15] based and FBFET [16] based neuron circuits require large number of transistors, capacitors and additional bias lines leading to lower power & area efficiency of the circuits. The p-n-p-n diode [17] based circuit has the advantage of zero additional bias lines and frequency tunability but is limited by the frequency range and lack of leaky integration response in the neuron circuit. The SCR device [28] based circuit demonstrates leaky integrate and fire response but requires more number of components and additional bias lines. Several recent memristor based circuits have also been reported with similar compact circuits [19], [20]. However, these circuits either lack the demonstration of leaky integration response or complete reset to near zero V_{rest} after spike generation. In addition, the LIF circuit reported in the present work can reproduce a range of spike frequencies from the biological range (286.38 Hz) to the high frequency range (8.42 kHz) whereas the previous reports have a much more limited frequency range. In addition, the present circuit has clearly demonstrated the leaky integration and reset part of the LIF neuron circuit with minimal number of circuit elements over a wide frequency range.

III. CONCLUSION

In summary, we developed a compact LIF neuron circuit based on experimentally fabricated NPG device. The fabricated NPG device exhibited excellent ON/OFF ratio ($\sim 10^6$) and low V_{hold}. A simple SPICE model was proposed to emulate the electrical characteristics of the NPG device. Based on the novel SPICE model, a low footprint LIF neuron circuit was simulated which demonstrated leaky integrate and reset behavior with near zero V_{rest}. Spiking behavior of the LIF circuit could be tuned using a range of circuit and device parameters yielding a wide frequency range from biological frequency range to the kHz range. Our LIF neuron circuit also successfully demonstrated the synaptic strength modulation. The demonstration of a compact and fully tunable LIF neuron circuit based on a scalable NPG device paves the way for its applicability in emerging and future bioinspired computing applications. Our future work will be focused on monolithically integrating R_s and C_m into the proposed neuron circuit, which will require additional investigation into materials, device structures, and fabrication methods.

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