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Series Capacitance Gate Driver to Suppress Voltage Oscillation of SiC MOSFET

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ABSTRACT The severe voltage oscillation of SiC MOSFET in switching transient affects the safety of devices and EMI. In this article, a series capacitance gate driver (SCGD) is proposed to solve this problem. The series capacitance is charged or discharged in switching transient so that the equivalent driving resistance is gradually increased compared with that of conventional gate driver (CGD), and the voltage oscillation is suppressed. Under the same voltage oscillation level, the average equivalent driving resistance of SCGD is smaller than that of CGD through reasonable parameters design. This means that the optimization of both voltage oscillation and switching loss is realized. Although active gate driver (AGD) has good performance in this respect, the effect may be affected by the delay and control accuracy due to very short switching transient time of SiC MOSFET. Compared with AGD, the proposed SCGD only adds passive components without any control and has a simple structure. The experimental results verify the effectiveness of SCGD.

INDEX TERMS SiC MOSFET gate driver, series capacitance, voltage oscillation, safety and EMI, switching loss.

I. INTRODUCTION

The traditional MOSFET uses Si as the primary material, with mature technology and wide application. However, Si MOSFET is challenging to meet the technical requirements of high voltage, high temperature, and high power density in switching power supply [1], [2]. Compared with the traditional Si MOSFET, SiC MOSFET has higher thermal conductivity so it can withstand a higher current density. A higher band gap width, about three times that of Si MOSFET, determines that the SiC MOSFET will have a higher voltage and operating temperature. SiC MOSFET has a faster switching speed and lower conductive resistance, which means that it has advantages in switching loss and conduction losses [3], [4], [5], making them more suitable for high switching frequency applications. Therefore, SiC MOSFET is very suitable for small power applications (tens of kW to hundreds of kW) with high switching frequency, such as modular photovoltaic inverters, chargers or motor drivers of electric vehicle [6], [7], etc., which is conducive to improving the efficiency, power density and reliability of the system.

Because of the faster switching speed of SiC MOSFET, the drain-source voltage oscillation and complementary transistor or diode voltage oscillation excited by parasitic inductance in switching transient are more serious [8]. The voltage oscillation will lead the device damage, such as the drain-source overvoltage breakdown, gate-source overvoltage breakdown caused by the Miller effect [9] (The gate-source voltage safety threshold of SiC MOSFET is small [10]), false opening caused by bridge arm crosstalk [11], etc. Additionally, the oscillation of drain-source voltage and diode voltage will aggravate the electromagnetic interference (EMI) of the system and put forward higher requirements for electromagnetic compatibility (EMC) design [12]. Therefore, it is necessary to suppress the voltage oscillation of SiC MOSFET.

According to the mechanism of voltage oscillation, reducing the stray inductance of the primary circuit [13] is the fundamental solution, but in practical application, it is difficult to eliminate the stray inductance. Currently, improving the gate driver to suppress voltage oscillation is the leading research direction. The traditional method mainly suppresses voltage oscillation by adding passive components, such as increasing the driving resistance of conventional gate driver (CGD) [14], paralleling the RC snubber [15], and adding a Zener diode to absorb overvoltage [16], etc. Adding a Zener diode has a limited effect on suppressing oscillation; increasing the driving resistance or paralleling the RC snubber can effectively suppress the voltage oscillation but will reduce the switching speed and increase the switching loss. Although the SiC MOSFET has excellent advantages in switching speed, its switching loss is still significant in hundreds of kHz hard switching occasions, which is not conducive to improving system power density [17], [18].

Active gate driver (AGD) has recently been developed to optimize both voltage oscillation and switching loss. By adding active devices such as MOSFETs or operational amplifiers based on CGD, AGD can increase the driving current to reduce the switching loss in the stage that does not cause voltage oscillation and reduce the driving current to suppress voltage oscillation in the stage that causes voltage oscillation [19]. In [20], an two-stage driving resistance AGD is proposed. The auxiliary switches are connected in parallel with the driving resistance to control the driving current at different switching stages. The AGD can realize multi-level driving voltage and resistance with the help of CPLD, reducing the driving current in the switching stage when the voltage oscillation needs to be suppressed and increasing the driving current in other stages to reduce the switching loss [21], [22]. In [23], an intelligent AGD is proposed. It sets different control targets according to the converter state and achieves multi-objective optimization by adjusting the driving voltage, current, and resistance, such as voltage oscillation suppression, switching loss reduction, temperature control, etc. Although the above AGDs have good performance, the circuit structure is relatively complex with many control signals, and the cost is also high. Additionally, the sampling circuit is also required for the drain current, gate-source, or drain-source voltage, making it difficult to guarantee the reliability of AGD in high switching frequency.

Considering the requirements for the reliability of the gate driver in high switching frequency occasions and the simplicity of the circuit structure, AGD based on current source were proposed in [24]. The driving speed was controlled by timer, which eliminates the sampling circuit and improves the reliability to a certain extent. However, its performance strongly depends on the accuracy of the control timing. In [25], a charging pump gate driver (CPGD) is proposed. This method effectively increases the average driving current in the turn-on transient and can optimize the switching loss and voltage oscillation. Compared with other methods, its advantages are mainly reflected in the simple circuit structure, no additional control, etc. However, the parameters design pays more attention to reducing switching loss, which worsens the voltage oscillation and easily causes large gate-source voltage oscillation resulting in the gate-source breakdown of the SiC MOSFET. Additionally, CPGD does not consider the optimization of turn-off transient. In [26], a partial-bootstrap gate driver (PBGD) is proposed. PBGD adds some extra devices based on CPGD to realize the optimization of both turn-on and turn-off loss. However, the circuit structure is relatively complex, and the suppression of voltage oscillation has not been considered. Adding series capacitance on the basis of CGD has the same equivalent circuit as PBGD and the simpler structure. But the existing series capacitance methods do not consider the application in voltage oscillation suppression.

This article proposes a series capacitance gate driver (SCGD). It only adds some passive components, such as capacitance, resistance, diode, and Zener diode on the basis of CGD, which is simpler and more reliable than AGD. SCGD has the ability to suppress both turn-on and turn-off voltage oscillation through the appropriate parameters design. It realizes this function by the charge and discharge of series capacitance in switching transient. Due to the gradual change of equivalent driving resistance caused by series capacitance charging and discharging, SCGD also realize the optimization of switching loss, that is the switching loss is lower than that of CGD at the same oscillation amplitude level.

Overall, to suppress voltage oscillations, it is necessary to increase the driving resistance of CGD, which significantly increases losses. The proposed SCGD utilizes the charge and discharge of series capacitance to increase the average driving current while having the same voltage oscillation as CGD, which will optimize the switching loss. Compared with SCGD, AGD has stronger adaptability in optimization effect at different voltage and current level. But, due to the delay in its feedback part and the susceptibility of the signal to interference, its reliability is reduced at high switching speeds. In addition, the circuit structure of AGD is also relatively complex. PBGD is consistent with SCGD in principle, but SCGD has auxiliary branches that increase the degree of freedom in parameters design. It also requires fewer devices and has a simpler structure.

This article is organized as follows. In Section II, the modeling analysis of SiC MOSFET is given, and the voltage or current expression in different stages are obtained. Section III introduces the working principle and parameters design of the proposed SCGD; then analyzes the voltage oscillation suppression effect and switching loss. In Section IV, taking a SiC device as an example, the experimental verification of SCGD is carried out. Section V gives the conclusion of this article.

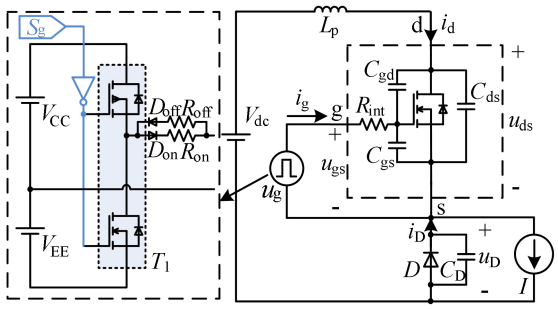


FIGURE 1. SiC MOSFET switching test circuit using CGD.

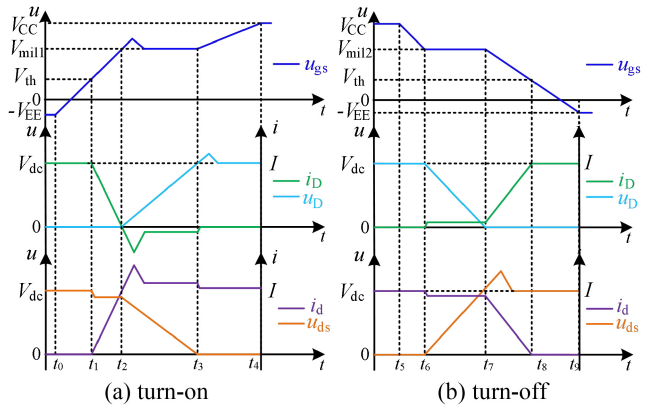


FIGURE 2. Typical transient waveforms using CGD.

II. BEHAVIOR MODEL OF SIC MOSFET

Fig. 1 shows the SiC MOSFET switching test circuit using CGD. d, g, and s are the drain, gate and source of the SiC MOSFET, respectively. C_{gs}, C_{gd} and C_{ds} are the parasitic capacitance of the gate-source, gate-drain, and drain-source. L_p is the stray inductance of the main circuit. R_{int} is the gate resistance inside the SiC MOSFET package. R_{on} and R_{off} are the additional gate resistance outside the package. S_g is the PWM signal, which is used to realize the high and low level output of totem pole T_1. V_{CC} is the high-level output voltage, and the low-level output voltage is V_{EE}. V_{dc} is the bus voltage, I is the load current, and the arrow signals its positive direction. When the SiC MOSFET is turned on, the current flows through the drain and source, and when it is turned off, the current flows through the freewheel diode D. C_D is the parasitic capacitance of D.

In order to obtain the voltage oscillation characteristics of SiC MOSFETs, the transient behavior model should be analyzed first. The typical waveforms are shown in Fig. 2.

Fig. 2 (a) is the typical turn-on transient waveform using CGD. According to the different driving current paths, this transient can be divided into three stages [27].

Stage 1 ($t \in [t_0, t_2]$): in this stage, V_{CC} charges C_{gs} through the driving resistance R_{on}, and u_{gs} starts to rise from $-V_{EE}$. When u_{gs} reaches the threshold voltage V_{th}, i_d starts to rise from 0 to load current I, as shown in Fig. 2 (a) $t_1 \sim t_2$. The related expression is written as (1).

$$\begin{cases} u_{gs} = (-V_{EE} - V_{CC})e^{-\frac{t-t_0}{(R_{on}+R_{int})C_{gs}}} + V_{CC} \\ i_d = g_{fs}\left(u_{gs} - V_{th}\right), \quad t_1 < t < t_2 \\ u_{ds} = V_{dc} - L_p\frac{di_d}{dt}, \quad t_1 < t < t_2 \end{cases} \tag{1}$$

Stage 2 ($t \in [t_2, t_3]$): at t_2, i_d rises to I and i_D drops to 0. Because of the reverse recovery characteristic, the diode will not be turned off immediately, and i_D will rise in the reverse direction. At the end of reverse recovery, i_d tends to be stable, u_{gs} is maintained at the Miller voltage V_{mil1}, and the driving current i_g almost all flows through C_{gd}, making u_{gd} and u_{ds} drop. The related expression is written as (2).

$$\begin{cases} u_{gd} = -\frac{(V_{CC}-V_{mil1})(t-t_2)}{(R_{on}+R_{int})C_{gd}} + V_{dc} - V_{mil1} \\ V_{mil1} \approx \frac{I}{g_{fs}} + V_{th} \\ u_{ds} = u_{gd} + V_{mil1} \end{cases} \tag{2}$$

Stage 3 ($t \in [t_3, t_4]$): at t_3, u_{ds} drops to near 0, V_{CC} charges C_{gs} again, and u_{gs} continues to rise to V_{CC}. The expression of driving current in the whole turn-on transient can be written as (3).

$$i_g = \frac{V_{CC} - u_{gs}}{R_{on} + R_{int}} \tag{3}$$

Fig. 2 (b) is the typical turn-off transient waveform using CGD. According to the different driving current paths, this transient is divided into three stages, too.

Stage 4 ($t \in [t_5, t_6]$): in this stage, C_{gs} discharges through V_{EE} and the driving resistance R_{off} until u_{gs} reaches the Miller voltage V_{mil2}.

Stage 5 ($t \in [t_6, t_7]$): in this stage, u_{gs} is maintained at V_{mil2}, the driving current i_g almost all flows through C_{gd}, making u_{gd} and u_{ds} rise. The related expression is written as (4).

$$\begin{cases} u_{gd} = \frac{V_{mil2}(t-t_6)}{(R_{off}+R_{int})C_{gd}} \\ V_{mil2} \approx \frac{I}{g_{fs}} + V_{th} \\ u_{ds} = u_{gd} + V_{mil2} \end{cases} \tag{4}$$

Stage 6 ($t \in [t_7, t_9]$): at t_7, u_{ds} reaches V_{dc}, C_{gs} discharges through V_{EE} again, and i_d begins to drop. At t_8, u_{gs} drops to the threshold voltage V_{th}, and i_d drops to 0.

$$\begin{cases} u_{gs} = V_{mil2}e^{-\frac{t-t_7}{(R_{off}+R_{int})C_{gs}}} \\ i_d = g_{fs}\left(u_{gs} - V_{th}\right), \quad t_7 < t < t_8 \end{cases} \tag{5}$$

After t_8, C_{gs} discharges through V_{EE} again, and u_{gs} continues to drop to $-V_{EE}$. Similarly to equation (3), the expression of i_g in the whole turn-off transient can be written as (6).

$$i_g = \frac{-V_{EE} - u_{gs}}{R_{off} + R_{int}} \tag{6}$$

Based on the above analysis, the voltage oscillation in turn-on transient occurs at t_3. When u_{ds} drops to near 0, the change rate will suddenly decrease, and i_D will cause the voltage oscillation of u_D under the resonance between C_D and L_p. In order to simplify the analysis, the total resistance

of the main circuit is ignored, and the relation is written as (7).

$$L_pC_D\frac{d^2u_D}{dt^2}+u_D=V_{dc} \tag{7}$$

According to the root formula, the form of u_D can be written as (8), and A is the oscillation amplitude, B is the oscillation period, and C is the oscillation phase.

$$\begin{cases} u_D = Acos(Bt + C) + V_{dc} \\ B = \frac{1}{\sqrt{L_pC_D}} \end{cases} \tag{8}$$

The initial value of i_D is $-i_{gt3}C_D/C_{gd}$, where i_{gt3} is the driving current at t_3 in turn-on transient. Therefore the expression of oscillation amplitude A can be solved as (9).

$$A=\frac{i_{gt3}\sqrt{L_pC_D}}{C_{gd}} \tag{9}$$

The voltage oscillation in turn-off transient occurs at t_7. Due to the drop of i_d, L_p will generate a reverse voltage drop, and u_{ds} will overshoot and oscillate [27]. The peak value of u_{ds} is written as (10), where i_{gt2} is the driving current at t_2 in turn-off transient.

$$u_{dsp}=V_{dc}+L_p\frac{di_d}{dt}\approx V_{dc}+L_p\frac{i_{gt2}g_{fs}}{C_{gs}} \tag{10}$$

From the equations (9) and (10), the voltage oscillation amplitude is positively related to the driving current at t_3 in turn-on transient and t_7 in turn-off transient. If i_g is too large, the oscillation amplitude will be significant, which will endanger the device's safety. Directly increasing the driving resistance of CGD can effectively reduce i_g, but it will also lead to a significant decrease in driving speed and increase the switching loss.

III. SERIES CAPACITANCE GATE DRIVER AND ANALYSIS

A. CIRCUIT TOPOLOGY

Based on the attenuation principle of driving current in the Miller plateau, this article proposes the SCGD to improve SiC MOSFET voltage oscillation while optimizing switching loss.

The proposed SCGD only adds passive components, as shown in Fig. 3. C_{sc} is the series capacitance. u_{sc} is the voltage of C_{sc}, and its polarity is shown as a positive sign. Since C_{sc} is connected in series in the circuit, the high-level voltage of T_1 needs to be $V_{CC}+V_Z$ to ensure that the steady-state turn-on voltage of u_{gs} can reach V_{CC}. Z is a unidirectional Zener diode, and the clamping voltage is V_Z, which can avoid the C_{sc} overcharge. C_a, R_a, D_{a1} and D_{a2} constitute auxiliary branches, and u_a is the voltage of C_a. In turn-on transient, to ensure that the charging of C_a does not affect the charging of C_{sc}, set the appropriate value of R_a to make the charging rate of C_a less than that of C_{sc}, and then make D_{a2} turned off. In turn-off transient, C_a and C_{sc} discharge parallel, as shown in Fig. 7. The function of the auxiliary branch is to provide a free degree for parameters design.

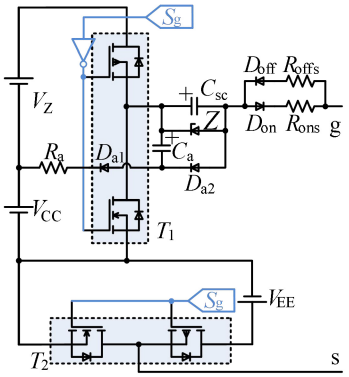


FIGURE 3. Topology of the proposed SCGD.

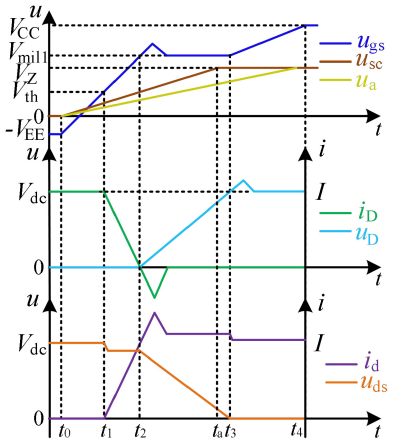


FIGURE 4. Typical turn-on transient waveform using SCGD.

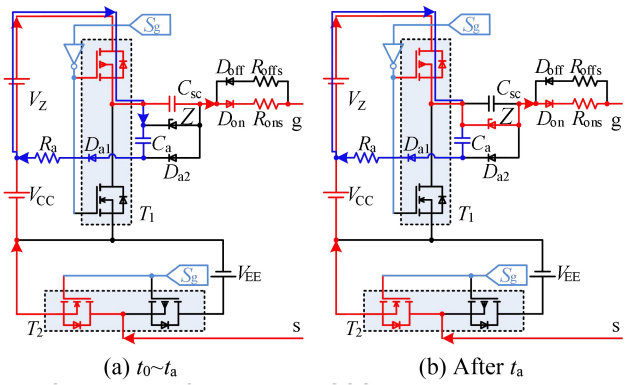


FIGURE 5. Current path of the proposed SCGD in turn-on transient.

B. OPERATION PRINCIPLE

According to the analysis in Section II, the voltage oscillation and loss are both affected by the driving current. Therefore, the main focus of this part is on the driving current difference between the SCGD and the CGD.

The typical turn-on transient waveform and current path using SCGD are shown in Fig. 4 and 5. Similarly to equation (3), the driving current of SCGD is also the driving resistance voltage divided by its resistance value, as shown

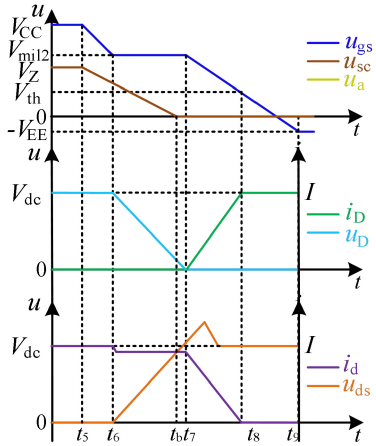


FIGURE 6. Typical turn-off transient waveform using SCGD.

in (11).

$$i_g = \frac{V_{CC} + V_Z - u_{sc} - u_{gs}}{R_{ons} + R_{int}} \tag{11}$$

Unlike equation (3), equation (11) contains the variable of series capacitance voltage u_{sc}. According to the analysis of stages 1 to 3 in behavior model, the driving current will flow to different parasitic capacitance at different time. Combined with the current paths in Fig. 5, the expression of u_{sc} can be described in three stages.

In $t_0 \sim t_2$, V_{CC} and V_Z are connected in series to charge C_{sc} and C_{gs}. The expression is written as follow, and C_{eq1} is defined as $C_{gs} \parallel C_{sc}$.

$$\begin{cases} u_{gs} = \frac{C_{sc}}{C_{sc}+C_{gs}}(V_{CC} + V_Z + V_{EE})\left[1 - e^{-\frac{t-t_0}{(R_{ons}+R_{int})C_{eq1}}}\right] \\ -V_{EE} \\ u_{sc} = \frac{C_{gs}}{C_{sc}+C_{gs}}V_{CC} + V_Z + V_{EE}\left[1 - e^{-\frac{t-t_0}{(R_{ons}+R_{int})C_{eq1}}}\right] \end{cases} \tag{12}$$

In $t_2 \sim t_a$, because u_{gs} is maintained at V_{mil1}, V_{CC} and V_Z are connected in series to charge C_{sc}. The expression is written as (13).

$$\begin{cases} u_{gs} = V_{mil1} \\ u_{sc} = \left[V_{CC} + V_Z - V_{mil1} - \frac{C_{gs}(V_{mil1}+V_{EE})}{C_{sc}}\right] \\ \left[1 - e^{-\frac{t-t_2}{(R_{ons}+R_{int})C_{sc}}}\right] + \frac{C_{gs}(V_{mil1}+V_{EE})}{C_{sc}} \end{cases} \tag{13}$$

After t_a, u_{sc} is maintained at V_Z under the clamping action of the Zener diode Z. By substituting this value into equation (11), the expression of the driving current returns to the same form as CGD.

In addition, V_Z will also charge C_a through the auxiliary branch to prepare for the discharge in turn-off transient, as shown by the blue line in Fig. 5.

The typical turn-off transient waveform and current path using SCGD are shown in Fig. 6 and 7. Similarly to equation (6), the driving current of SCGD is written as (14).

$$i_g = \frac{-V_{EE} - u_{sc} - u_{gs}}{R_{offs} + R_{int}} \tag{14}$$

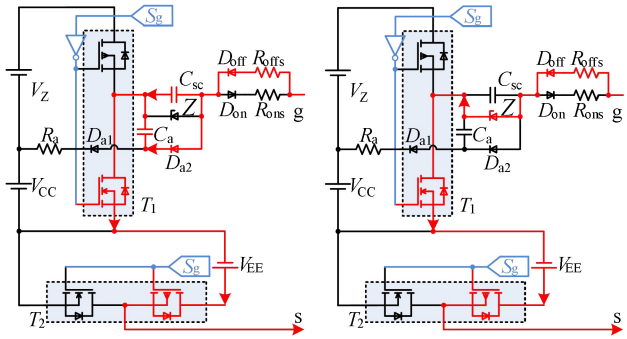


FIGURE 7. Current path of the proposed SCGD in turn-off transient.

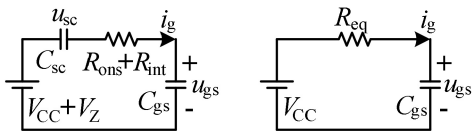


FIGURE 8. Current path of the proposed SCGD in turn-on transient.

According to the analysis of stages 4 to 6 in behavior model, the driving current will flow to different parasitic capacitance at different time. Combined with the current paths in Fig. 7, the expression of u_{sc} can be described in three stages.

In $t_5 \sim t_6$, C_{sc} and C_a are connected in parallel and then discharge in series with C_{gs}. The expression is written as follow, and C_{eq2} is defined as $C_{gs} \parallel (C_{sc}+C_a)$.

$$\begin{cases} u_{gs} = \frac{C_{sc}+C_a}{C_{sc}+C_a+C_{gs}}(V_{CC} + V_Z + V_{EE}) \\ \left[e^{-\frac{t-t_5}{(R_{offs}+R_{int})C_{eq2}}} - 1\right] + V_{CC} \\ u_{sc} = \frac{C_{gs}}{C_{sc}+C_a+C_{gs}}(V_{CC} + V_Z + V_{EE}) \\ \left[e^{-\frac{t-t_5}{(R_{offs}+R_{int})C_{eq2}}} - 1\right] \end{cases} \tag{15}$$

In $t_6 \sim t_b$, because u_{gs} is maintained at V_{mil2}, C_{sc} and C_a discharge in parallel. The expression is written as (16).

$$\begin{cases} u_{gs} = V_{mil2} \\ u_{sc} = \left[-V_{EE} - V_{mil2} - V_Z + \frac{C_{gs}(V_{CC}-V_{mil2})}{C_{sc}+C_a}\right] \\ \left[e^{-\frac{t-t_6}{(R_{offs}+R_{int})(C_{sc}+C_a)}} - 1\right] + V_Z - \frac{C_{gs}(V_{CC}-V_{mil2})}{C_{sc}+C_a} \end{cases} \tag{16}$$

After t_b, u_{sc} is maintained at 0 under the freewheeling effect of Z. By substituting this value into equation (14), the expression of the driving current returns to the same form as CGD.

For the convenience of comparison with CGD, the voltage change of series capacitance can be equivalent to the change of driving resistance, as shown in Fig. 8.

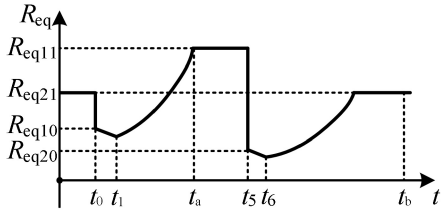


FIGURE 9. Equivalent driving resistance of SCGD.

Making the driving currents before and after the equivalence in Fig. 8 equal, the expression of the SCGD equivalent driving resistance R_{eq} is obtained as equation (17).

$$\begin{cases} R_{eq1} = \dfrac{(V_{CC}-u_{gs})(R_{ons}+R_{int})}{V_{CC}+V_Z-u_{sc}-u_{gs}}, & \text{turn}-\text{on} \\ R_{eq2} = \dfrac{(-V_{EE}-u_{gs})(R_{offs}+R_{int})}{-V_{EE}-u_{sc}-u_{gs}}, & \text{turn}-\text{off} \end{cases} \tag{17}$$

Substituting the expressions of u_{gs} and u_{sc} in each stage into equation (17), the equivalent driving resistance curve of SCGD is obtained as shown in Fig. 9.

Fig. 9 is the driving resistance curve, and the expression of relevant variables is shown as (18).

$$\begin{cases} R_{eq10} = \dfrac{(V_{CC}+V_{EE})(R_{ons}+R_{int})}{V_{CC}+V_Z+V_{EE}} \\ R_{eq11} = R_{ons}+R_{int} \\ R_{eq20} = \dfrac{(-V_{EE}-u_{gs})(R_{offs}+R_{int})}{-V_{EE}-u_{sc}-u_{gs}} \\ R_{eq21} = R_{offs}+R_{int} \end{cases} \tag{18}$$

According to Fig. 9, the driving resistance curve of SCGD is gradually increasing in the switching transient. If t_a is set before t_3 and t_b is set before t_7 through reasonable parameters design, the voltage oscillation can be suppressed. Compared with CGD's method of directly increasing the driving resistance to R_{eq11} and R_{eq21} to suppress voltage oscillation, the average driving resistance of SCGD in $t_0 \sim t_a$ and $t_5 \sim t_b$ is smaller than that of CGD, that is, the switching loss is taken into account while optimizing voltage oscillation.

C. PARAMETERS DESIGN

C.1. CONSTRAINT OF VOLTAGE OSCILLATION IN TURN-ON TRANSIENT

The voltage oscillation in turn-on transient will affect the safety of the diode D. According to the previous analysis, the voltage oscillation amplitude of u_D in the turn-on transient is positively related to the value of i_g at t_3. To suppress the voltage oscillation as much as possible, u_{sc} must reach V_Z before t_3. However, realizing the clamping of Z in advance will slow down the driving speed and increase the loss. Therefore, it is necessary to make the time when u_{sc} reaches V_Z close to t_3 as much as possible. According to (2), when I is around 0, V_{mil1} is the minimum, and u_{sc} at t_3 is the minimum. This constraint should be satisfied by making u_{sc} reach V_Z at t_3 in this case, and can be written as (19).

$$C_{sc} = \frac{C_{gd}V_{dc}}{V_Z - n(V_{mil1}|_{I=0} + V_{EE})} \tag{19}$$

When I is greater than 0, the driving resistance can always reach the maximum value R_{eq11} before t_3, ensuring the voltage oscillation suppression effect at different current levels.

In addition, due to the small driving resistance at t_1, the driving current may be large, leading to large drain current oscillation, gate-source oscillation and crosstalk. Therefore, the driving resistance at t_1 should be controlled at a suitable value R_{onm}, and the constraint can be written as (20).

$$\begin{cases} C_{gs} = nC_{sc} \\ \dfrac{V_{CC}+V_Z-(n+1)V_{mil1}|_{I=0}-nV_{EE}}{R_{ons}+R_{int}} = \dfrac{V_{CC}-V_{mil1}|_{I=0}}{R_{onm}+R_{int}} \end{cases} \tag{20}$$

C.2. CONSTRAINT OF VOLTAGE OSCILLATION IN TURN-OFF TRANSIENT

The voltage oscillation in the turn-off transient will affect the safety of the SiC MOSFET, and under the coupling effect of Miller capacitance, it will lead to a large oscillation of u_{gs}, which is easy to cause negative gate breakdown. According to the previous analysis, the voltage oscillation amplitude of u_{ds} in turn-off transient is positively related to the value of i_g at t_7. To suppress the voltage oscillation as much as possible, u_{sc} must reach 0 before t_7. However, realizing the freewheeling of Z in advance will slow down the driving speed and increase the loss. Therefore, it is necessary to make the time when u_{sc} reaches 0 close to t_7 as much as possible. According to (4), when I is equal to the rated load current I_e, V_{mil2} is the maximum and u_{sc} at t_7 is the maximum. This constraint should be satisfied by making u_{sc} reach 0 at t_2 in this case, and can be written as (21).

$$C_{sc} + C_a = \frac{C_{gs}(V_{CC} - V_{mil2}|_{I=Ie}) + C_{gd}V_{dc}}{V_Z} \tag{21}$$

When I is less than I_e, the driving resistance can always reach the maximum value R_{eq21} before t_7, ensuring the voltage oscillation suppression effect at different current levels. Similarly, the driving resistance at t_6 should be controlled at a suitable value R_{offm}, and the constraint can be written as (22).

$$\begin{cases} n_a = \dfrac{C_{gs}}{C_{sc}+C_a} \\ \dfrac{V_Z+V_{EE}+(n_a+1)V_{mil2}|_{I=Ie}-n_aV_{CC}}{R_{offs}+R_{int}} = \dfrac{V_{EE}+V_{mil2}|_{I=Ie}}{R_{offm}+R_{int}} \end{cases} \tag{22}$$

C.3. EFFECT OF N ON EQUIVALENT RESISTANCE

n is taken as the independent variable to observe its effect on performance. When the constraint *1)* and *2)* are met, the change of equivalent driving resistance curve with different n values is shown in Fig. 10.

According to Fig. 10, the larger the value of n, the larger the value of the equivalent driving resistance at ta, which means that the ability to suppress voltage oscillation is stronger. However, the average value of the equivalent resistance in the switching transient is also larger, which means that the switching loss will increase. Therefore, the value of n should be selected according to the specific situation.

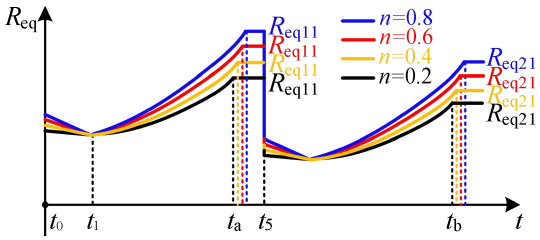
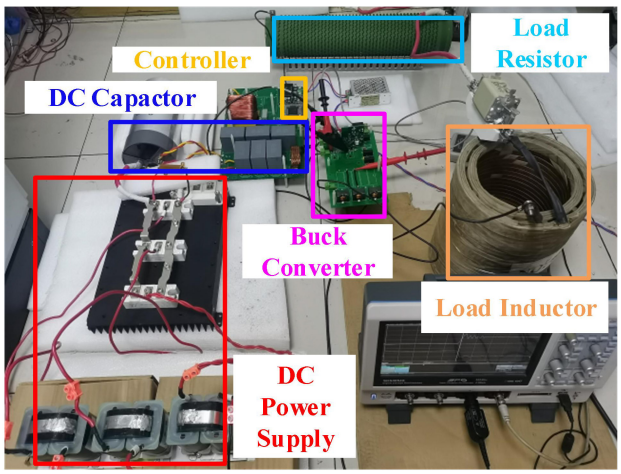
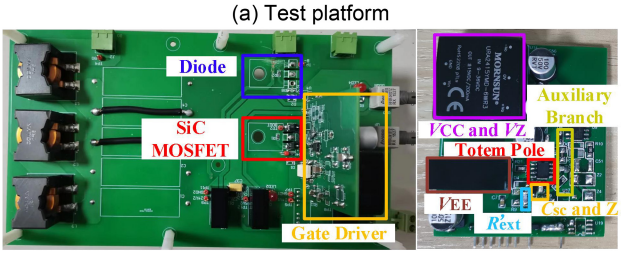


FIGURE 10. R_{eq} of SCGD at different n in turn-on transient.



(a) Test platform



(b) BUCK converter and gate driver

FIGURE 11. Switching test platform.

TABLE 1. Measurement equipments types.

Category	Type	Bandwidth
Oscilloscope	SDS3054X, SIGLENT	500MHz
Voltage probe	P5100A, Tektronics	500MHz
Current probe	SSDN-414-10, T&M	2000MHz

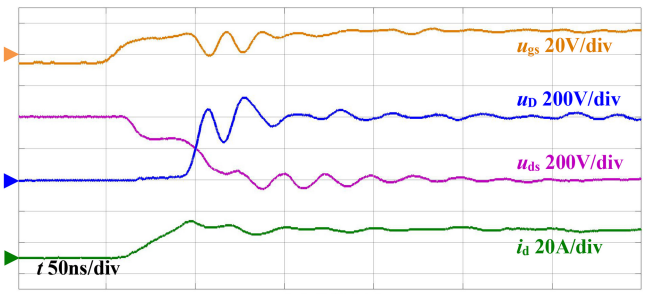
C.4. CONSTRAINT OF AUXILIARY RESISTANCE

The design of R_a should consider that the rising rate of u_a is lower than u_{sc} in turn-on transient to avoid affecting the turn-on loss. On the other hand, u_a should rise to V_Z before the minimum pulse width time T_{pmin} to avoid affecting the turn-off loss. The parameters relationship of this constraint is written as (23).

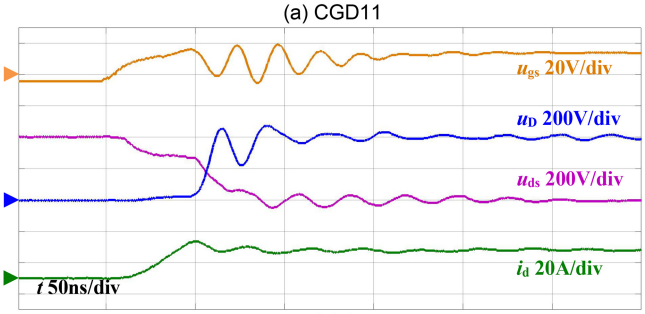
$$\begin{cases} R_a C_a > \frac{C_{sc} C_{gs}}{C_{sc}+C_{gs}} (R_{ons} + R_{int}) \\ R_a C_a < \frac{T_{pmin}}{4} \end{cases} \tag{23}$$

TABLE 2. Main experimental parameters.

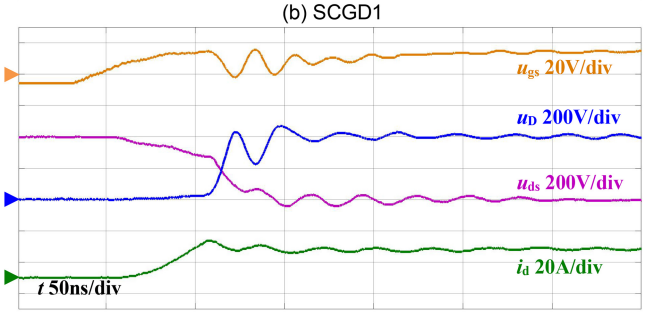
Category	Parameter	Value
\	DC voltage V_{dc}	400V
\	Load current I	17.5A
\	Positive driving voltage V_{CC}	15V
\	Negative driving voltage V_{EE}	5V
CGD11	Driving resistance R_{on1} and R_{off1}	10Ω
CGD12	Driving resistance R_{on1} and R_{off1}	30Ω
SCGD1	Driving resistance R_{ons} and R_{offs}	30Ω
CGD21	Driving resistance R_{on1} and R_{off1}	5Ω
CGD22	Driving resistance R_{on1} and R_{off1}	20Ω
SCGD2	Driving resistance R_{ons} and R_{offs}	20Ω
SCGD1 and 2	clamping voltage V_Z	15V
SCGD1 and 2	Series capacitance C_{sc}	738pF
SCGD1 and 2	Auxiliary capacitance C_a	500pF
SCGD1 and 2	Auxiliary resistance R_a	50Ω



(a) CGD11



(b) SCGD1



(c) CGD12

FIGURE 12. Experimental waveforms in turn-on transient (1st group).

C.5. FULL ACCELERATION MODE

When the stray inductance of the system can be reduced to a very small value, the voltage oscillation of the SiC MOSFET will also be significantly reduced. In this case, faster driving speed can be pursued to further reduce switching loss and improve power density. However, the gate internal resistance of SiC MOSFET is usually large, which limits

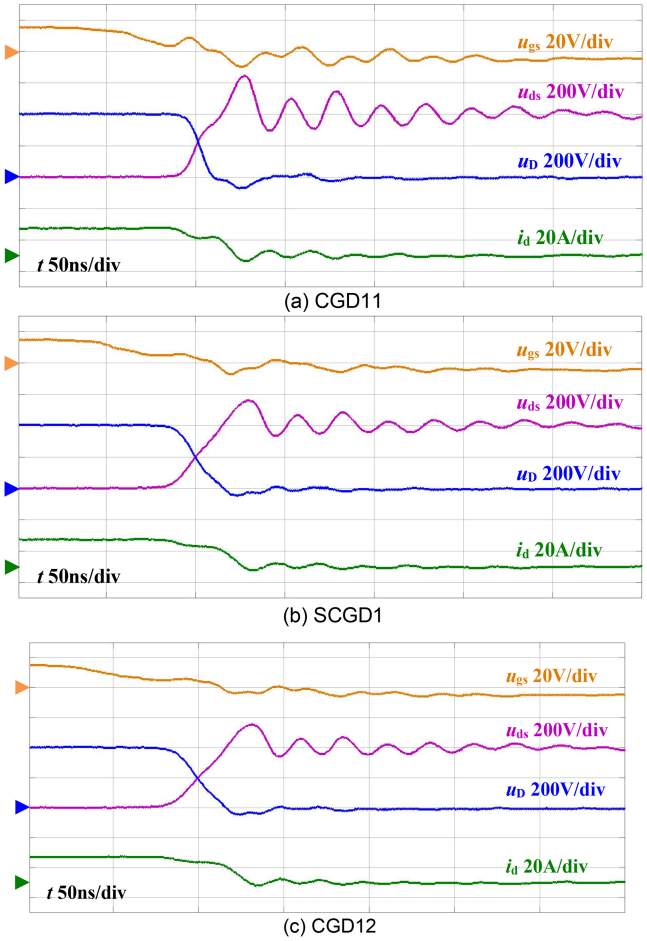


FIGURE 13. Experimental waveforms in turn-off transient (1st group).

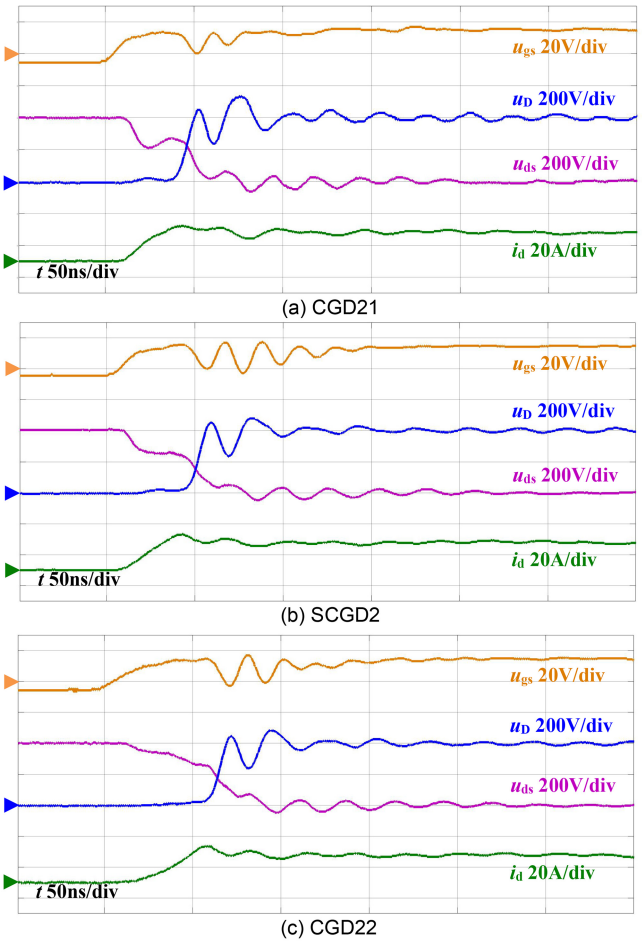


FIGURE 14. Experimental waveform in turn-on transient (2nd group).

TABLE 3. Switching loss and voltage oscillation amplitudes of 1st group.

Category	E_{on}	E_{off}	V_D peak value	V_{ds} peak value
CGD11	177uJ	79uJ	519V	645V
SCGD1	198uJ	104uJ	473V	561V
CGD12	223uJ	123uJ	470V	554V

the improvement of its switching speed. If SCGD is used, we can reduce its external driving resistant and increase the values of V_Z and C_{sc} at the same time. Through reasonable parameters design, its equivalent driving resistance is lower than R_{int}, which can further improve the switching speed.

IV. EXPERIMENTAL RESULTS

The Buck converter shown in Fig. 11 is built as a switching test circuit for experimental verification. The SiC MOSFET adopts CREE C3M0120090D and the diode adopts CREE C3D16065D.

Because the switching transient of SiC MOSFET is very fast, the bandwidth of measurement equipments needs to be very high. The principles for selecting bandwidth and measurement equipments is shown in [28], and the expression of bandwidth constraint is shown as follows.

$$f_{bd} \geq k\frac{0.35}{\min(t_r,\ t_f)} \tag{24}$$

In equation (24), k is the coefficient, t_r is the rising time of SiC MOSFET and t_f is the falling time. According to [28], when k is taken from 3 to 5, the measurement error of amplitude is small. When k is taken as 10, the measurement error of phase is small. Therefore, k is taken as 10 in this article. In addition, t_r and t_f can be determined according to the datasheet of SiC MOSFET. By substituting the above values into equation (24), it can be concluded that the bandwidth of measurement equipments should be greater than 500MHz. The specific types of measurement equipments are shown in the Table 1.

The voltage probe and current probe in Table 1 are both passive probes. Therefore, u_{gs}, u_{ds}, u_D, and i_d are measured separately based on the reference signal in actual measurement. In addition, the power supply of the oscilloscope is isolated by a transformer and common mode inductors are connected in series at the output of DC power and the input of control power to suppress common mode interference in the measurement [28].

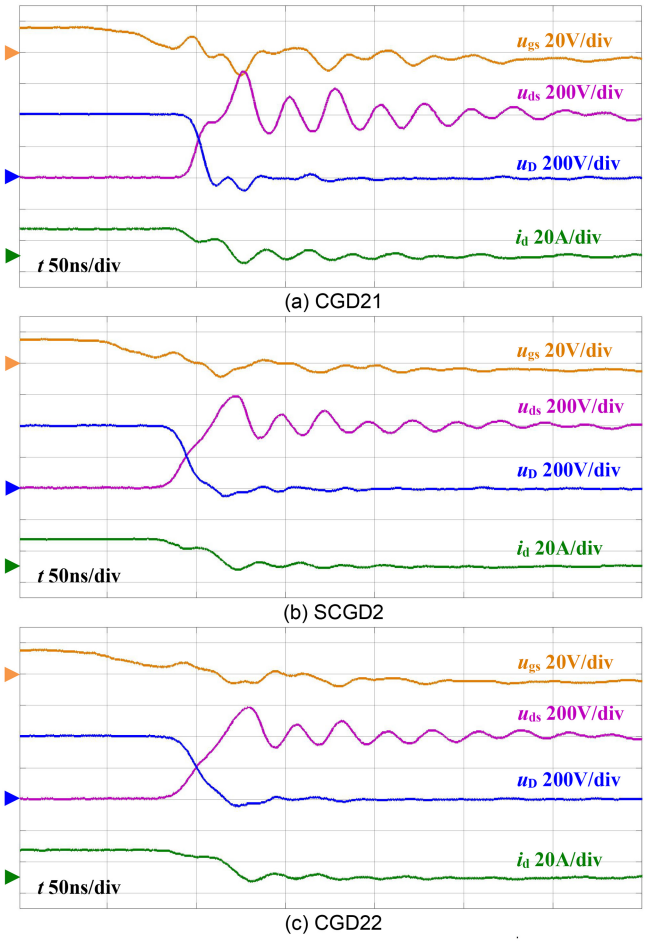


FIGURE 15. Experimental waveform in turn-off transient (2nd group).

According to Fig. 10, if the value of n is larger, the driving resistance of SCGD will also be larger under the parameters constraints, which means that the voltage oscillation suppression effect is better, but the switching loss is also larger. In order to obtain balanced performance, the value of n should be moderate. This article takes n=0.55 as an example to carry out the experiment, and the relevant parameters are shown in the following table.

The first group of experiments will compare the performance of CGD11, CGD12, and SCGD1. The experimental waveforms are shown in Fig. 12 and Fig. 13.

The switching loss calculation results and voltage oscillation amplitudes of the first group are shown in Table 3. Compared with CGD11, SCGD1 has a better voltage oscillation level. For SCGD1, the peak value of u_D is 473V, and the oscillation amplitude accounts for 18.3% of V_{dc}, which is lower than 519V (29.8%) of CGD11. The peak value of u_{ds} is 561V (40.3%), which is lower than 645V (61.3%) of CGD11. Compared with CGD12, the driving resistance value of SCGD1 is the same. Therefore, the voltage oscillation amplitude of SCGD1 is similar to that of CGD12. But, SCGD1 has certain advantages in switching loss. The turn-on loss of SCGD is 198uJ, which is lower than 223uJ of CGD12. The turn-off loss of SCGD1 is 104uJ, which is lower than 123uJ of CGD12. The total loss has been optimized by about 12.7% compared to that of CGD12.

TABLE 4. Switching loss and voltage oscillation amplitudes of 2nd group.

Category	E_{on}	E_{off}	V_D peak value	V_{ds} peak value
CGD21	163uJ	68uJ	533V	680V
SCGD2	185uJ	94uJ	480V	586V
CGD22	204uJ	110uJ	485V	589V

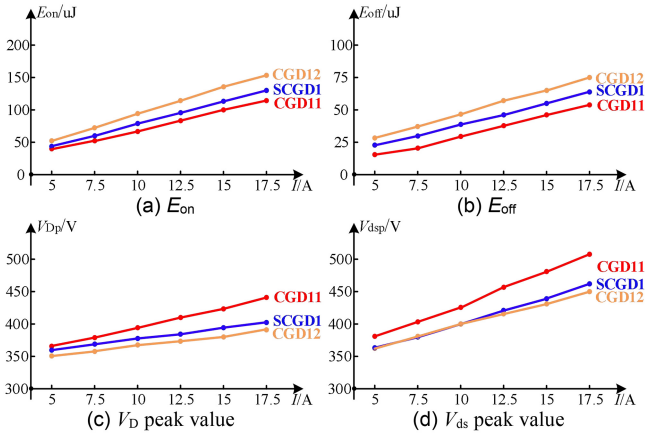


FIGURE 16. Experimental results under different current levels (V_{dc} = 300V).

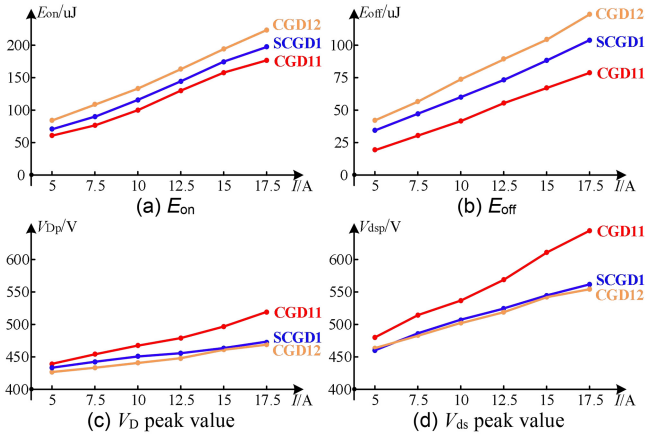


FIGURE 17. Experimental results under different current levels (V_{dc} = 400V).

The driving resistances used in the second group of experiments is different from that of the first group. The experimental waveforms are shown in Fig. 14 and Fig. 15.

The switching loss calculation results and voltage oscillation amplitudes of the first group are shown in Table 4. Compared with CGD21, SCGD2 has a better voltage oscillation level. For SCGD2, the peak value of u_D is 480V, and the oscillation amplitude accounts for 20% of V_{dc}, which is lower than 533V (33.3%) of CGD21. The peak value of u_{ds} is 586V (46.5%), which is lower than 680V (70%) of CGD21. Compared with CGD22, the driving resistance value

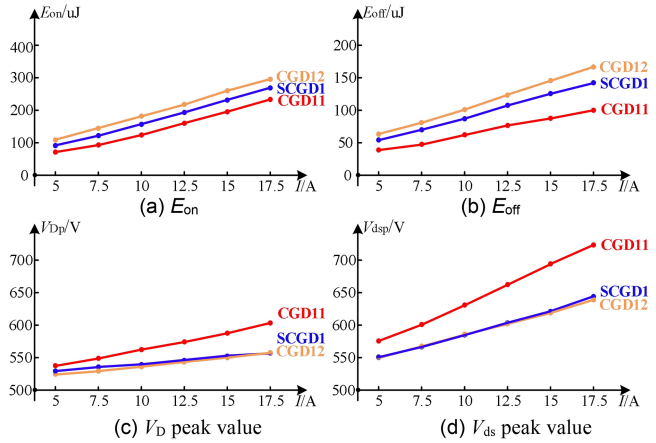


FIGURE 18. Experimental results under different current levels (V_{dc} = 500V).

of SCGD2 is the same. Therefore, the voltage oscillation amplitude of SCGD2 is similar to that of CGD22. Same as the first group, SCGD2 also has certain advantages in switching loss. The turn-on loss of SCGD2 is 185uJ, which is lower than 204uJ of CGD22. The turn-off loss of SCGD2 is 94uJ, which is lower than 110uJ of CGD22. The total loss has been optimized by about 11.1% compared to that of CGD22.

In order to further verify the effectiveness of SCGD, this article takes the driving resistance of the first group as an example and conducts experiments at different voltage and current levels. The experimental results are shown in the following figures.

According to the experimental results in Fig. 16, 17 and 18, under different current and voltage levels, the voltage oscillation amplitude of SCGD1 is smaller than that of CGD11, and its switching loss is better than that of CGD12 when the voltage oscillation amplitude is similar. The above experimental results show that SCGD achieves both voltage oscillation suppression and switching loss optimization compared with CGD, and means that SCGD has advantages in device safety, EMI suppression and efficiency.

V. CONCLUSION

This article proposes a series capacitance gate driver (SCGD) for SiC MOSFET. The circuit structure is simple without any control and easy to be applied in engineering. Compared with the conventional gate driver (CGD), the proposed SCGD realizes the optimization of both voltage oscillation and switching loss, which is conductive to device safety, EMI suppression and efficiency. Besides, SCGD is also applicable to Si MOSFET and IGBT due to their noticeable Miller plateau effect.

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