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Superior Turn-Off dV/dt Controllability From Suppression of Dynamic Avalanche in 3300V Scaled IGBTs

XIANG ZHOU, MUNETOSHI FUKUI, KIYOSHI TAKEUCHI (Member, IEEE), TAKUYA SARAYA (Member, IEEE), AND TOSHIRO HIRAMOTO (Member, IEEE)

Institute of Industrial Science, The University of Tokyo, Meguro 153-8505, Tokyo, Japan

Corresponding author: X. ZHOU (e-mail: zhou-xiang996@g.ecc.u-tokyo.ac.jp)

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ABSTRACT Systematic comparison of dynamic performance has been made among 3300V scaled IGBTs with scaling factor (k) from 1 to 10 by TCAD simulations. The results from a new evaluation method demonstrate superior turn-off dV/dt controllability in scaled IGBTs, regardless of stronger Injection Enhancement (IE) effect. On the basis of physical reason analysis, including the extraction of extra energy and charge quantity generated from impact ionization, it's convinced that Dynamic Avalanche (DA) is suppressed in scaled IGBTs successfully. Thus IGBT scaling method is proven to be able to break through the trade-off relationships between lower on-state voltage drop and better switching controllability, also lower switching power loss.

INDEX TERMS IGBT, scaling, TCAD simulation, dynamic avalanche, switching controllability.

I. INTRODUCTION

The concept of IGBT scaling, where all the geometrical dimensions in MOS parts as well as gate voltage are scaled down proportionately, has been proposed to enhance the IGBT performances [1], [2]. We have successfully fabricated scaled IGBTs and demonstrated better E_{off}-$V_{ce,sat}$ trade-off relationship in scaled IGBTs [3], [4], [5], where E_{off} is turn-off loss and $V_{ce,sat}$ is on-state voltage. The studies from more various aspects of scaled IGBTs have continued to go deeper to achieving real application [6], [7].

On the other hand, the dynamic avalanche (DA), which happens locally at lower reverse bias than static breakdown voltage, poses fundamental performance limits and reliability concerns on conventional IGBTs [8], [9]. The major negative influence of DA to device performance, higher switching power loss and worse controllability, has been emphasized from previous works [10], [11], [12], [13]. Several physical models based on physical analysis of DA during the turn-off process have enabled people to evaluate quantitatively and figure out ways to refrain from DA [14], [15], [16], [17], [18], [19]. Some fairly novel device structures have been proposed and claimed to be able to stop suffering from DA [20], [21], [22], [23].

As easily predicted, DA was projected to be more severe in scaled IGBTs because of higher carrier density by the IE effect, which may lead to dV/dt controllability degradation and reliability problems because of more transient carriers during the turn-off process. Hopefully, the scaling method was reported to be an effective way to stretch the all-round performance of IGBT [24], [25], while more detailed physical analysis applied to the trench gate IGBT is mandatory.

In this paper, a new method of extracting dV/dt controllability has been proposed and applied to comparison of DA among scaled trench IGBTs. Systemic analysis is performed to authenticate the advantages of scaling methods in IGBT from various aspects. This paper is an extended version of a conference presentation [25] and will more thoroughly describe the simulation results and discussion.

II. DEVICE STRUCTURE AND IE EFFECT

As demonstrated in Fig. 1, a full scaling method has been applied to the top cell region in 3300V IGBT with scaling factor k=1, 3, 5, 10. Structural and electrical parameters of reference (k=1) and scaled (k=3, 5, 10) IGBTs are summarized in Table 1. Corresponding device structures

TABLE 1. Structural and electrical parameters of original and scaled trench gate IGBTs.

Parameters	k=1	k=3	k=5	k=10
Cell pitch, W (um)	16	16	16	16
Mesa width, S (um)	3	1	0.6	0.3
Trench depth, D_T (um)	6	2	1.2	0.6
P-base depth, D_P (um)	3	1	0.6	0.3
Trench extrusion, D_T-D_P (um)	3	1	0.6	0.3
Gate oxide thickness, t_{ox} (nm)	100	33.3	20	10
Gate voltage, V_g (V)	15	5	3	1.5
Threshold Voltage, V_{th} (V)	6	2	1.2	0.6
Trench width, W_T (um)	1	0.33	0.20	0.10
Thickness, t_{Si} (um)	360	360	360	360

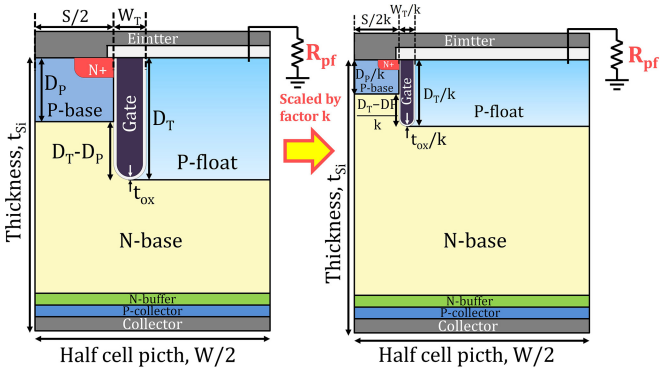

FIGURE 1. Schematic cross section of original and scaled trench gate IGBTs.

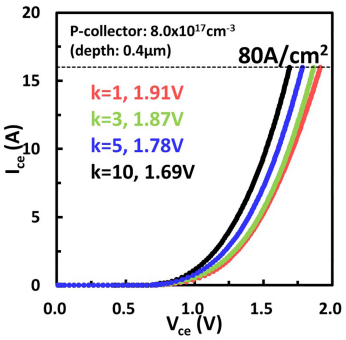

FIGURE 2. On-state characteristics of k=1, k=3, k=5 and k=10 IGBTs.

were generated in TCAD simulation tool for further study. It's worth mentioning that the p-float region in Fig. 1 was connected to ground through an adjustable resistor R_{pf}. The baseline doping concentration and thickness of the P-collector region were 8.0×10^{17}cm^{-3} and 0.4μm that kept invariable in scaled IGBTs. A typical inductive load circuit was used to evaluate turn-off performance, with default operating voltage of 1700V (V_{cc}) and gate voltage source swing of $\pm V_g$. The active area of IGBT was 0.2cm^2 with on-state current of 16A (80A/cm^2).

First, the static performance advantages of scaled IGBT are reviewed. In Fig. 2, the output characteristics of original and scaled IGBTs are overlapped to show the difference. It's

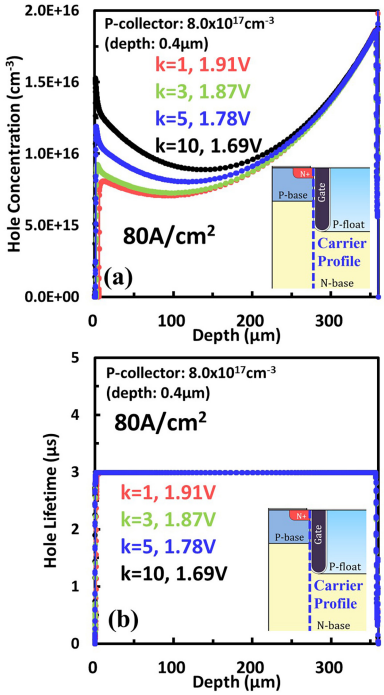

FIGURE 3. (a) Holes carrier profile and (b) holes lifetime profile of k=1, k=3, k=5 and k=10 IGBTs along channel region under current density 80A/cm^2.

obvious that on-state voltage drop $V_{ce,sat}$ has been improved from 1.91V to 1.69V from k=1 to k=10 devices in spite of scaling gate voltage. The lower on-state voltage drop mostly comes from higher carrier density in the n-base region of the emitter side, see Fig. 3(a). This improvement is thanks to stronger IE effect, a well-known benefit from scaling principle in IGBT. In Fig. 3(b), holes carrier lifetime is also compared among original and scaled IGBTs. As defined by the default physical model of silicon, the holes carrier lifetime is about 3μs in all devices. Whereas higher carrier density at emitter side hinders the expansion of space charge region, also increases the transient carrier density in space charge region during turn-off. As a result, a steeper electric field profile with higher maximum value forms under the same switching condition. It becomes reasonable to assume that DA is prone to happen in scaled IGBTs and degrades dynamic performance.

III. COMPARISON OF DV/DT CONTROLLABILITY

The detailed trigger mechanism of DA during turn-off has to be discussed first. A typical switching waveform of k=1 device with gate resistance Rg=72.5Ω is shown in Fig. 4(a), where electron ($I_{E\text{-}e}$) and hole current ($I_{E\text{-}h}$) parts of the emitter electrode are also included. Benefits from the convenience of simulation tools, the hole and electron current parts of each electrode can be plotted separately to facilitate analysis. At time t_2, when V_{ge} reduces to be equal to threshold voltage V_{th}, electron current $I_{E\text{-}e}$ is shut down by MOS gate and hole current $I_{E\text{-}h}$ jumps to 100% I_C.

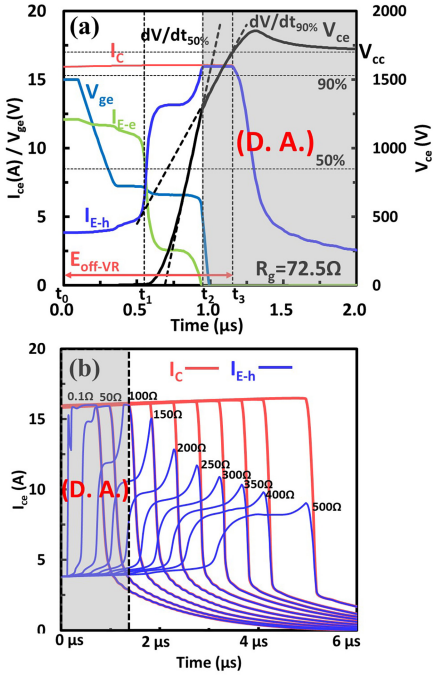

FIGURE 4. (a) A typical turn-off waveforms of k=1 IGBT at $dV/dt_{50\%}$= 5V/ns and Rg= 72.5Ω and (b) emitter hole current of k=1 IGBT at various Rg.

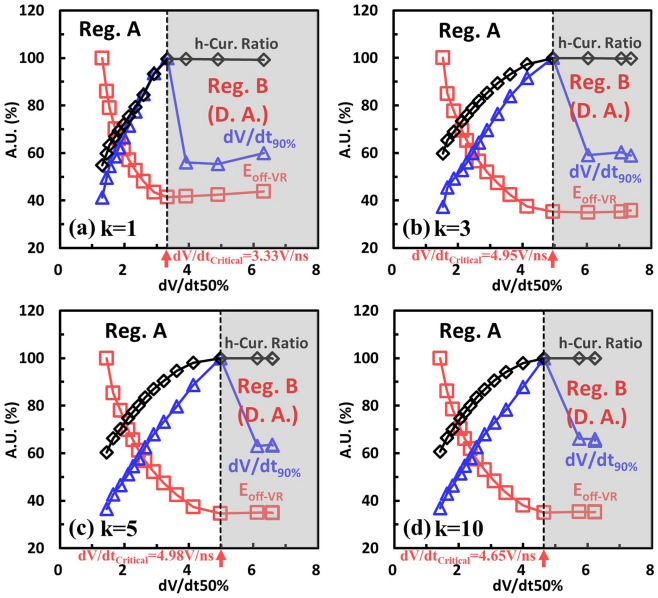

FIGURE 5. Normalized $E_{off\text{-}VR}$, $dV/dt_{90\%}$, and hole current ratio as function of $dV/dt_{50\%}$ of (a) k=1, (b) k=3, (c) k=5 and (d) k=10 IGBTs.

The Eq. (1) shows magnitude of electric field E(t) revolution as function of charge density and space charge region width $W_{SC}(t)$.

$$E(t) = \frac{1}{\varepsilon}\left(qN_D + \frac{J_{E-h}}{V_{sat,p}} - \frac{J_{E-e}}{V_{sat,n}}\right)W_{SC}(t) \qquad (1)$$

where J_{E-e} is electron current density and J_{E-h} is hole current density. From Eq. (1), we know that the sudden increase of hole/electron current ratio lifts the maximum electric field in the space charge region substantially. After that, the DA happens (gray area), and it generates electron/hole pairs and stabilizes the electric field peak value. Besides, the slope of V_{ce} (dV/dt) is reduced because of the stabilized peak electric field value and slower expansion of space charge region because of generated carriers from impact ionization. As a natural result, the total switching power loss also goes higher when DA happens.

It's a common measure to relieve DA under slower switching speed by increasing Rg. It is found that the peak emitter hole current ratio is reduced under slower switching conditions with larger Rg, as the blue lines shown in Fig. 4(b). Under slower switching conditions, the time point that V_{ge} reduces to V_{th} is after the time point that I_C starts to fall. This makes the hole current peak lower than 100% I_C and thus suppresses DA significantly. Therefore, a necessary and sufficient condition to avoid DA is that V_{ge} reaches V_{th} after I_C starts to fall. From the other side, the hole current peak becomes equal to 100% I_C can be taken as a distinguishing feature of whether DA happens.

Now, we start to discuss the controllability of dV/dt. It is indicated previously that DA limits the switching speed as well as controllable range of dV/dt. Then, a judging method is needed for dV/dt controllability comparison. A new method of judging device turn-off controllability by extracting critical dV/dt values will be introduced here. But before that, some essential parameters need to be introduced in Fig. 4(a). Turn-off energy loss of voltage rising part ($E_{off\text{-}VR}$) is calculated by integration of I_C and V_{ce} up to t_3 (when V_{ce}=V_{cc}). Two dV/dt values are calculated as the slopes of V_{ce} at 50% V_{cc} ($dV/dt_{50\%}$) and 90% V_{cc} ($dV/dt_{90\%}$). Hole current ratio is calculated as the ratio between the peak hole current value and the maximum I_C.

Those aforementioned parameters of k=1, 3, 5, 10 devices are normalized to their maximum values and plotted as a function of $dV/dt_{50\%}$ in Fig. 5, where $dV/dt_{50\%}$ was adjusted by varying Rg. Those four graphs are split into two regions A and B with clear boundaries, where region B is dominated by DA. At the boundary of region A/B, saturation of $E_{off\text{-}VR}$, saturation of hole current ratio, and drop of $dV/dt_{90\%}$ occur at same $dV/dt_{50\%}$ value, where strong DA happens and influences the turn-off waveform intensely which should be avoided. The $dV/dt_{50\%}$ value at the boundary is defined as $dV/dt_{Critical}$. Higher $dV/dt_{Critical}$ value represents larger controllable dV/dt range during turn-off that is beneficial for high-frequency applications. Surprisingly, better dV/dt controllability in scaled IGBTs than k=1 case is demonstrated from simulation results and it also indicates that DA is suppressed in scaled IGBTs.

Nevertheless, the change of $dV/dt_{Critical}$ value is not monotonous from k=1 to k=10 devices. It's speculated that the stronger IE effect in scaled IGBT makes the results complicated to analyze. Hence, it would be ideal to eliminate

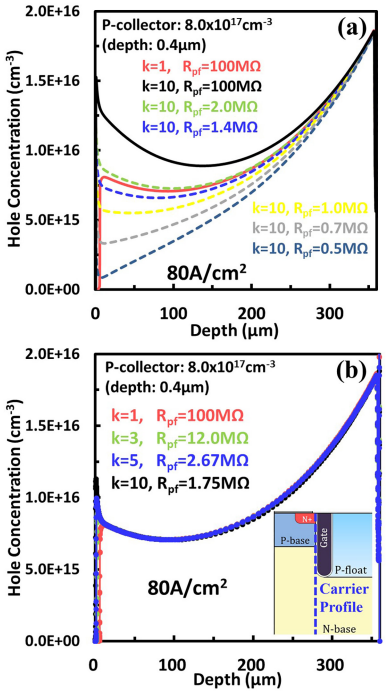

FIGURE 6. (a) Holes carrier profile of k=10 IGBT under different R_{pf} resistance conditions compared to k=1 case; (b) holes carrier profile of k=1, k=3, k=5 and k=10 IGBTs under equivalent IE effect condition after R_{pf} adjustment.

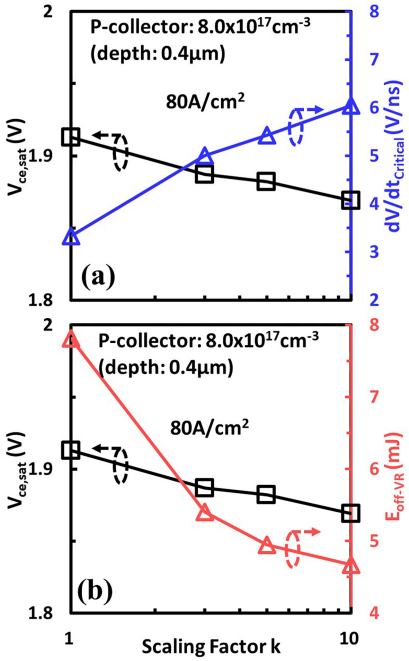

FIGURE 7. Comparison of (a) $dV/dt_{Critical}$ and $V_{ce,sat}$; (b) E_{off-VR} and $V_{ce,sat}$ as function of scaling factor k under equivalent IE effect condition after adjusted by R_{pf}.

the influence of the stronger IE effect in scaled IGBTs and make the circumstance simpler. As a common method in real IGBT device design, p-float region connecting resistor R_{pf} value is used to optimize device performance. It's also found out that different R_{pf} values yield different hole concentration at the emitter side. As Fig. 6(a) shows, the adjustment of R_{pf} value can tune the carrier profile at the emitter side in k=10 IGBT, where the k=1 case is added for reference. Under on-state, the p-float region is another path besides p-base region for holes that are injected from the collector side to go out. Controlling the hole current flows through the p-float region by R_{pf} resistance, the holes density at the emitter side is able to be tuned. Which also means that the strength of IE effect can also be adjusted by R_{pf} resistance value. To get rid of the influence of stronger IE effect in scaled IGBTs, R_{pf} resistance has been adjusted to align carrier profiles of scaled IGBTs with k=1 case, as Fig. 6(b) shows. We call this "equivalent IE effect condition". Compared with the original carrier profile in Fig. 3(a), the carrier profile under equivalent IE effect condition is almost overlapped.

The $dV/dt_{Critical}$ values under the equivalent IE effect condition are extracted and plotted as a function of k in Fig. 7(a), where $V_{ce,sat}$ is also added for comparison. Under this new circumstance (equivalent IE effect condition), $dV/dt_{Critical}$ values are improved monotonously with higher scaling factor from 1 to 10, which demonstrates wider controllable dV/dt range. Moreover, even under the equivalent IE effect condition after R_{pf} is adjusted, slightly better on-state voltage drop is still shown in scaled IGBTs. Since the influence of IE effect on $V_{ce,sat}$ has been removed here which is reflected in the similar carrier profile in drift region. The lower $V_{ce,sat}$ is speculated to benefit from the smaller resistance of MOS channel and mesa parts in scaled IGBTs. Moreover, the power loss E_{off-VR} is demonstrated to be lower in scaled IGBTs, as shown in Fig. 7(b). Those indisputable results indicate that scaled IGBTs can enjoy lower $V_{ce,sat}$, higher $dV/dt_{Critical,}$ lower E_{off-VR} at same time. The following discussion is all built on equivalent IE effect condition.

IV. PHYSICAL REASON AND MORE EVIDENCE

Here, the physical reason behind the suppression of DA in scaled IGBT needs to be discussed. For fair comparison, the physical parameters inside the device should be compared under identical switching condition. The switching waveforms of k=1 and k=10 devices under $dV/dt_{50\%}$=5V/ns have been shown in Fig. 8. The dash line marks the capture time point (t_c) when V_{ce} equals to 1700V. In Fig. 9, the 2D graphs show distribution of electric field and impact ionization rate of k=1 and k=10 devices at the same reverse bias (V_{ce}= 1700V) and under the same switching conditions ($dV/dt_{50\%}$= 5V/ns) as demonstrated in Fig. 8. It's pretty clear that the high electric field and impact ionization rate regions are localized in the neighborhood of trench bottom in k=1 case as shown in Fig. 9(a)-(b), which stems from electric field crowding effect in cylindrical geometry. Whereas in Fig. 9(c)-(d), the k=10 case, the high impact ionization as well as high electric field regions are hardly to be seen under

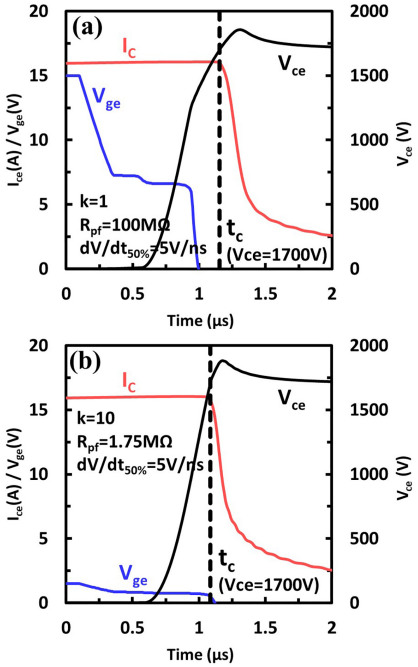

FIGURE 8. **(a) Turn-off waveforms of k=1 IGBT and (b) k=10 IGBT after R_{pf} adjustment, where the dash line (t_c) marks the time point that physical parameters are captured.**

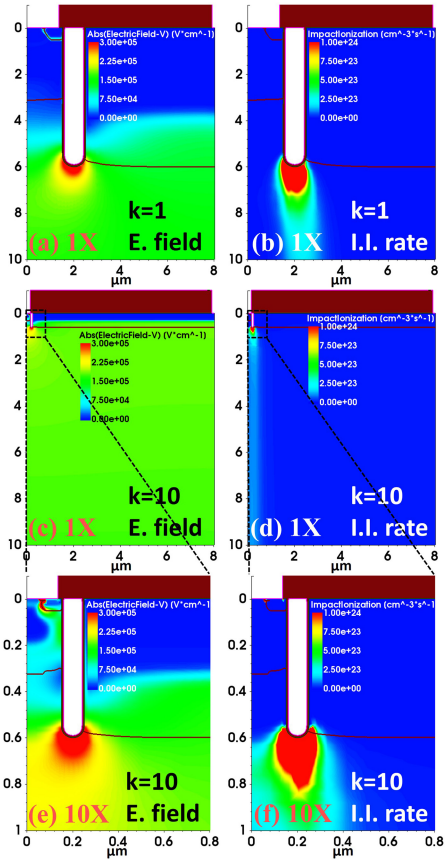

FIGURE 9. **Demonstration of 2D electric field and impact ionization rate of k=1 and k=10 IGBTs when V_{ce} equals to 1700V under $dV/dt_{50\%}$= 5V/ns.**

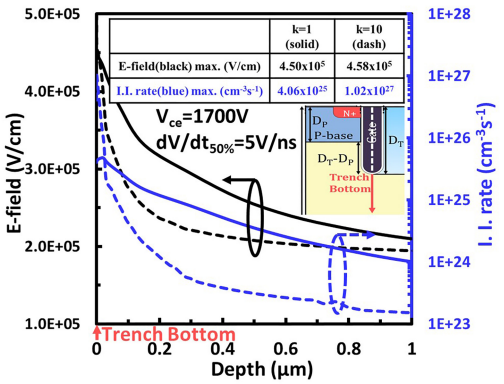

FIGURE 10. **Comparison of 1D electric field and impact ionization rate between k=1 and k=10 IGBTs along trench middle line when V_{ce} equals to 1700V under $dV/dt_{50\%}$=5V/ns condition.**

the same scale. It has to be zoomed in to show the detailed information of k=10 case in Fig. 9(e)-(f). So it's found that DA is limited in an almost 10 times smaller area, compared to k=1 case. In other words, DA is confined to be more localized in scaled IGBTs.

For further comparison, the magnitude of electric field and impact ionization rate along the trench middle line is plotted as a 1D graph in Fig. 10. Although it's seen that the maximum values of both magnitude of electric field and impact ionization rate are higher in scaled IGBT. However, higher maximum values of electric field and impact ionization rate are not equivalent to worse severity of DA. It's more worthwhile to notice that the electric field and impact ionization rate decay more rapidly with distance from trench bottom in the scaled IGBT case. This phenomenon may be attributed to the better electric field uniformity that originates from a smaller mesa region. According to the impact ionization integral, an adequate distance of high enough electric field is essential for avalanche breakdown to happen. In other words, the electric field has to go higher if the space range for impact ionization is limited, just like the scaled IGBT case. As a result, thanks to better electric field uniformity, the condition for DA to happen becomes more stringent in scaled IGBT.

With the convenience of TCAD simulation, we are able to extract the quantity of extra charges (Q_A) and extra energy loss ($\Delta E_{off\text{-}VR}$) generated by DA by enabling or disabling the avalanche generation model in the simulation tool. An example comparison of the switching waveforms of k=1 case with and without avalanche generation model is demonstrated in Fig. 11(a). The Q_A (the gray area between two I_C curves) is calculated by the difference of two integrals of I_C curves over time. The $\Delta E_{off\text{-}VR}$ is just the difference of voltage rising part energy loss calculations of two cases. The Q_A and $\Delta E_{off\text{-}VR}$ values are plotted as a function of scaling factor k in Fig. 11(b). There is no doubt that DA is mitigated in scaled IGBTs since both Q_A and $\Delta E_{off\text{-}VR}$ values become lower with scaling factor k under the same switching condition. It is persuasive that Q_A and $\Delta E_{off\text{-}VR}$ are more significant parameters than maximum values of electric field

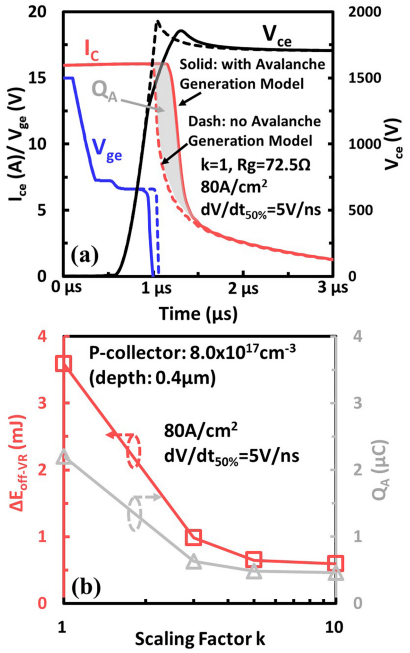

FIGURE 11. (a) Comparison of switching waveforms of k=1 IGBT between with avalanche generation model and without avalanche generation model at $dV/dt_{50\%}$= 5V/ns and Rg= 72.5Ω; (b) change of $\Delta E_{off\text{-}VR}$ and Q_A as function of scaling factor k.

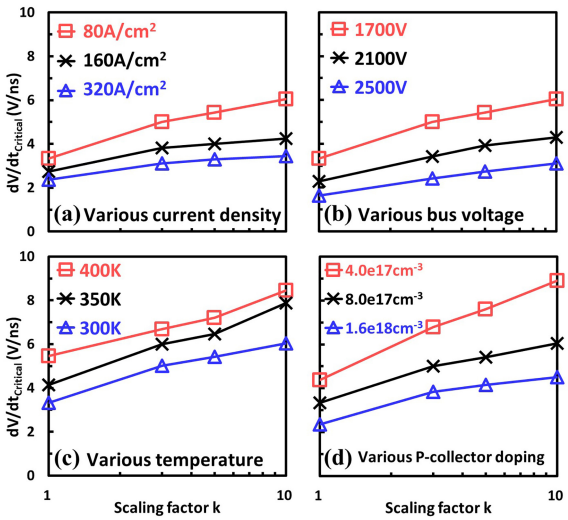

FIGURE 12. Comparison of $dV/dt_{Critical}$ at various (a) on-state current density; (b) bus voltage; (c) ambient temperature and (d) P-collector doping concentration as function of scaling factor k under equivalent IE effect condition after adjusted by R_{pf}.

or impact ionization rate to evaluate the severity of DA during turn-off.

In this part, $dV/dt_{Critical}$ values are compared among scaled IGBTs as function of scaling factor under various switching conditions. In common sense, DA is easier to happen if the turn-off current density goes higher. That is because the higher density of transient carriers in space charge region increases the impact ionization rate. This point has been proven in Fig. 12(a). But even at higher on-state

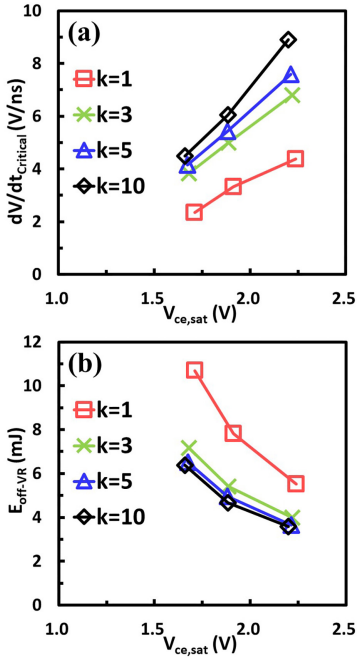

FIGURE 13. Comparison of trade-off relationships between (a) $dV/dt_{Critical}$ vs. $V_{ce,sat}$; (b) E_{off-VR} vs. $V_{ce,sat}$ as function of scaling factor k under equivalent IE effect condition after adjusted by R_{pf}. The p-collector doping concentration assumed is $1.6\times10^{18}cm^{-3}$, $8.0\times10^{17}cm^{-3}$, and $4.0\times10^{17}cm^{-3}$.

current density 160A/cm^2 and 320A/cm^2, the relation that $dV/dt_{Critical}$ value increases with higher scaling factor k still holds. On the other hand, $dV/dt_{Critical}$ values have been proven to improve in scaled IGBTs even at higher bus voltage 2100V and 2500V in Fig. 12(b). It's supposed that DA is suppressed under higher ambient temperature owing to the lower impact ionization coefficients. Our results in Fig. 12(c) are consistent with this point and demonstrate even greater improvement of dV/dt controllability of scaled IGBTs at higher temperature conditions. Finally, p-collector doping concentration was also modified in simulation to see the difference in Fig. 12(d). At lower doping concentration design of p-collector or faster switching mode IGBT, scaled IGBT reveals further wider controllable dV/dt range during device turn-off. There is enough evidence to assert that scaled IGBT is profitable for higher switching speed applications.

Furthermore, the $dV/dt_{Critical}$ and $E_{off\text{-}VR}$ values are analyzed as function of on-state voltage drop (various p-collector doping concentration) for IGBTs with different scaling factor k in Fig. 13. Please notice that higher doping concentration corresponds to lower $V_{ce,sat}$. It's explicit that with larger scaling factor k, higher $dV/dt_{Critical}$ and lower $E_{off\text{-}VR}$ values can be realized at the same $V_{ce,sat}$ value. In other ways, scaling method in IGBT is able to break through the trade-off relationships between lower on-state voltage drop ($V_{ce,sat}$) and better switching controllability ($dV/dt_{Critical}$), also lower on-state voltage drop ($V_{ce,sat}$) and lower switching power loss ($E_{off\text{-}VR}$). Summarizing the above discussion, it is speculated that $dV/dt_{Critical}$ in scaled IGBTs

may be worsened by higher carrier density at the emitter side by the IE effect, while at same time, $dV/dt_{Critical}$ is improved by better electric field uniformity originating from a smaller dimension of the mesa region. So far, all results under equivalent IE effect condition validate that the superior turn-off dV/dt controllability and also lower switching power loss since the successful suppression of DA in scaled IGBTs.

V. CONCLUSION

After comprehensive analysis based on a new evaluation method, scaled IGBT is believed to benefit from superior dV/dt controllability during turn-off thanks to the suppression of DA. The physical analysis tells us that the prominent improvement of electric field uniformity is capable of mitigating DA in scaled IGBT structure, which is also adequate to compensate for the influence of higher carrier density from stronger IE effect. Finally, with the help of adjustable R_{pf} approach, scaling method in IGBTs is concluded to be able to enjoy lower $V_{ce,sat}$ by stronger IE effect and better turn-off dV/dt controllability, also lower switching power loss simultaneously.

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