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A 65nm Cryogenic CMOS Design and Performance at 4.2K for Quantum State Controller Application

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ABSTRACT A performance evaluation of cryogenic CMOS circuit at liquid-helium temperature (4.2K) is conducted using a standard 65nm bulk CMOS for quantum state controller (QSC) applications. The ON-current (Ion) of the core n/pMOSFET are increased by 25% and 9% with excellent gate modulation (Ion/Ioff=$\sim 10^9$). The cryogenic characteristics of copper interconnects in the back end of the line (BEOL), including line and via resistances, capacitances, and Joule-heating effect (JHE) are accurately assessed. The interconnect and via resistances decrease with temperature due to a reduction of electron-phonon scattering, resulting in resistances that are 75% and 20% lower at 4.2K compared to those at room temperature(RT). No significant change in inter-line capacitance and no severe JHE are observed in the Cu BEOL at 4.2K. The developed cell libraries for Simulation Program with Integrated Circuit Emphasis (SPICE) model and the technology file, which includes RC interconnect parameters, enable precise design of CMOS circuits at 4.2K. This results in a demonstrated +18.3% increase in speed or −16% reduction in power consumption for ring-oscillator (ROSC) at 4.2K, aligning well with the simulation results obtained from the developed model.

INDEX TERMS Cryogenic CMOS, cryogenic BEOL, quantum computing, quantum state controller.

I. INTRODUCTION

To meet increased demand of computing for various applications, there is an increased effort spent in classical and/or alternative computing. Quantum Computers (QCs) operating using qubits, which can be simultaneously in two states, e.g., |0> and |1>, can execute certain algorithms faster than the classical computing [1], [2], [3]. Therefore, a fusion of the classical and quantum computing has great potential for the future of computing. A superconducting transmon is one of the promising qubit candidates for scaled QC systems since the state of the artificial atom can be tailored by RF pulses in the range from 4 to 6 GHz to manipulate their states [4]. To minimize the impact of thermal noise on the operation, the transoms are placed at a few mK in a dilution refrigerator and are controlled by classical electronics connected with long cables from a rack-mounted system at room temperature (RT). Figure 1 show the schematic image of quantum computing system in the refrigerator. It does not appear feasible to provide a control line for every qubit from RT to a 10mK environment for a 10^6 qubits system due to various factors, including RF loss, cross talk, heat load, and mechanical congestion of the wires. These factors would result in an input-output (I/O) bottleneck [5]. To scale up the QCs to millions of qubits, cryogenic electronics, based on complementary metal-oxide-semiconductor (CMOS) technology, may offer a scalable and reliable solution to overcome the I/O bottleneck [6], [7]. However, the smaller cooling power at cryogenic temperature is another bottleneck when the classical electronics is used. Cryogenic qubit state controllers (QSCs) should be operated

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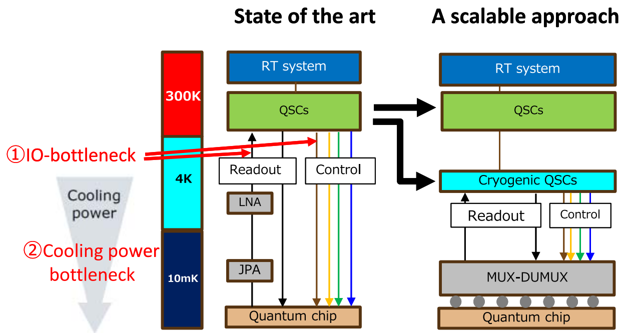

FIGURE 1. Schematic image of the state-of-the-art quantum computing system. Cryogenic quantum state controller is placed at 4K for a scalable approach, where the transoms and QSCs can be connected to each other with low-loss superconducting interconnects.

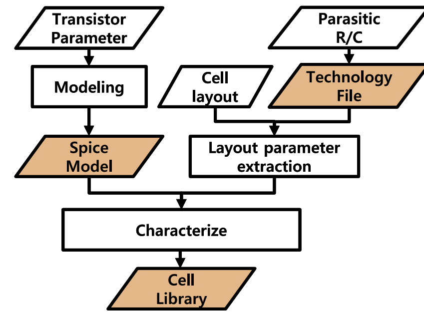

FIGURE 2. Development flow for a cell library of the standard CMOS.

at a low power of a few watts. When we place the QSCs below the superconducting transition temperature of the wiring metal, it is possible to connect the transoms and the QSCs by low-loss superconducting interconnects. This is a potential advantage of the cryogenic control system in the refrigerator.

Historically, a low-temperature circuit was developed for spacecraft applications. Recently, a cryo-CMOS is re-cool since operating it at liquid-nitrogen temperatures improves the performance of high-performance computing (HPC). Therefore, the cryo-CMOS technology is extensively studied [8], [9]. To design the CMOS circuits at cryogenic temperature, the cryogenic MOS transistor model [10] and the cell library have been reported [11]. However, the conventional standard surface potential-based compact model used in Simulation Program with Integrated Circuit Emphasis (SPICE) does not fully support MOS device operations at temperature below 20K. Girish et al. conducted a comprehensive investigation into the existing temperature schemes in these models and concluded that reformulation is necessary for an accurate evaluation of switching speed and leakage from room temperature down to cryogenic temperatures. They proposed new temperature models for charge density, including band tail state carriers, threshold voltage, mobility, and current saturation [12].

Our objective is to provide a straightforward estimation of CMOS circuit performance without the reformulation of the model. Whenever feasible, we have just re-optimized parameters within the existing model to align them with real measurements extracted at 4.2K. In addition to the MOS transistor characteristics, it is necessary to consider back end of the line (BEOL) characteristics that depend on technology nodes and operating temperature. Understanding of BEOL characteristics, such as interconnect and via resistances as well as interline capacitances, remains inadequate at cryogenic temperatures. For dielectrics, a thermal conductivity is known to decrease with temperature. A careful evaluation is required to understand the Joule heating effect (JHE) on BEOL.

The present paper describes the results of an investigation of the cryogenic behavior of CMOSs and interconnects, the objective of which is to characterize the electrical behavior and to provide the simple SPICE model for circuit designers of the QSCs. The preliminary results have been presented by the authors at IEEE international interconnect technology conference (IITC) 2022 [13]. In this article, detailed explanations and new experimental results of cryogenic transistor SPICE models, along with a circuit demonstration of a ring oscillator (ROSC) operation, have been included to facilitate a more in-depth discussion of cryogenic behavior.

II. EXPERIMENTAL SETUPS

A standard 65nm bulk CMOS with 1P9M was used for the evaluation. We fabricated core transistors with channel lengths (Lg) ranging from 0.06μm to 10μm and channel widths (Wg) ranging from 0.24μm to 10μm, and the operating voltage is 1.2 V. For high-voltage (HV) transistors, we prepared Lg ranging from 0.24μm to 10μm and Wg ranging from 0.36μm to 10μm, and the operating voltage is 2.5 V. For BEOL, Cu interconnects from M1 to M7 are evaluated, in which the line widths of the lines are ranging from 0.1 to 4μm and the diameter of the Cu-via is 0.1μm$^{\phi}$ from V1 to V6. There are no special process modifications during fabrication for the cryogenic operation.

Figure 2 shows a development flow of the cell library. The SPICE model is constructed using the parameters of transistors, while the technology file is built based on parasitic measurements of resistance and capacitance of interconnects at liquid-helium temperature (4.2K). For the parameter extractions, ~300 test element groups (TEGs) with the different gate length and the width of transistors are measured at 4.2K. The measurement setup consists of a hollow steel pipe, where the devices under test placed are mounted on ceramic packages and placed at one end, while the other end features the connectors to interface with the instruments at room temperature. The pipe is dipped into a helium barrel.

III. CRYOGENIC BEOL CHARACTERIZATION

First, we evaluate the interconnects and via-connections in BEOL. Figure 3 shows sheet resistances of the lines from

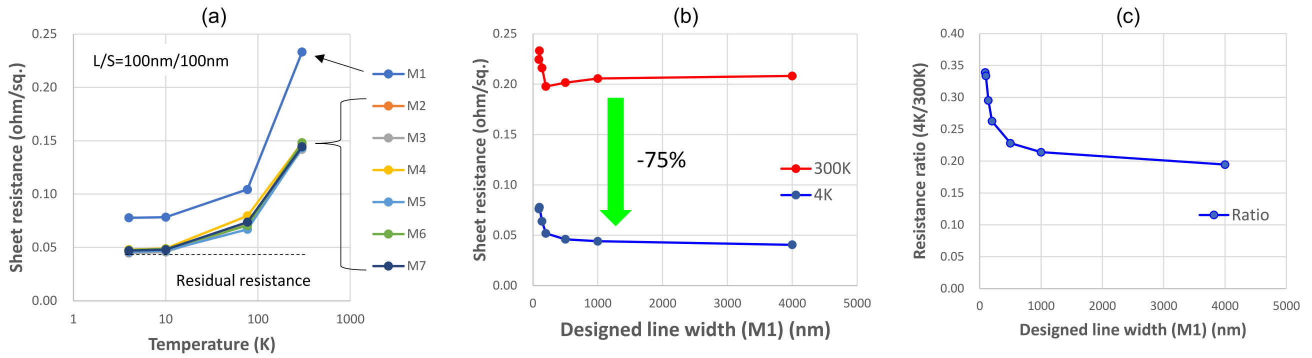

FIGURE 3. **(a) Sheet resistance of Cu interconnects from M1 to M7 with Line/Space= 0.1/0.1 μm as a function of temperature. (b) Sheet resistance of Cu interconnects as a function of line width dependence measured at two different temperatures of 4K and 300K, (c) Resistance ratio of the Cu interconnects as a function of the line width measured at 4K and 300K.**

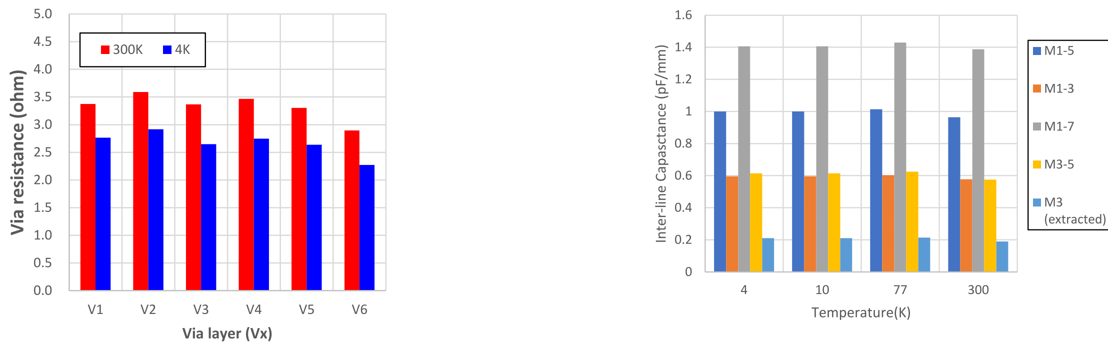

FIGURE 4. **Cu via-resistances per unit measured at 300K and 4K.**

FIGURE 5. **Interline capacitances measured over a range of temperatures from 4K to 300K.**

M1 to M7, (a) as a function of the temperature, (b) as a function of line width, and (c) the ratio of sheet resistance between 4K and RT. The sheet resistances of L/S=0.1/0.1μm line decrease with temperature irrespective of the layers. Typically, 75% reduction is achieved by decreasing phonon-electron scattering, but a residual resistance remains at 4K. The residual resistance originates from impurities in Cu material itself and scattering at grain boundaries and interfaces. A difference between the sheet resistances of M1 and M2 is explained by the smaller line height of M1 (h=120 nm) compared to M2 (h=150 nm), in which the small cross-sectional area of the line enhances the small size effect. A wider line exhibits a larger reduction in resistance at 4K as shown in Fig. 3 (b), because the narrower line has higher residual resistance due to small size effect caused by electron scattering at sidewalls [14], [15]. Figure 4 shows Cu-via resistances from V1 to V6. The via-resistances show ~3.4 Ω at RT and ~2.6 Ω at 4K, respectively, regardless of the layers, and 20% reduction is obtained. The reduction is primarily attributed to a decrease in the resistance of Ta/TaN barriers at the bottom of the vias.

Figure 5 shows the interline (Metal-Oxide-Metal; MOM) capacitances. Here, we prepared four different multi-layered comb patterns for the capacitance evaluation. The M3 interline capacitance is extracted from the experimental data and ~0.2pF/mm is obtained at 4K. Notable, there is no alteration in the interline capacitance value at 4K.

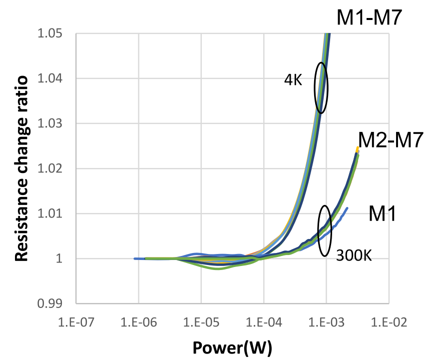

FIGURE 6. **Analysis of Joule heating effect on the interconnects of M1 toM7 layers measured at 4K and 300K.**

Figure 6 shows JHE on Cu interconnects of L/S=0.1/0.1μm (50% data ratio) from M1 to M7. The resistance change ratio is shown as a function of the applied power for the interconnects. When the same voltage is applied to the line, the higher current flows at 4K since the line resistance is lower than that at 300K. Over a range from 0.1mW, the increment in the resistance due to the JHE at 4K is larger than that at 300K, given the decrease in thermal conductivity of dielectrics with temperature [16]. At 1mW, the resistance is 4% higher at 4K. 1mWcorresponds to 15mA at the measured voltage regardless of the layers, where the current is high enough compared to the maximum

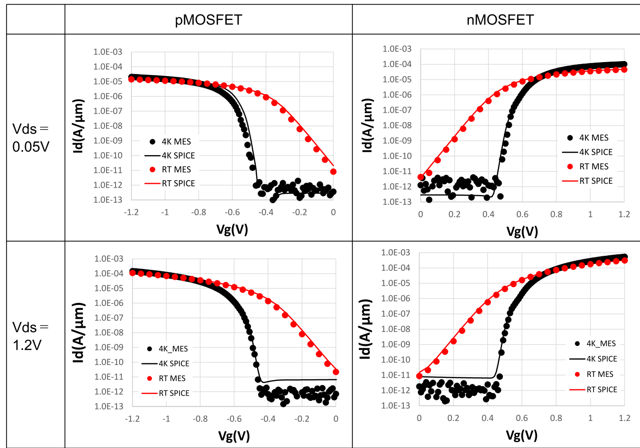

FIGURE 7. Id-Vg characteristics at Vds =0.05 and 1.2V of nMOSFET and pMOSFET measured at 4K and room temperature. Symbols are experimentally measured and solid line is SPICE model.

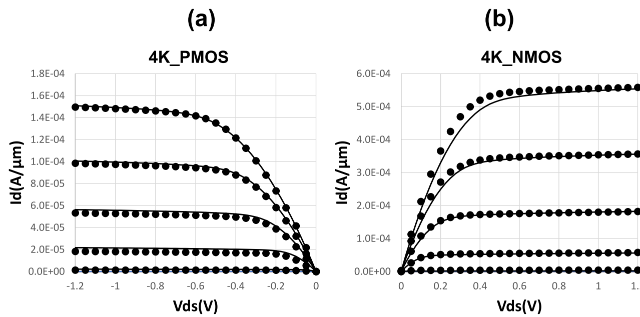

FIGURE 8. Model validation with Id-Vd characteristics for different Vg from 0 to 1.2V with 0.15V step, (a) pMOSFET and (b) nMOSFET measured at 4K. Symbols are experimentally measured and solid line are SPICE models.

allowable current (Imax) in local interconnects. Thus, it is confirmed that there is no critical effect of JHE on interconnect performance at 4K.

IV. CRYO-CMOS SPICE MODEL

Next, we evaluate logic transistors of Lg at the range from 0.06μm to 10μm. We have also extracted parameters for transistors of various size of Wg ranging from 0.4μm to 10μm. For the SPICE model at 4K, BSIM6 (Berkeley Short-channel IGFET Model) [21] is used to fit the experimental data without reformulation. The BSIM6 is in the flexibility to fit data from different technologies and guarantees symmetry around Vds=0. Id-Vg characteristics of the n/pMOSFETs at the temperature of 300K (room temperature (RT)) and 4K are evaluated. Figure 7 shows the Id-Vgs model validation with experimental data of core nMOSFET and core pMOSFET with L/W=1μm/1μm at 4K and RT, respectively. Our model matches the experimental Id–Vgs data for the temperature of 4K with a single global set of parameters. The leakage current below the subthreshold voltage is not fitting well enough for high Vds measurement, but we judged it to be sufficient for this performance estimation. Figure 8 demonstrates that our SPICE model also aligns well with the Id–Vds characteristics for various values of Vg at a temperature of 4 K.

TABLE 1. Summary of FEOL/BEOL characteristics.

	Element	Parameter	Temperature		Relative change
			300K	4K	
FEOL	nFET L/W: 0.06um/1um	V_{th} (V)	0.35	0.46	+110 mV
		I_{dsat} (uA/um)	497	622	+25 %
		I_{off} (uA/um)	1.4×10^{-4}	1.0×10^{-6}	-two orders
		SS (mV/dec)	89	12	-77 mV/dec
		DIBL (mV/V)	105	112	+7mV/V
	pFET L/W: 0.06um/1um	V_{th} (V)	0.31	0.51	+200 mV
		I_{dsat} (uA/um)	269	278	+9 %
		I_{off} (uA/um)	3.3×10^{-4}	2.5×10^{-7}	-three orders
		SS (mV/dec)	89	10	-79 mV/dec
		DIBL (mV/V)	-89	-134	-45mV/V
BEOL	Line L/S: 0.1um/0.1um	R_{line} (Ohm/sq.)	0.2	0.05	-80 %
		Capacitance (pF/mm)	0.2	0.2	-
		Interline leak (A/mm)	$<1\times10^{-13}$	$<1\times10^{-13}$	-
		JHE R change limit power (mW)	0.1	0.1	-
	Via 0.1umΦ	R_{via} (Ohm/unit)	3.5	2.5	-20%
	MIM	MIM (pF)	82	82	-
	eFuse	Fused power (W)	0.14	0.1	-20%

Typical CMOS (core transistor Lg/Wg=0.06/1μm) and BEOL (L/S=0.1/0.1μm, via=0.1μmφ) characteristics are summarized in Table 1. Table 1 is updated from [13]. Carrier mobility in transistors improves at cryogenic temperature [17], but current drive capability only marginally improves by +25%/+9% at 4K as compared to that at RT due to the mitigating effect of the increased threshold voltage Vth, in which the Vth increases by +110mV/+200mV in n/pMOSFET. The increment in Vth at the low temperature is originated from Fermi level shift towards the band edge [18]. Subthreshold swing (SS) calculated at 0.1V lower than Vth has decreased to 12mV/dec in nMOSFET and 10mV/dec in pMOSFET at 4K. Subthreshold leakage (and junction leakage) reduces by 2∼3 order of magnitude at 4K, thus suppressing the static power of CMOS circuits.

We added additional constraints to the design rule for the transistors in the digital cell library. We found that a transient drain current increment due to longer ionization time of freezeout dopant and is more dominant in longer channel MOSFETs (not shown in this article) [19]. Therefore, it is necessary to restrict the range of Lg used for the core transistors. Another issue with a high voltage (HV) transistor used in Input/Output (I/O) is the kink effect, which occurs due to carrier freeze-out and impact ionization at the drain [20]. Further evaluation is necessary for the HV transistors. In this work, we mainly focus on the operation of core transistor circuits.

V. CRYOGENIC CMOS PERFORMANCE

A. SPICE SIMULATION FOR DISTRIBUTED RC LINE

Interconnections are becoming a major concern in integrated circuit at cryogenic temperatures, as the resistance of the wires decreases with temperatures. Using the developed cell library, we simulated the propagation delay in a distributed RC line circuit with the same footprint at both 4K and 300K. Figure 9 shows the distributed RC line model of an inverter-chain used for SPICE simulation. To evaluate the effects of transistors and interconnects on RC propagation delay,

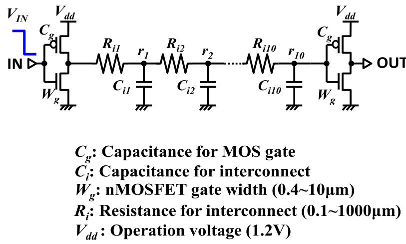

FIGURE 9. Distributed RC line model used in SPICE simulation. The gate width (Wg) and interconnect length are the variable parameters. The delays are compared at the temperatures of 4K and 300K.

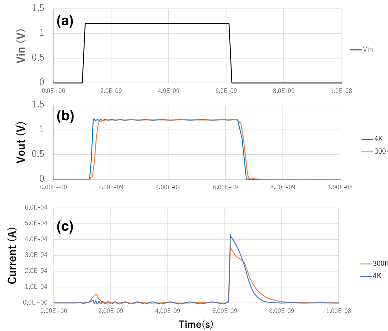

FIGURE 10. Waveforms in SPICE simulation of the model with Wg=1μm, interconnect length=1000μm. (a)Vin, (b)Vout, (c)current at the temperatures of 4K and 300K on Vdd.

Lg is held constant at 0.06μm, while *Wg* and line length of the interconnects are varied with in the ranges of 0.4 to10μm and 0.1 to 1000μm, respectively. Figure 10 shows the waveforms (a)Vin, (b)Vout and (c) current at Vdd in the inverters simulated on SPICE in *Lg*/*Wg*=0.06μm/1μm and interconnect length=1000μm at two different temperatures of 4K and 300K. Here, we defined the delay time as the point where rising edge of Vout reaches Vdd/2. The improvement in the delay is achieved at 4K thanks to the lower resistance of the interconnects and the higher Ion of the transistors. The switching energy is nearly the same due to the consistent capacitance. However, the short-through current during the inverter switching decreases at 4K due to the lower sub-threshold slope (SS) of the transistors. To clearly see the difference of the delay between 4K and RT, fig. 11 shows relative delays of the RC line on SPICE at 4K as compared to those at 300K. The 5∼60% increase in operation speed at 4K, depending on the driver size and the interconnect load. Here, we can classify the relative delay into three groups based on the length of interconnects. Range A (to ∼1μm of the wire length) is the area where transistor drivability is the dominant factor. Range B (3∼20μm) is the area where interconnect capacitance is dominant. Range C (>10μm) is the area where interconnect resistance is dominant. The boundary positions depend on driver size (*Wg*) of the transistors. The boundary in the smaller *Wg* transistor appears from the shorter length of the interconnects. In range A, where transistor resistance is dominant, we confirmed ∼20% faster operation at 4K compared to RT, mainly due to the drain

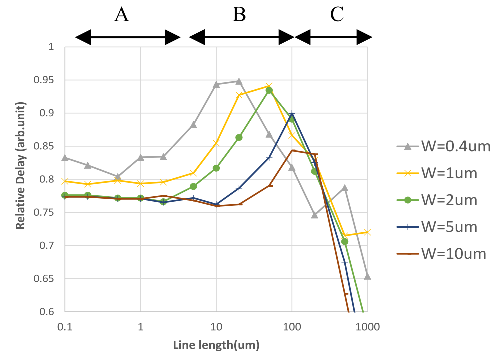

FIGURE 11. Relative delay of the RC line on SPICE at 4K as compared to those at 300K. The improvements of the delay are obtained at 4K, depending on the line length.

current improvement of the transistors. In range B, where interconnect capacitance is dominant, the advantage at 4K decreases to approximately 5% because the interconnect capacitance remains unchanged regardless of temperature. In range C, where interconnect resistance is dominant, we achieved ∼60% increase in operation speed at 4K, primarily attributable to the reduced resistance of the interconnects at this temperature. Lowering the operating temperature is highly effective for circuits with longer wire. Hence, the performance enhancement at 4K is demonstrated by the SPICE simulation of the inverter chain with interconnect loads. This result is valuable for the design of optimal circuits.

B. RING OSCILLATOR OPERATION

To validate the accuracy of the developed cell library, we compared experimental data with simulated results of a ring oscillator (ROSC) operation, in which the operating frequency of the ROSC is measured experimentally at RT and 4.2K. Figure 12 shows the schematic circuit image of the ROSC. The ROSC is a circuit composed of an odd number of NAND gates in a ring, whose output oscillates between two voltage levels, representing true and false. The NAND gates, or inverters, are attached in a chain and the output of the last inverter is fed back into the first. Four stage frequency divider is inserted to measure the ROSC frequency. Figure 13 shows the measurement results. The ROSC operates 18.7% faster with an operating voltage of 1.2V at 4K, as demonstrated and well consistent with the simulated result. When maintaining the same operation speed, the operation voltage at 4K can be reduced by 0.1V (−8.3%), resulting in 16% reduction of operating power. The dynamic power reduction is demonstrated. The static power will also be reduced by the reduction of the sub-threshold leakage current of the transistors (See Fig. 7), depending on the circuit design and the ratio of active transistors. Further evaluation for the actual QSC is desired in future work.

VI. CONCLUSION

The cryo-CMOS performance has been investigated by including BEOL for the first time. The newly developed

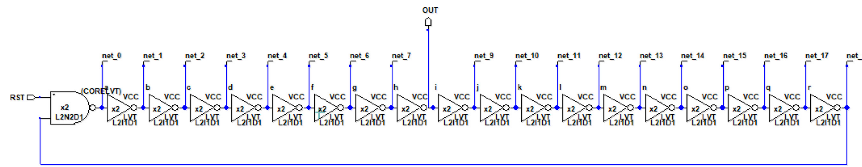

FIGURE 12. Schematic circuit image of the ring oscillator.

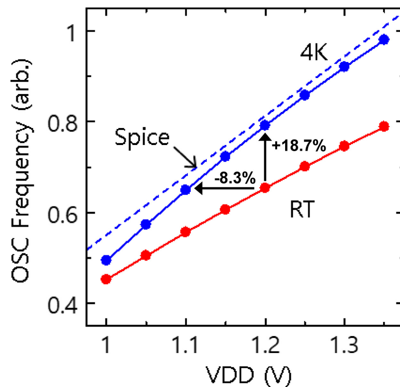

FIGURE 13. Frequency of the ring oscillator as a function of operation voltage at RT and 4K.

4K-cell library including BEOL characteristics realizes the accurate CMOS circuit design at 4K. Incorporating the BEOL characteristics is essential for maximizing the CMOS circuit performance for designing the QSCs.

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REFERENCES

[1] L. K. Grover, "Quantum mechanics helps in searching for a needle in a haystackPhys," *Phys. Rev. Lett.* vol. 79, p. 325, Jul. 1997, doi: 10.1103/PhysRevLett.79.325.

[2] P.W. Shor, "Polynomial-time algorithms for prime factorization and discrete logarithms on a quantum computer," *SIAM J. Comput.* vol. 26, pp. 1484–1509, Oct. 1997, doi: 10.1137/S0097539795293172.

[3] M. H. Yung, J. D. Whitfield, S. Boixo, D. G. Tempel, and A. Aspuru-Guzik, "Introduction to quantum algorithms for physics and chemistry," in *Advances in Chemical Physics*, vol. 154, Hoboken, NJ, USA: Wiley, 2014. [Online]. Available:https://doi.org/10.1002/9781118742631.ch03

[4] Y. Nakamura, Y. A. Pashkin, and J. S. Tsai, "Coherent control of macroscopic quantum states in a single-Cooper-pair box," *Nature* vol. 398, pp. 786–788 Apr. 1999, doi: 10.1038/19718.

[5] D. J. Reilly, "Challenges in scaling-up the control interface of a quantum computer," in *Proc. IEEE Int. Electron Devices Meet. (IEDM)* 2019, pp. 31.7.1–31.7.6, doi: 10.1109/IEDM19573.2019.8993497.

[6] B. Patra et al., "Cryo-CMOS circuits and systems for quantum computing applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, Jan. 2018, doi: 10.1109/JSSC.2017.2737549.

[7] D. J. Frank et al., "A Cryo-CMOS low-power semi-autonomous qubit state controller in 14nm FinFET technology," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2022, pp. 360–362, doi: 10.1109/ISSCC42614.2022.9731538.

[8] H.-L. Chiang et al., "Design technology co-optimization for cold CMOS benefits in advanced technologies" in *Proc. IEEE Int. Electron Devices Meet. (IEDM)*, 2021, pp. 13.2.1–13.2.4, doi: 10.1109/IEDM19574.2021.9720573.

[9] S. S. Parihar, V. M. Van Santen, S. Thomann, G. Pahwa, Y. S. Chauhan, and H. Amrouch, "Cryogenic CMOS for quantum processing: 5-nm FinFET-based SRAM arrays at 10 K," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 8, pp. 3089–3102, Aug. 2023, doi: 10.1109/TCSI.2023.3278351.

[10] A. Beckers, F. Jazaeri, and C. Enz, "Cryogenic MOS transistor model," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3617–3625, Sep. 2018, doi: 10.1109/TED.2018.2854701.

[11] E. Schriek, F. Sebastiano, and E. Charbon, "A Cryo-CMOS digital cell library for quantum computing applications," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 310–313, 2020, doi: 10.1109/LSSC.2020.3017705.

[12] G. Pahwa, P. Kushwaha, A. Dasgupta, S. Salahuddin, and C. Hu, "Compact modeling of temperature effects in FDSOI and FinFET devices down to cryogenic temperatures," *IEEE Trans. Electron Devices*, vol. 68, no. 9, pp. 4223–4230, Sep. 2021, doi: 10.1109/TED.2021.3097971.

[13] K. Okamoto et al., "Cryogenic CMOS performance analysis including BEOL characteristics at 4K for quantum controller application," in *Proc. IEEE Int. Interconnect Technol. Conf.*, 2022, pp. 139–141, doi: 10.1109/IITC52079.2022.9881293.

[14] M. Tada et al., "Improving reliability of copper dual-damascene interconnects by impurity doping and interface strengthening," *IEEE Trans. Electron Devices*, vol. 54, no. 8, pp. 1867–1877, Aug. 2007, doi: 10.1109/TED.2007.901265.

[15] M. Tada et al., "Feasibility study of 45-nm-node scaled-down cu interconnects with molecular-pore-stacking (MPS) SiOCH films," *IEEE Trans. Electron Devices*, vol. 54, no. 4, pp. 797–806, Apr. 2007, doi: 10.1109/TED.2007.892357.

[16] G. D. Cahill, S. K. Watson, and R. O. Pohl, "Lower limit to the thermal conductivity of disordered crystals," *Phys. Rev. B*, vol. 46, p. 6131, Sep. 1992, doi: 10.1103/PhysRevB.46.6131.

[17] H. Oka, T. Inaba, S. Iizuka, H. Asai, K. Kato, and T. Mori, "Effect of conduction band edge states on coulomb-limiting electron mobility in cryogenic MOSFET operation," in *Symp. VLSI Technol. Circuits Tech. Dig.*, 2022, pp. 334–335, doi: 10.1109/VLSITechnologyandCir46769.2022.9830505.

[18] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. New York, NJ, USA: Wiley, 2006.

[19] T. Miyao et al., "Enhanced drain current in transient mode due to long ionization time of shallow impurities at 4K in 65-nm bulk cryo CMOS transistors," in *Proc. Device Res. Conf. (DRC)*, Ohio, USA, 2022, pp. 1–2, doi: 10.1109/DRC55272.2022.9855815.

[20] A. Grill et al., "Reliability and variability of advanced CMOS devices at cryogenic temperature," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, doi: 10.1109/IRPS45951.2020.9128316.

[21] "BSIM-CMG model: BSIM-CMG-GAA 100.0.0beta0_1." Accessed: May 9, 2023. [Online]. Available: http://bsim.berkeley.edu/models/bsimcmg/