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Design and Simulation Optimization of an Ultra-Low Specific On-Resistance LDMOS Device

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ABSTRACT The design of LDMOS (Lateral double diffused metal oxide semiconductor) devices with CFP (Contact field plate) has been of great significance in recent years, according to its advantages of low resistance and high switch efficiency. In this paper, this ultra-low $R_{on,sp}$ (Specific on-resistance) LDMOS device is simulated, designed, and fabricated. The effects on FOM (Figures-of-merits) characters from physical dimensions, including field plate length L, field plate thickness H, and slot contact width W, have been analyzed and discussed. The best device structure is proposed through simulation, and a related fabrication process is introduced correspondingly. Finally, the electrical measurement results show that $R_{on,sp}$ can achieve as low as 6.9m$\Omega\cdot$mm^2 when the source-drain BV(Breakdown voltage) arrives at 34.1V, which is improved by 47.1% compared with conventional devices. Furthermore, the TLP (Transmission line pulse) test results indicate that the device owns an ideal SOA (Safe operation area) from both typical devices (W = 10μm) and very large devices (W = 2mm).

INDEX TERMS Contact field plate (CFP), figures of merits (FOM), lateral double diffusion metal oxide semiconductor (LDMOS), specific on-resistance ($R_{on,sp}$).

I. INTRODUCTION

Recently, BCD (Bipolar-CMOS-DMOS) circuits based on LDMOS (Lateral double diffusion metal oxide semiconductor) devices have been widely applied in PMICs (Power management integrated), IoT (Internet of Things), AI (Artificial intelligence), and automotive owing to its advantages of high speed and easy integration [1], [2], [3]. In the device structure design and process integration of LDMOS, field plate technology is the most critical technology widely used for source-drain BV (Breakdown voltage) improvement [4], [5], [6]. An appropriate field plate structure could produce a uniform distribution of the electric field in the drift region by reducing the surface peak electric field and increasing the lateral electric field, thereby increasing the device's BV.

At present, the field plate commonly used in the IC (Integrated circuit) manufacturing industry are two structures: mini-STI (Shallow trench isolation) field plate and mini-LOCOS (Local oxidation of silicon) field plate [6], [7]. Many new researchers have been published [8], [9], [10], [11], [12], and they focus on optimizing and innovating field plate structures in LDMOS devices. These novel field plate structures indeed bring a significant improvement in device FOM (Figures of merits) performance to a certain degree. However, among all these structures, poly gates have to land on the gate oxide and field plate oxide meanwhile. This inherent feature inevitably causes a higher gate-drain parasitic capacitance C_{GD}, then results in lower switching efficiency and higher $R_{on,sp}$ (Specific on-resistance).

For further improvement, an optimized LDMOS device named CFP (Contact field plate) is introduced [13], [14]. In this structure, gate oxide bias and field oxide bias are separated completely. Thus, it yields a lower $R_{on,sp}$ and higher switch efficiency. However, this novel device's electrical performance and process fabrication are still under continuous study [15], and related published results are

currently insufficient. Therefore, research works on CFP LDMOS devices are still of great practical significance for our semiconductor IC industry.

II. STRUCTURES AND ANALYSIS

A. STRUCTURE DESCRIPTION

Fig. 1(a) illustrates the basic schematic of CFP LDMOS devices and Fig. 1(b) is the conventional schematic for comparison. From bottom to top, there are:

(1) Deep N well ⑦: High energy implant and the high-temperature drive in for device full isolation;

(2) Drift region ⑥;

(3) Body region ⑤;

(4) Drain terminal ④;

(5) Source terminal ③;

(6) Gate terminal ①: include ploy gate ①-①, gate oxide ①-②, and oxide-nitride spacer ①-③ in both sides of poly gate;

(7) Contact field plate ②: consisting of slot contact ②-① and field plate dielectric layer ②-②. The field plate dielectric layer ②-② is composed of a multi-layer of SiO_2, Si_3N_4, and SiO_2. The slot contact ②-① passes through the top SiO_2 layer, then penetrates and lands on the middle Si_3N_4 layer. The authors define field plate length as L, contact width as W, and effective thickness (bottom oxide combined 100Å remaining Si_3N_4 that post etching) as H.

In which, contact field plate terminal ②-① connects with source terminal ③ via the metal layers. Thus, the CFP device is still considered as a four-terminal device.

Fig. 1(c) and (d) illustrate respectively the CFP LDMOS and conventional LDMOS [16], [17] device's static intrinsic capacitances [18], [19], which is consisting of the gate-to-source capacitance C_{GS}, the gate-to-drain capacitance C_{GD} and the drain-to-source capacitance C_{DS}. In which, C_{GS} and C_{GD} are all consisting with oxide capacitance C_{GOX}/C_{FOX} and gate side wall capacitance C_{OF}. The capacitance between the field plate electrode and the drift region is not considered since the field plate electrode connects with the source electrode through the metal lines.

B. CAPACITANCE & SWITCHING EFFICIENCY

Higher dynamic performance is required for LDMOS device design and the transit frequency f_T is linked to C_{GS} and C_{GD} capacitances: [20], [21], [22]

$$f_T = \frac{g_m}{2\pi C_0} \propto \frac{1}{C_{GD} + C_{GS}} \tag{1-1}$$

where, f_T is the transit frequency linked with switching efficiency, g_m the device trans-conductance, relates with low gate oxide voltage region, C_0 the total capacitance, majorly consist of C_{GS} and C_{GD}.

From Fig. 1(c) and (d), the C_{GS} is with same composition from CFP with conventional LDMOS, and the C_{OF} is assumed very low and can be ignored, therefore, here only the C_{GD} related with gate oxide/field plate oxide and parasitic inversion/accumulation charging is discussed.

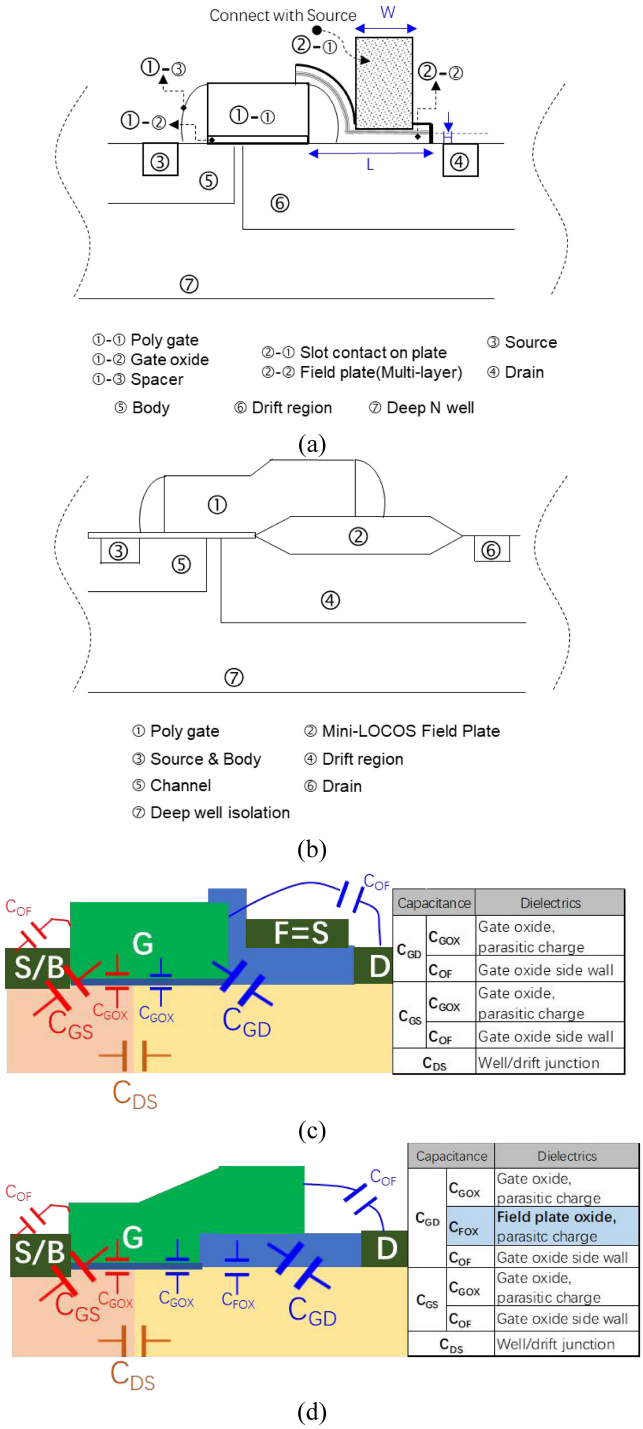


FIGURE 1. Schematic of (a) CFP devices; (b) conventional devices; capacitances of (c) CFP devices; (d) conventional devices, as [22].

LDMOS capacitance model is totally different with conventional MOSFET models. Reference [23], [24] introduced good C_{GD} methodology already for conventional LDMOS.

Fig. 2 (a) illustrates the C_{GD} simulation results versus V_{GS}, respectively from CFP and conventional LDMOS, in which our conventional curves are similar with [23] (grey dash line).

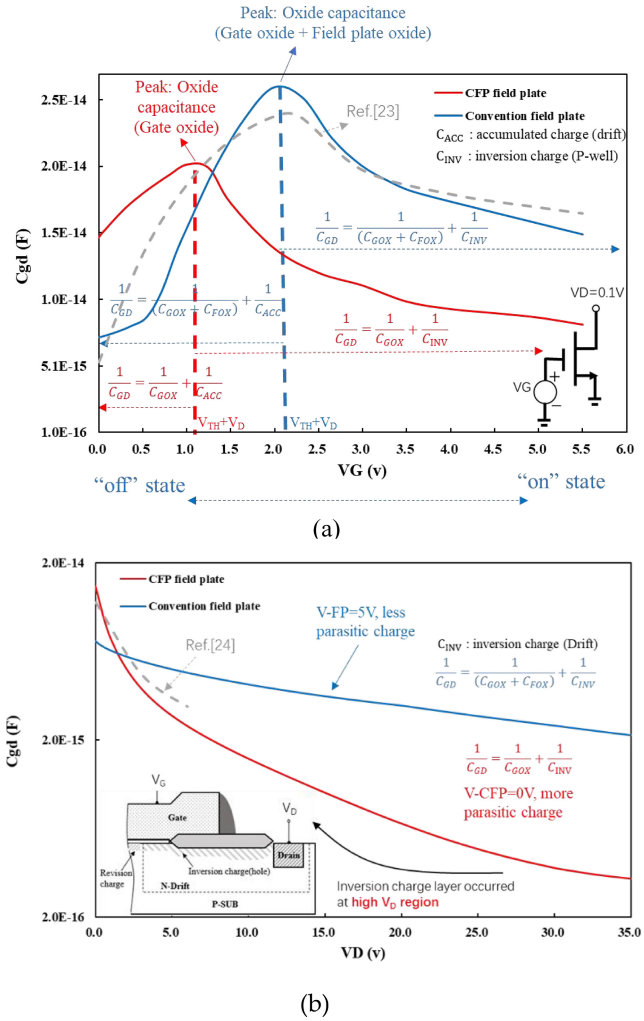


FIGURE 2. C_{GD} **simulation results for CFP and conventional LDMOS respectively (a) versus** V_{GS}**; (b) versus** V_{DS}**.**

The behavior of C_{GD} depends on drift region design parameters, and we simulate the results from CFP LDMOS (red solid line) and conventional device (blue solid line) under the same drift concentration. It is indicated that CFP devices can achieve lower C_{GD} than conventional devices. It is easy to be explained since there is only the gate oxide contribute to the oxide capacitance, while for conventional device, there are both gate oxide and field oxide. For example, at the peak point ($V_{GS} = V_{TH} + V_D$), based on production line experience, the authors give a typical value of gate oxide thickness 150Å, gate oxide length 0.6μm, field oxide thickness 800Å, field oxide length 1.0μm, and correspondingly calculate the CFP LDMOS capacitance C_{CFP} is around 24% lower than conventional LDMOS capacitance $C_{con.}$:

$$C_{CFP} = (1 - 24\%) \times C_{con.} \tag{1-2}$$

Fig. 2(b) illustrates the C_{GD} simulation results versus V_{DS}, respectively from CFP and conventional LDMOS. It is indicated that CFP device also can achieve lower C_{GD} under very high drain voltage. that is due to more parasitic charge under field plate when contact field plate forced 0V instead of 5V.

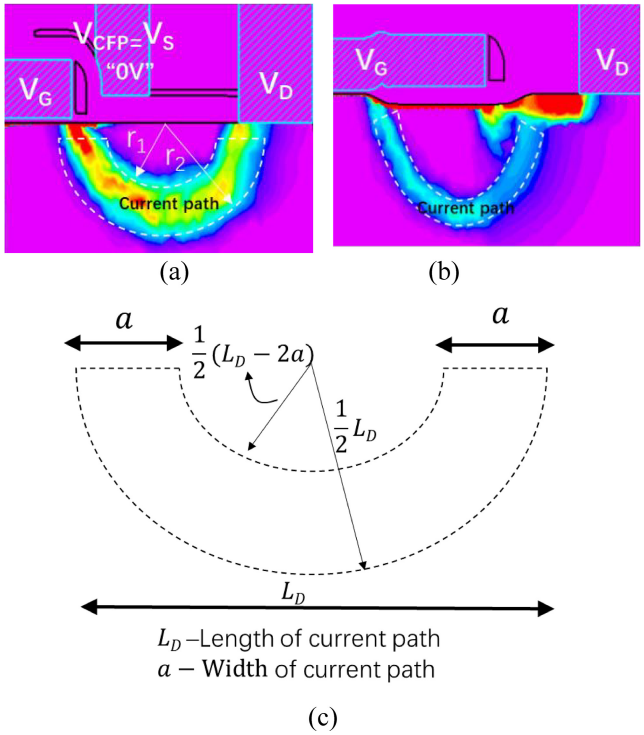


FIGURE 3. **Current path in CFP LDMOS (a) simulation from CFP LDMOS; (b) simulation from conventional LDMOS; (c) ideal ring type model.**

Of course, LDMOS capacitance is very complex, and in our simulation, the junction capacitance, gate sidewall capacitance, etc., are not considered. Meanwhile, usually CFP LDMOS size (gate length, drift length, field plate thickness, etc.) is lower that of conventional LDMOS, so the results in Fig. 2 cannot be taken as an accurate model. However, for the qualitative evaluation, lower C_{GD} and high switching efficiency is a confirmed result.

C. $R_{ON,SP}$ – BV FOM CHARACTERS

FOM(Figures-of-merits) character relating the BV and $R_{\text{on,sp}}$ is well-known for LDMOS device. Baliga introduced a very practical formula in 1989, called Baliga's formula: [25]

$$R_{\text{on,sp}} = \frac{4BV^2}{\varepsilon \mu_n E_C^{s\,3}}, \tag{2-1}$$

where, ε is the dielectric constant of silicon, μ_n the electron mobility, E_C^s silicon surface breakdown voltage.

In Baliga's law (2-1), the current path is considered a linear shape straight along with a silicon surface. However, as shown in Fig. 3(a), in the CFP device, when the CFP terminal connected with source $V_{CFP} = 0V$, and force high drain bias V_{DS} close to BV, the extra "0" potential depletion point enhance the width of the drift depletion region and the current path is not linear shape but likes a ring type. For comparison, Fig. 3(b), illustrates the current path from a

conventional device with the same drift/body concentration. It lacks the extra "0" potential depletion point due to $V_{FP} = V_{GS}$, and thus, not a large current width can be acquired correspondingly.

As shown in Fig. 3(b), we consider the current path as an ideal ring shape and define the length of the current path length as L_D and the width of the current path as a, respectively. Using a similar methodology as [26], the specific on-resistance can be expressed as:

$$R_{\text{on,sp}} = R_{DS} \times HP = \frac{1}{q\mu_n N_D} \frac{1}{\int_{L_D-2a}^{L_D} \frac{1}{\pi r} dr} \times 2L_D = \frac{1}{q\mu_n N_D} \frac{2\pi L_D}{ln\left(\frac{L_D}{L_D-2a}\right)}, \quad (2\text{-}2)$$

where, R_{DS} is the drift region resistance; HP the half-pitch of device; q, N_{D} respectively elementary charge, and drift doping concentration.

Different with the [26], N_{D} is still considered as uniform and can be expressed as

$$N_D = \frac{\varepsilon_s E_C^{s\,2}}{2qBV} \quad (2\text{-}3)$$

And BV is determined by the length of current path L_D:

$$BV = \pi L_D E_C^s \quad (2\text{-}4)$$

Thus,

$$R_{\text{on,sp}} = \frac{1}{\ln\left(\frac{L_D}{L_D-2a}\right)} \times \frac{4BV^2}{\varepsilon\mu_n E_C^{s\,3}} \quad (2\text{-}5)$$

That is, the FOM factor:

$$\frac{BV^2}{R_{\text{on,sp}}} = \frac{1}{4}\varepsilon\mu_n E_C^{s\,3} \times \ln\left(\frac{L_D}{L_{D-2a}}\right) = M \times \frac{1}{4}\varepsilon\mu_n E_C^{s\,3} \quad (2\text{-}6)$$

where

$$M = \ln\left(\frac{1}{1-\frac{2a}{L_D}}\right),$$

where M is defined as a modulator factor. It is determined by the current length L_D and the current width a, and a larger depletion region (proportional to L_D) or a higher a value will yield a better (higher) factor M.

From the comparison between Fig. 3(a) and (b), the CFP device can achieve a larger current path a due to extra "0" penitential depletion under the field plate. It could be a mechanism for better FOM characters from CFP devices, and detailed discussions will be introduced in the following simulation and measurement curves.

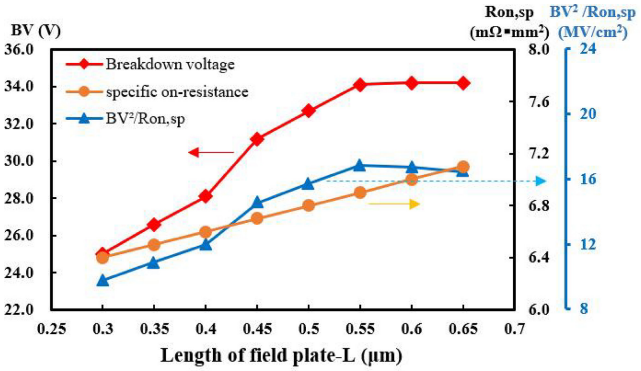
III. FIELD PLATE L/W/H EFFECTS AND DISCUSSION

A. SIMULATION MODEL

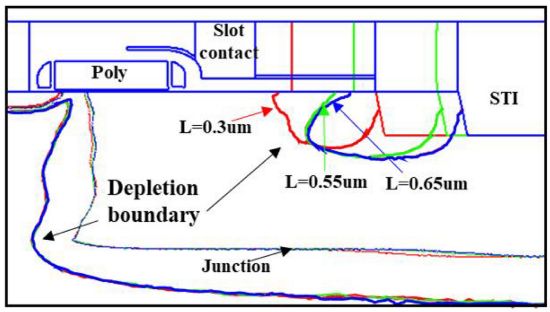
TCAD (Technology computer-aided design) simulation has already played an increasingly significant role in the LDMOS device structure designs [27], [28]. For a CFP device, modulation factor M is strongly related to the device's physical dimension, including field plate length L, effective field plate thickness H, and slot field plate contact width W.

As known, FOM performance is strongly correlated with drift concentration and body concentration. To evaluate the physical size effects of the CFP, the authors fix drift implant P, $2 \times 10^{12}\text{cm}^{-2}$, p-body implant B, $6 \times 10^{13}\text{cm}^{-2}$, and use the Sivaco software 2-D model for TCAD simulation.

For detail, at "on-state", we force gate/drain bias $V_{\text{GS}} = V_{\text{DS}} = 5V$, ground source, and body $V_{\text{CFP}} = V_{\text{S}} = V_{\text{B}} = 0$. At "off-state", ground source/body/gate, $V_{\text{CFP}} = V_{\text{S}} = V_{\text{B}} = V_{GS} = 0$, force drain bias as high as the breakdown voltage. And the $R_{\text{on,sp}}$ is calculated by measuring the linear current I_{dlin} of the device, $R_{\text{on,sp}} = 0.1/(I_{dlin} \times W_{\text{device}} \times L_{\text{device}})$, 0.1 is the drain voltage for linear current I_{dlin} measurement.



(a)



(b)

FIGURE 4. *L* effects (a) on FOM; (b) on depletion region.

B. FIELD PLATE LENGTH-L EFFECTS

Fig. 4 (a) illustrates the effect of field plate length L on FOM characters. As the L increase, the $R_{\text{on,sp}}$ increases lineally, that is easily to be understand due to the current path increase. When L is small (e.g., $L < 0.55\mu\text{m}$), the BV increase as well, that is because of the increase of L_D, as illustrated in formula (2-4). However, when $L > 0.55\mu\text{m}$, the decrease for both BV and FOM factor $BV^2/R_{\text{on,sp}}$ is observed.

To understand the degradation, the depletion region is illustrated in Fig. 4(b). It can be seen when L increase from $0.3\mu\text{m}$ to $0.55\mu\text{m}$, the depletion region increase obviously, while the depletion boundary keeps nearly no change from

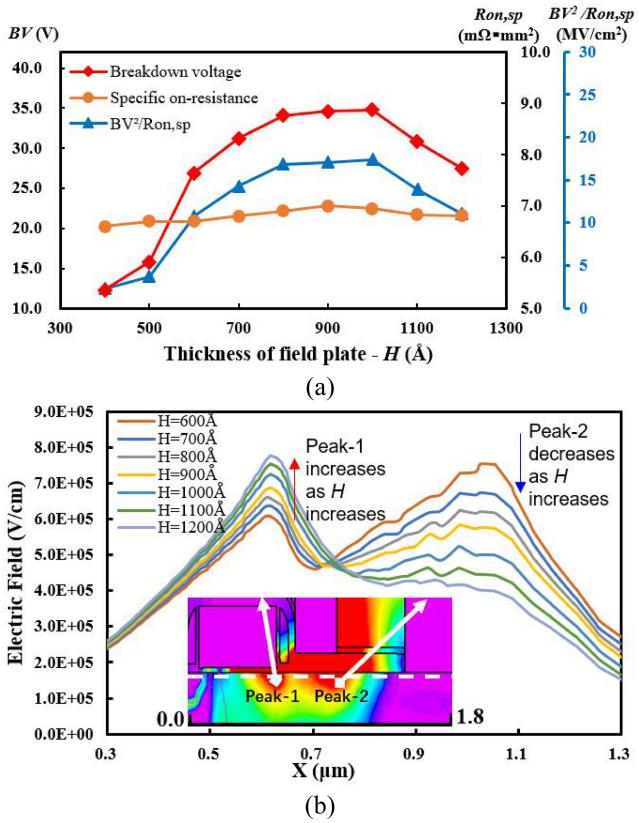


FIGURE 5. *H* effects (a) on FOM; (b) on electric field distribution.

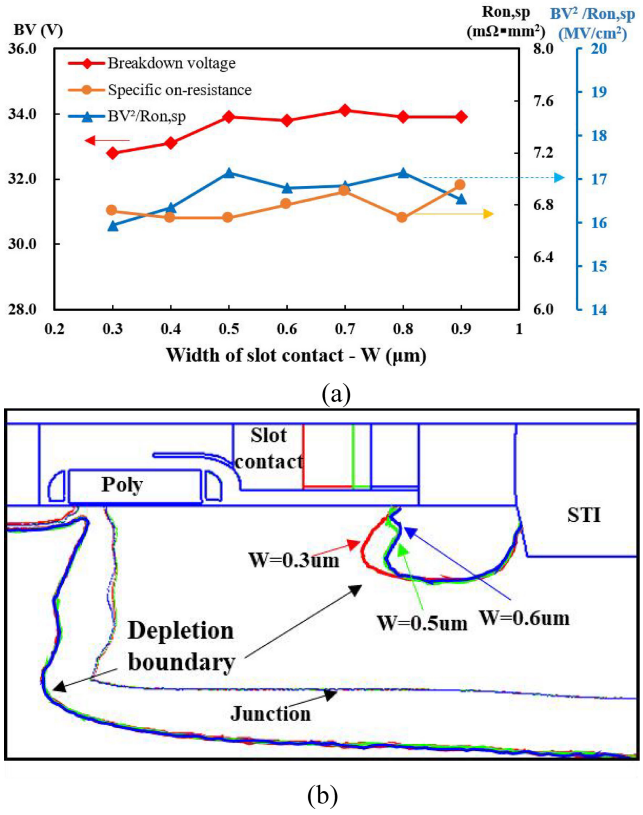


FIGURE 6. *W* effects (a) on FOM; (b) on depletion region.

$L = 0.55\mu m$ to $L = 0.65\mu m$. Since the current path length L_D, which is discussed in Section II-C, is proportional to the depletion region, the result consists of equation (2-6). The reason for BV limitation at $L = 0.55\mu m$ is due to depletion region limitation, which is considered related to drift/body concentration, and another possible reason is that the current path length L_D is not circular again at higher drift region.

C. FIELD PLATE THICKNESS H EFFECTS

Fig. 5 (a) illustrates the effects of field plate thickness H on FOM characters. Where the H is effective field plate thickness, that can be considered as equal to bottom SiO_2 thickness, as shown in Fig. 1(a) blue marks.

As the H increase, the $R_{on,sp}$ nearly no increases, that is easily to be understand according to current path L_D and current width a should be slightly changed. The BV appears a trend of increasing first and then decreasing (e.g., $H > 900$Å), and the FOM factor degradation occurs correspondingly.

To understand the degradation of BV, electric field distribution is illustrated in Fig. 5(b). The electric field distribution is modulated while the current path keeps a ring shape. There are two electric field peaks (peak means Silicon surface breakdown point). Peak-1 is at the poly gate edge close to CFP, and Peak-2 is at the CFP edge towards to the drain terminal. At $H < 900$Å, when H increases, peak-2 decreases. This is the reason why BV increased. At $H > 900$Å, when H increases, the peak-1 increases obviously, and it becomes to dominate the degradation of BV. The electric field peak modulation is assumed to be induced by the lower capability of modulation under higher CFP oxide thickness.

D. CONTACT WIDTH W EFFECTS

Fig. 6 (a) illustrates the effect of field plate contact width W on FOM characters. As the W increase, both the $R_{on,sp}$ and BV increases slightly, possible reason is L_D and a introduced formula (2-5), (2-6) are majorly limited by field plate length L. To indicate it, Fig. 6(b) illustrates the depletion region variations. It can be seen nearly the same depletion boundary is acquired at variable contact width W. It indicates the field plate oxide dominated the modulation on the drift region instead of the slot contact. This observation could bring us the probability of other shapes field plat contact design, such as square shape contacts, rectangle shape contacts, tomatoes on sticks shape contacts, etc.

Finally, from the simulation results, for the fixed doping condition (drift: P, $2 \times 10^{12} cm^{-2}$; p-body: B, $6 \times 10^{13} cm^{-2}$), the best device physical size is proposed, as shown in Table 1. The best dimension could have some changes concerning variations in drift region length, doping, and thickness.

TABLE 1. Best physical size and doping concentration of device (under concentration condition: drift, P, 2 × $10^{12}cm^{-2}$; p-body, B, 6 × $10^{13}cm^{-2}$).

Physical structure	Best	Electrical results
Field plate length - L	0.5 ~ 0.6μm	FOM ($BV^2/R_{on,sp}$) =17.25 MW/cm^2
Field plate thickness- H	800 ~ 1000Å	$R_{on,sp}$ = 6.9 mΩ ·mm^2,
Slot contact width-W	0.3 ~ 0.5 μm	BV = 34.5V

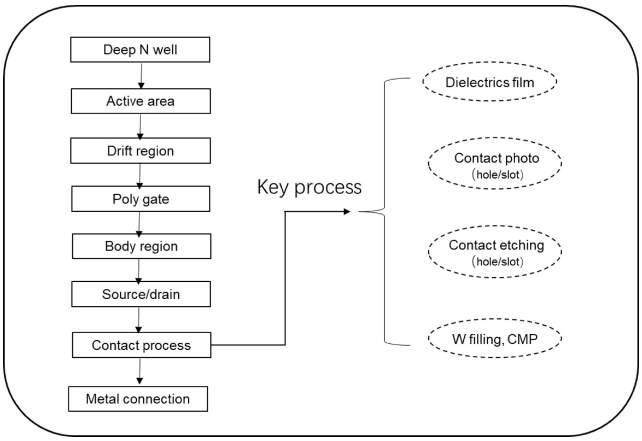


FIGURE 7. Brief process flow and key process.

IV. PROCESS AND ELECTRICAL RESULTS

A. PROCESS FLOW

Relying on the most advanced 12-inch IC production line in (CanSemi semiconductor corp.), series of CFP LDMOS devices have been produced. Fig. 7 is the brief process flow and CFP contact key process modules:

① Deep N well; ② Active area; ③ Drift region; N-concentration, high resistance region for electric field reduction [29]; ④ Poly gate; ⑤ Body region, P type implant works as channel [30], ⑥ Source/drain; ⑦ Contact process and ⑧ Metal connection.

The contact process is the most critical and most challenging process step due to the demands of both hole-type contacts and slot-type contacts should be processed same time. The authors divide it into four process modules:

Dielectrics film: Sandwich films SiO_2-Si_3N_4-SiO_2 are applied. The bottom SiO_2 works as field plate capacitor dielectrics, and its thickness can be considered as effective thickness H, illustrated in Fig. 1(a) in blue marks. The middle Si_3N_4 film is a stop layer for dry etching, and the top SiO_2 a cap layer, respectively. The slot field plate contact passes through the top SiO_2 and then lands on the Si_3N_4 film, keeping around 100Å Si_3N_4 film remaining for the process margin.

Contact photo: Both circular hole contacts and slot contacts are required, and the layout diagram of the device is shown in Figure 8.

Contact etching: It is apparent in the generation of the polymer during the dry plasma etching process, and the polymer is a good material for the hole pattern sidewall protection during dry RF (Radio frequency) etching. However, an excessive polymer can easily lead to self-stopping during slot contact etching. It is known as "etch stop" [31]. Therefore, in the etching recipe, we adjusted the etching bias power and reduced the flow ratio of carbon-based gas, thereby reducing the polymer generation during the etching process and preventing the etching from self-stopping effectively [32].

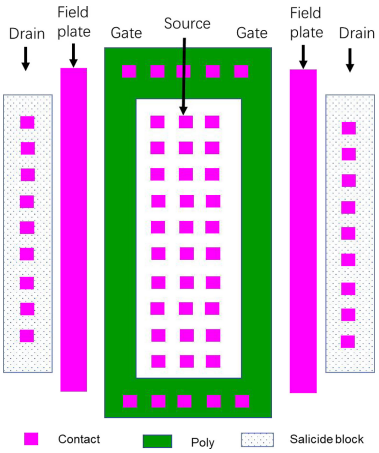


FIGURE 8. Layout diagram of LDMOS devices with CFP.

W filling, CMP(Chemical mechanical polar): Additional amount of tungsten metal deposition is required for the enlarged slot contact pattern.

Finally, perfect SEM(Scanning electron microscope) images of the top view of the contact are shown in Fig. 9(a), including both single-hole type contacts, array-type contacts, and slot-type field plate contacts with different sizes. The TEM (Transmission electron microscope) cross-section profile, alone X direction of the device structure, also is produced. Except for perfect profiles, normal contacts (such as source contacts) landed on the silicon surface well, and field plate contacts land on the middle Si_3N_4 film well, as shown in Fig. 9(b).

B. FOM RESULTS

Wafer level electrical parameters were tested with Agilent B1500 tools.

Fig. 10 illustrates the FOM ($R_{on,sp} - BV$) curves. The two blue lines are Baliga's formula from [25] and [26] conventional devices, respectively. [26] Baliga's curve seems high than that of [25], but the author didn't give out explanations. The green line is this work, and the red line is conventional devices fabricated in our same production lines. The grey line is [7], [33], [34], [35] devices with conventional field plates as well, these data is at similar level, and we put them together into one group.

It can be seen that the CFP devices can achieve much better FOM performance. Taking 16V devices as an example, the specific on-resistance $R_{sp,on}$ can be achieved as low as 6.9 $m\Omega{\cdot}mm^2$ when the source-drain breakdown voltage BV

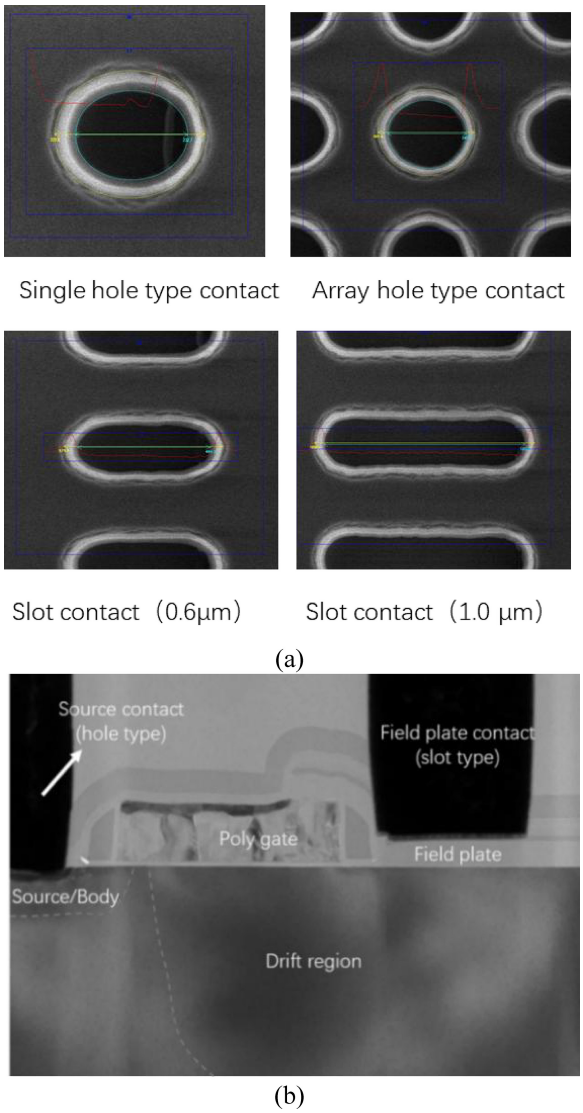


FIGURE 9. Physical results (a) SEM top view of contacts; (b) TEM cross section (along X direction).

arrives at 34.1V, which is nearly 47.1% improved compared with conventional devices.

What is more, the slope of the CFP FOM curve is not the same as Baliga's line, and it tends to be closer to the ideal Baliga's value at a higher BV region. It is consistent with the improvement of the modulator factor M (formula (2-6), in Section II-C), which is related to the increase of current path length L_D. However, there is a "jump" point away from Baliga's line at around $BV = 40$V. A possible reason the current path is not "circular type" again is due to depletion region limitation at the very long drift region. The behavior of the "jump" point indicates that CFP is not suitable for high BV (such as > 40V) applications so far.

C. TLP-SOA RESULTS

Fig. 11(a) and (b) illustrate the TLP [36] (Transmission line pulse)-SOA (Safe operation area) curves, and it is a good indication of the CFP device's robustness.

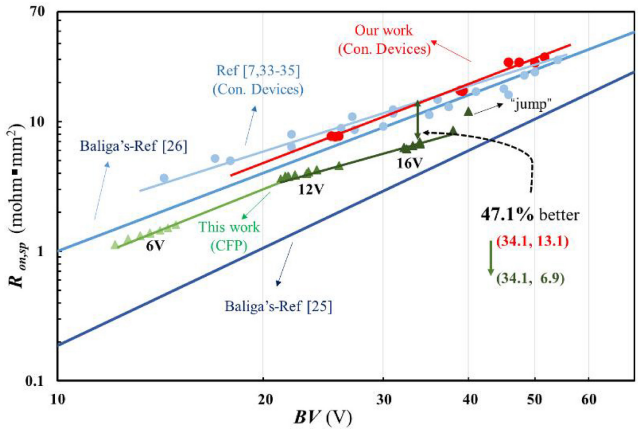


FIGURE 10. FOM curves with log-scale.

TABLE 2. TLP-SOA test environment.

Test setting	Conditions
V_S (V_{CFP})	Ground
V_B	Ground
V_{GS}	0V ~ 6V (>1.1 x V_{DD})
V_{DS}	Pulse, 0V ~ BV
External C (10nF)	10nF
Pulse width	100ns
Rise time	10ns

SOA curves are measured with the ES620 pulse generation tools, and the TLP test environment is described in Table 2.

Fig. 11(a) illustrates the TLP-SOA results of the 16V typical device with channel width W=10μm, and the device can achieve a similar ideal SOA region published in [10] and [36].

More comprehensively, Fig. 11(b) illustrates TLP-SOA results from a very large device with channel width W = 2mm. The design of a very large device is a good monitor for the quality of gate oxide and field plate oxide, and it can indicate the process and device robustness better. The results also show an ideal TLP-SOA performance.

V. CONCLUSION

The device's structure analysis indicates that the CFP LDMOS owns better switching efficiency due to its lower C_{GD} contributed by the full separation for poly gate and field plate oxide. Also, a ring shape current path model is built, and a modulated Baliga's formula is introduced, which can indicate the CFP device's advantage of better FOM performance.

Through the CFP device's TCAD simulation on its physical dimensions, including field plate length L, field plate thickness H, and slot contact width W, an ideal device's physical size is proposed. At the same time, L, H, and W effects on FOM characters are discussed.

Relying on the advanced 12-inch IC production line, a series of CFP devices have been fabricated and tested. The process is indicated by the SEM and TEM images. The FOM curves show that CFP device indeed yields much

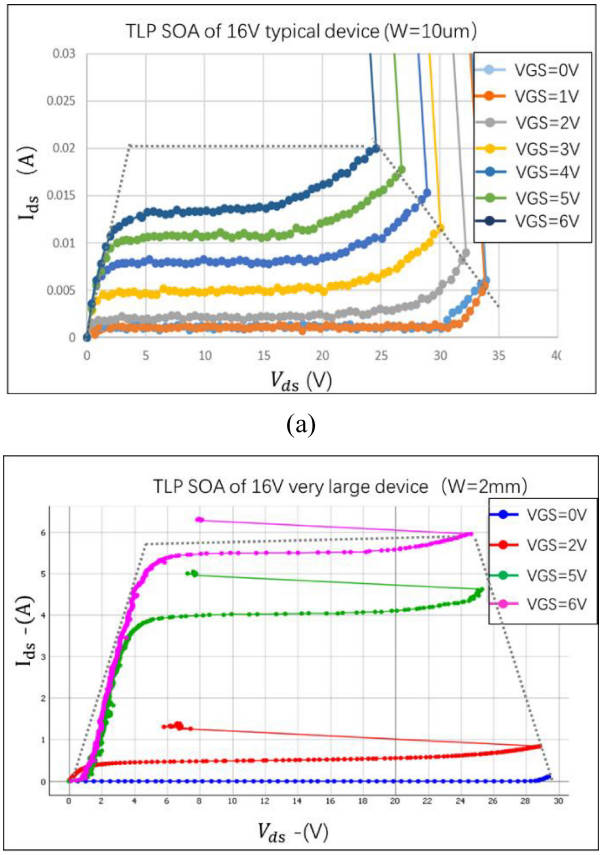


FIGURE 11. The TLP-SOA test results (a) from typical device (W = 10μm); (b) from very large device (W = 2mm).

better performance than conventional devices. The specific on-resistance $R_{sp,on}$ achieves as low as 6.9 $m\Omega{\cdot}mm^2$ when BV arrives at 34.1V, which is nearly 47.1% improved. Furthermore, ideal TLP- SOA curves are acquired from both typical device W = 10μm and very large device W = 2mm, which is evidence of the device's robustness as well.

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