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An a-IGZO TFT-Based AMOLED Pixel Circuit Employing Stable Mobility Compensation Suppressing Degradation of Detected V_{TH}

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ABSTRACT In this paper, we propose a new active-matrix organic light-emitting diode (AMOLED) pixel circuit using amorphous indium-gallium-zinc oxide (a-IGZO) thin film transistors (TFTs). The proposed pixel circuit consists of seven TFTs and two capacitors, compensating for both threshold voltage (V_{TH}) and mobility variations. The simulation results show that the proposed pixel circuit can successfully compensate for mobility variation. Also, the mobility compensation stage positively affects a significant V_{TH} fluctuation. The proposed circuit is fabricated within an area of 19.95 μm $\times$ 39.9 μm that can achieve 635 pixels per inch (PPI), and the experimental results show relatively consistent current levels even under severe TFT variations.

INDEX TERMS a-IGZO, TFT, pixel circuit, V_{TH}, mobility, compensation, high-PPI.

I. INTRODUCTION

The organic light-emitting diodes (OLEDs) have been widely used in various displays owing to their outstanding characteristics, including a wide viewing angle, high contrast ratio, and fast response time [1], [2], [3], [4], [5], [6]. Typically, OLEDs are driven by current, which is supplied by thin-film transistors (TFTs). Among various TFT technologies, amorphous indium-gallium-zinc oxide (a-IGZO) TFTs have gained significant attention due to their extremely low off-current, decent mobility, high on-off ratio, and excellent fabrication uniformity with low-temperature processes [7], [8], [9], [10], [11]. Consequently, a-IGZO TFTs have already been successfully employed in large-sized OLED displays, and are also considered as a promising candidate for mobile OLED displays [12].

However, the electrical characteristics of a-IGZO TFTs can be influenced by process fluctuations and undesired changes resulting from the positive bias temperature stress (PBTS) during operation [13], [14]. Such variations can cause a significant deterioration in image quality in OLED displays, as the TFTs may no longer supply the intended data current to the OLEDs. Therefore, compensating for these variations is essential to meet the demand for a high-quality display.

Decades of extensive research have introduced various compensation methods [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29]. These methods can be broadly categorized into internal and external compensations, and mobile displays typically adopt internal compensation methods that detect threshold voltage (V_{TH}) information within each pixel circuit. While numerous pixel circuits have been proposed, most focus solely on compensating for V_{TH} variation, with only a few addressing mobility compensations.

In this paper, we propose a new pixel circuit based on a-IGZO TFTs. The proposed circuit consists of seven TFTs and two capacitors, and capable of compensating for both V_{TH} and mobility variations. We simulate the accuracy of V_{TH} and mobility compensation with consideration of variations in the fabrication process through HSPICE. Additionally, we experimentally verify the operation of the proposed circuit is by fabricating circuits within a compact area measuring less than 19.95 μm $\times$ 39.9 μm. We measured the current of three

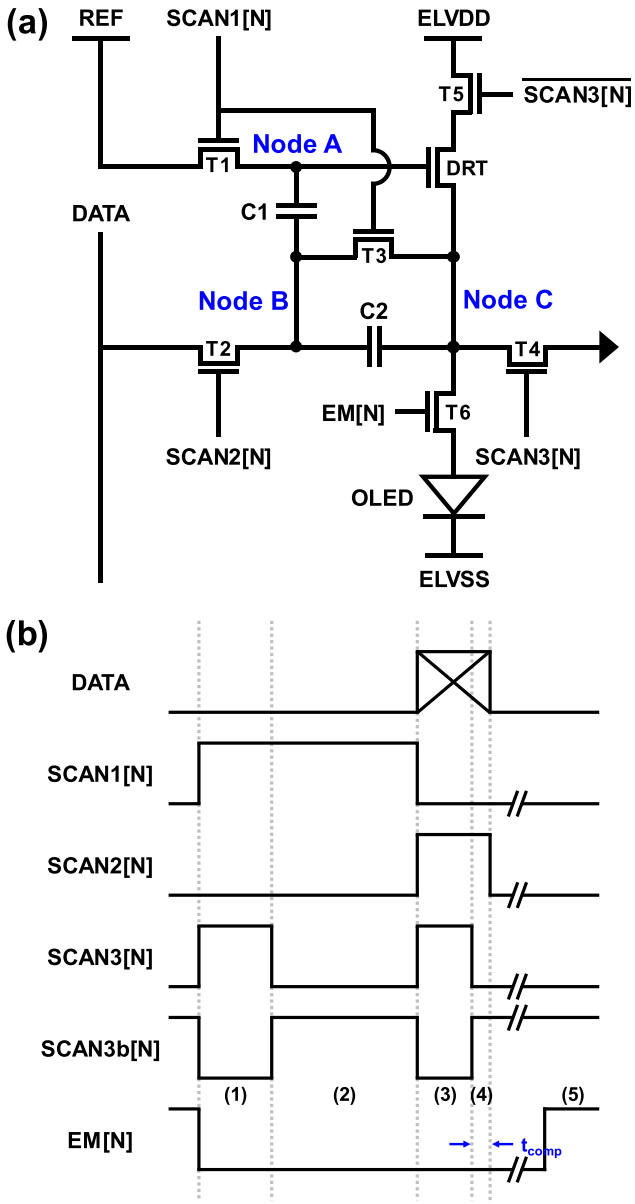

FIGURE 1. (a) Proposed 7T2C AMOLED pixel circuit structure, and (b) its signal timing diagram.

pixel circuits, and the results demonstrate high uniformity. The combined results from our simulation and experiment indicate that out proposed pixel circuit can effectively supply stable and uniform current, even under variations in V_{TH} and mobility.

II. PROPOSED PIXEL CIRCUIT

Fig. 1 shows the proposed pixel circuit structure and its signal timing diagram. The proposed pixel circuit consists of six switching TFTs (T1-T6), one driving TFT (DRT), and two storage capacitors, C1 and C2. The proposed circuit operates in five stages: (1) reset, (2) V_{TH} compensation, (3) data input, (4) mobility compensation, and (5) OLED emission. The detailed operation principles are described as follows:

(1) Reset stage: SCAN1[N] and SCAN3[N] signals are set to a high level, whereas SCAN2[N], SCAN3b[N] and EM[N] signals are set to a low level. All TFTs except T2, T5 and T6 are turned on, and the voltage of nodes A, B, and C is initialized to V_{REF}, 0 V, and 0 V, respectively. As SCAN3b[N] and SCAN3[N] share the same timing but differ only in the high/low level state, we will only mention the SCAN3[N] signal in the subsequent descriptions.

(2) V_{TH} compensation stage: SCAN3[N] signal is set to a low level. T4 is turned off and T5 is turned on, so the DRT current starts charging C1. Then, the voltage of nodes B and C increases equally until the DRT is turned off, while the voltage of node A is kept at V_{REF}. At the end of this stage, the voltage of nodes B and C increases to V_{REF} - $V_{TH,DRT}$, where $V_{TH,DRT}$ refers to the threshold voltage of DRT.

(3) Data input stage: SCAN1[N] signal is set to a low level, while SCAN2[N] and SCAN3[N] signals are set to a high level. T1, T3 and T5 are turned off, whereas T2 and T4 are turned on. Then, the voltage of nodes B and C is set to V_{DATA} and 0 V, respectively, and C2 stores V_{DATA}. Since C1 already stores $V_{TH,DRT}$ after the previous stage, the voltage of node A is increased to $V_{TH,DRT} + V_{DATA}$.

(4) Mobility compensation stage: After a data input stage, SCAN2[N] signal is still maintained at a high level for a short time, while SCAN3[N] signal is set to a low level. Then, the DRT current additionally charges C2 for a moment. As a result, the C2 voltage drops proportionally to the charging time and the DRT current. The DRT current in this stage is a function of both V_{DATA} and mobility, so the decreased C2 voltage can be expressed as V_{DATA} - $\Delta V(t_{comp}, \mu_{DRT}, V_{DATA})$, where μ_{DRT} refers to the mobility of DRT and t_{comp} refers to the duration of the mobility compensation stage.

The reduced voltage during the mobility compensation stage can be expressed as a specific equation. If we express the voltage of node C as $V_C(t)$, the change of $V_C(t)$ can be described by the following equation:

$$I_C(t) = C2 \times (dV_C(t)/dt), \tag{1}$$

where $V_C(0) = 0$ V. Here, $I_C(t)$ is equivalent to the DRT current, as the DRT current charges C2 during this stage. Then, $I_C(t)$ can be expressed by the following equation:

$$I_C(t) = k \times \left(V_{GS,DRT}(t) - V_{TH,DRT}\right)^2, \tag{2}$$

where k is $0.5\mu_n C_{ox}$(W/L). Since C1 stores $V_{TH,DRT}$, and C2 stores $V_{DATA} - V_C(t)$, the $V_{GS,DRT}(t)$ is $V_{TH,DRT} + V_{DATA} - V_C(t)$. Thus, we can derive the following differential equation from equations (1) and (2):

$$k \times (V_{DATA} - V_C(t))^2 = C2 \times (dV_C(t)/dt), \tag{3}$$

$$\int_0^t k dt = \int_0^t \frac{C2 \times (dV_C(t)/dt)}{(V_{DATA} - V_C(t))^2} dt \tag{4}$$

and we can obtain the equation for $V_C(t)$ as follows, by solving the equation (4):

$$V_C(t) = \frac{V_{DATA} \times kt}{kt + \frac{C2}{V_{DATA}}}. \tag{5}$$

The equation (4) clearly indicates that $V_C(t)$ depends on the mobility compensation time, mobility, and V_{DATA}. Therefore, the reduced voltage during the mobility compensation stage can be expressed as a function of those factors, $\Delta V(t_{comp}, \mu_{DRT}, V_{DATA})$. This approach compensates for the mobility variation without affecting the V_{TH} compensation accuracy, because the voltage of C1 remains unchanged as $V_{TH,DRT}$ while only the voltage of C2 is reduced during the mobility compensation stage. When the mobility compensation is completed, SCAN2[N] signal is set to a low level and all TFTs are turned off. At this point, the voltage of node C increases to ELVDD as DRT acts as a switch

(5) OLED emission stage: EM[N] signal is set to a high level. T6 is turned on and node C is connected to the anode of the OLED. Since the voltage stored in C1 and C2 is maintained until the reset stage of the next frame, the DRT flows a constant data current to the OLED proportional to the voltage of the capacitors. Therefore, the OLED current can be expressed as follows:

$$I_{OLED} = k \times \left(V_{GS,DRT} - V_{TH,DRT}\right)^2, \quad (6)$$

$$= k \times \left(V_{DATA} - \Delta V\left(t_{comp}, \quad \mu_{DRT}, V_{DATA}\right)\right)^2. \quad (7)$$

The OLED current equation of the proposed pixel circuit shows that it is independent of the threshold voltage of the DRT, and also compensates for the mobility variation of the DRTs in the panel.

III. SIMULATION RESULTS AND DISCUSSION

The voltage changes at each node during the circuit operation were verified using HSPICE from Synopsys. In the simulation, all switching TFTs are set to 3 μm in width and 3 μm in length, and the driving TFT is set to 3 μm in width and 12 μm in length. Two storage capacitors, C1 and C2, are set to 21 fF and 18 fF, respectively. These capacitance values were calculated based on the capacitor area in the designed layout and the fabrication design rule. The switching voltage of SCAN1[N], SCAN2[N], SCAN3[N], SCAN3b[N] and EM[N] signals ranges from -10 to 20 V. V_{DATA} ranges from 1 V to 10 V, and ELVDD, ELVSS, and V_{REF} are set to 12, 0, and 7 V, respectively. The OLED is modeled by diode-connected TFT, where the TFT is 10 μm in width and 9.5 μm in length. Prior to the simulation, an oxide TFT model library was developed based on the measured electrical properties of a fabricated oxide TFT device, and the developed library exhibited high accuracy with a coefficient of determination (R^2) of 0.9999 as shown in Fig. 2(a) and (b). Thus, we can secure high reliability of simulation.

Fig. 3(a) shows the simulated voltage of nodes A, B, and C when V_{DATA} is 4 V and t_{comp} is 0.7 μs. The duration of the data input stage is set to 3 μs to fulfill the 120 Hz refresh rate for UHD resolution even when t_{comp} increases to 0.7 μs. The voltage of each node in each stage closely matches the theoretical value described earlier. However, in the actual circuit operation, the switching voltage change can affect the stored voltage of the capacitor due to non-ideal factors such as parasitic capacitance between gate to source. As a result, when entering the mobility compensation stage, the voltage of node A (V_A) slightly increases, and the voltage of node C (V_C) slightly decreases. Fig. 3(b) shows the simulated voltage of node C when the $V_{TH,DRT}$ shifts from −4 V to 4 V. The voltage of node C during V_{TH} compensation stage accurately reflects such shift despite the wide range of $V_{TH,DRT}$ shift. Based on these results, we can confirm that the proposed pixel circuit is capable of precisely compensating for severe non-uniformity of $V_{TH,DRT}$. Fig. 4 shows the simulated voltage of node C and voltage difference between nodes A and C, when V_{DATA} is 4 V and t_{comp} is 0, 0.3, 0.5, and 0.7 μs, respectively. Here, the voltage difference between nodes A and C is equal to the total stored voltage in C1 and C2. Additionally, Fig. 5 shows an identical transient voltage waveform when t_{comp} is 0.7 μs, and V_{DATA} is 1, 4, 7, and 10 V, respectively. Fig. 4 and Fig. 5 demonstrate that the total stored voltage decreases as t_{comp} and V_{DATA} increase. These results confirm that the mobility compensation voltage is dependent on t_{comp} and V_{DATA}, as

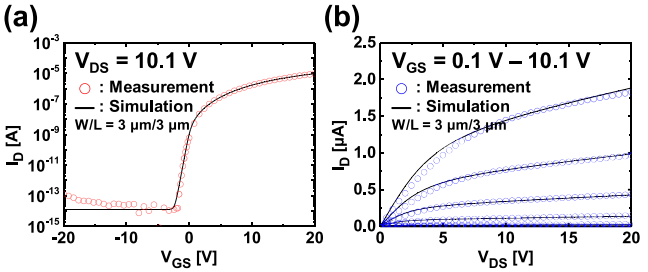

FIGURE 2. Measured and simulated (a) transfer characteristic, and (b) output curves of a-IGZO TFT with a size of 3 μm/3 μm. The V_{GS} interval of output curves is 2 V.

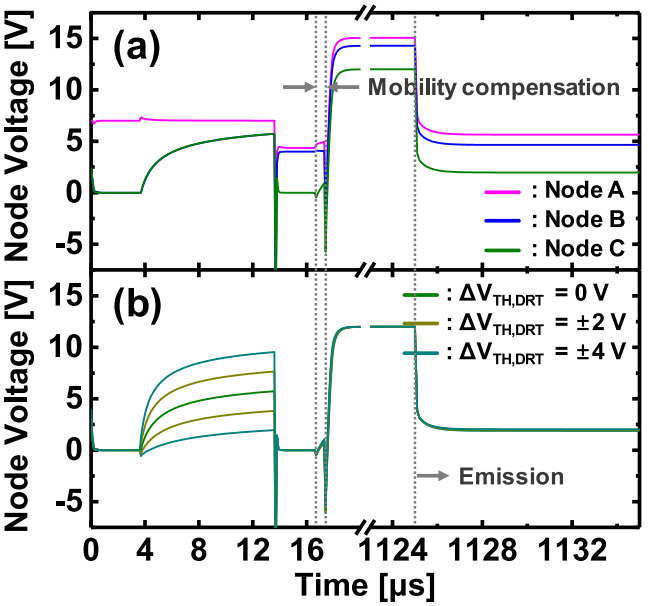

FIGURE 3. (a) Simulated voltage of node A, B, and C when V_{DATA} is 4 V and t_{comp} is 0.7 μs, and (b) simulated voltage of node C when $V_{TH,DRT}$ shift ranges from −4 V to 4 V.

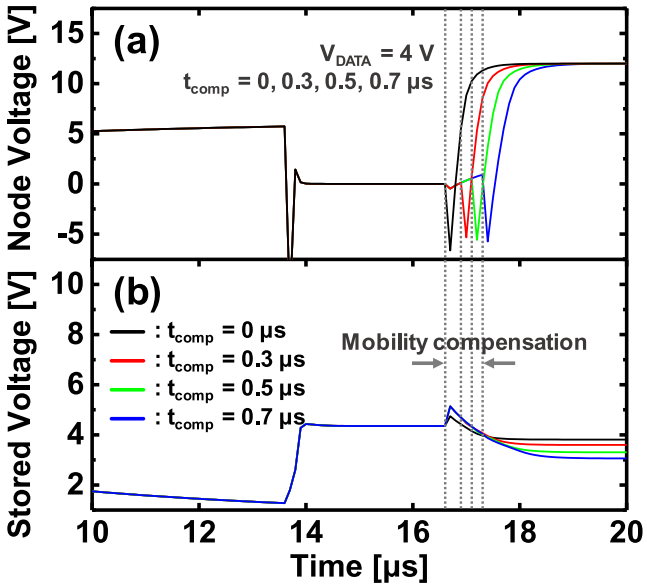

FIGURE 4. (a) Simulated voltage of node C, and (b) voltage difference between nodes A and C according to t_{comp}, when V_{DATA} is 4 V.

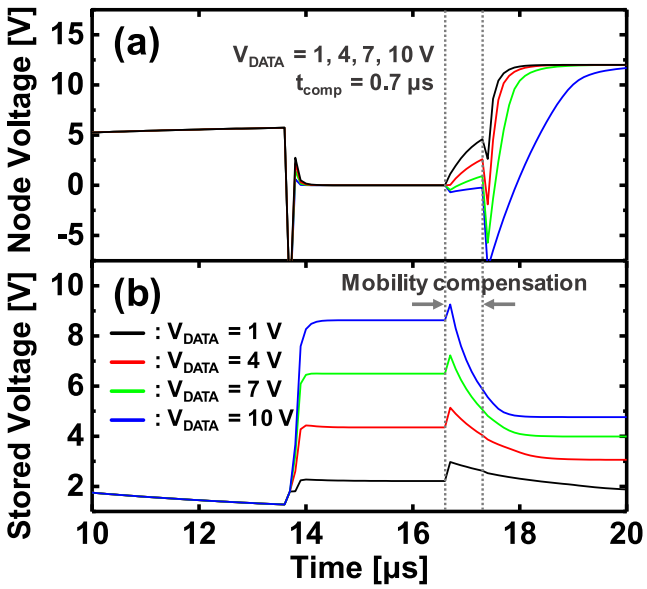

FIGURE 5. (a) Simulated voltage of node C, and (b) voltage difference between nodes A and C according to V_{DATA}, when t_{comp} is 0.7 μs.

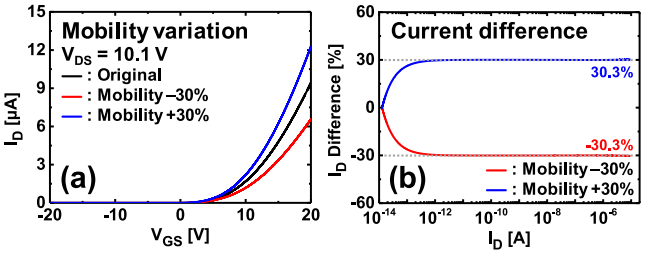

FIGURE 6. (a) Transfer curves with the mobility variation of 30%, and (b) its calculated current difference according to I_D.

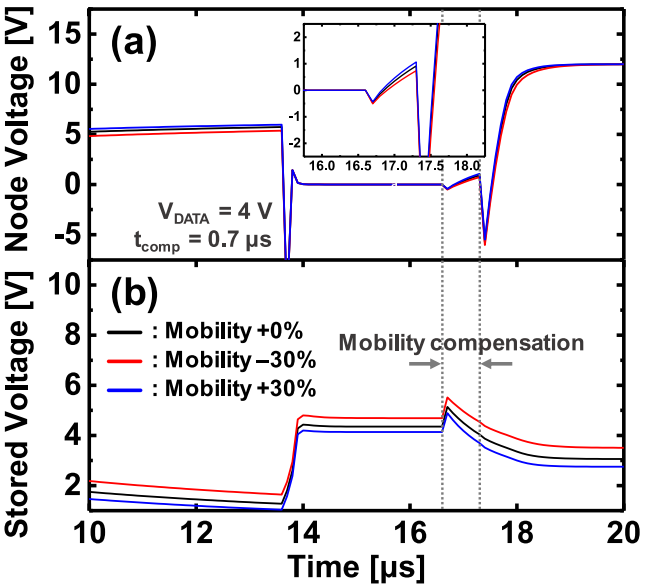

FIGURE 7. (a) Simulated voltage of node C, and (b) voltage difference between nodes A and C according to mobility, when t_{comp} is 0.7 μs, V_{DATA} is 4 V.

indicated in equation (5), and the mobility compensation stage operates effectively as intended.

The compensation accuracy of the proposed circuit for V_{TH} and mobility is verified through simulation. In the simulation, we adjust the V_{TH} of DRT ($V_{TH,DRT}$) and mobility of DRT (μ_{DRT}) by changing the relevant parameters in the model library. $V_{TH,DRT}$ is changed by ±4 V using the parameter VTO, while μ_{DRT} is changed by ±30% using parameters MUS, MU1, and MU0, which correspond to the subthreshold, low-field, and high-field mobility, respectively. These adjustments consider the standard deviations of characteristics in the fabrication process, which are extracted from measured data. The standard deviations are approximately 3.9 V for V_{TH} and 28% for mobility. Fig. 6(a) and (b) show the results of the implemented mobility variation, and the current difference remains at 30% across the entire current range. This results indicates that the mobility is accurately changed by 30% as intended.

Fig. 7 shows the identical voltage graphs as Fig. 4 and Fig. 5. Fig. 7 indicates that the mobility compensation voltage is approximately 0.2 V when the mobility differs by 30%, under the operating condition with t_{comp} of 0.7 μs and V_{DATA} of 4 V. Fig. 8(a) shows the compensated OLED current of the proposed pixel circuit when $\Delta\mu_{DRT}$ is ±30%. The current is plotted according to t_{comp}, where the t_{comp} was set as 0, 0.3, 0.5 and 0.7 μs. The current level decreases as t_{comp} increases, because the longer t_{comp}, the bigger the voltage drop. However, the longer t_{comp} further intensifes the difference in voltage drop caused by mobility variation, thereby enhancing the mobility compensation effect. Thus, the mobility compensation errordecreases as t_{comp} increases, as shown in Fig. 9(a). With a t_{comp} of 0.7 μs, the maximum current error rates are 3.2% and 4.8%

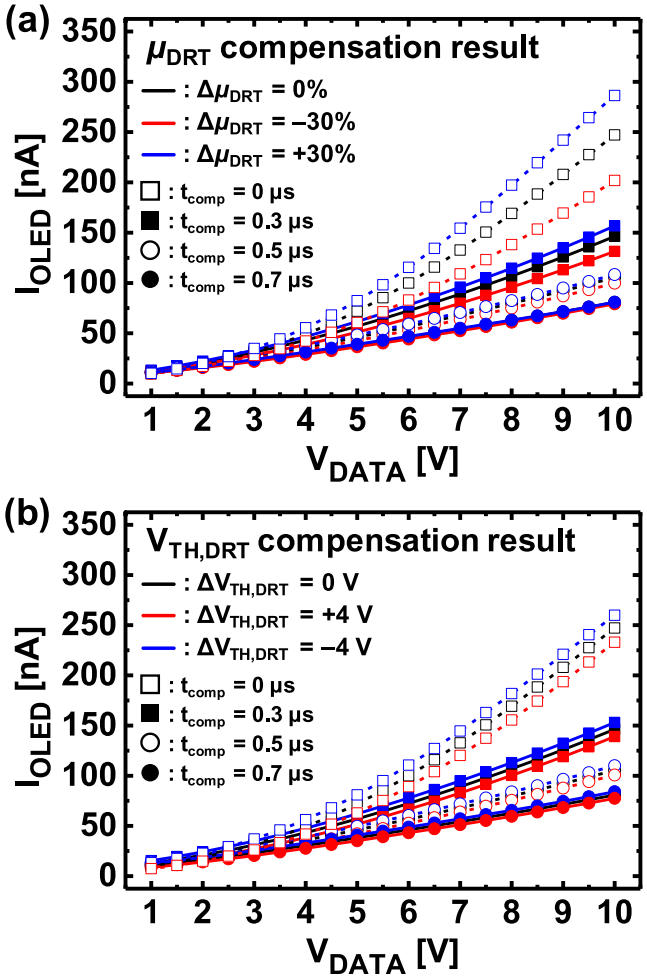

FIGURE 8. Compensated OLED current of the proposed pixel circuit when (a) $\Delta\mu_{DRT}$ is ±30%, and (b) $\Delta V_{TH,DRT}$ is ±4 V. The current is plotted according to t_{comp}, where t_{comp} is set as 0, 0.3, 0.5 and 0.7 μs.

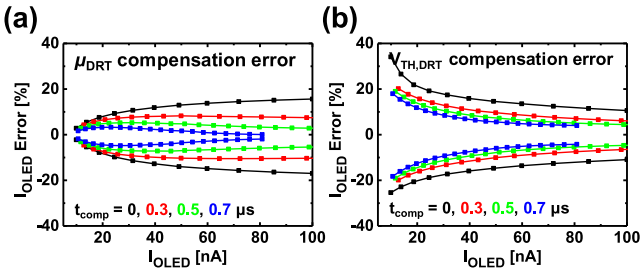

FIGURE 9. OLED current error rates of the proposed pixel circuit when (a) $\Delta\mu_{DRT}$ is ±30%, and (b) $\Delta V_{TH,DRT}$ is ±4 V. The current is plotted according to t_{comp}, where t_{comp} is set as 0, 0.3, 0.5 and 0.7 μs.

TABLE 1. Comparison of the proposed pixel circuit with other works.

Category	[27]	[28]	[29]	Proposed
Pixel circuit structure	3T2C	5T2C	3T2C	7T2C
V_{DS} at mobility compensation stage	$\propto V_{TH}$**	$\propto V_{TH}$	$\propto V_{TH}$	ELVDD
Capacitive coupling at data input stage	O	X	O	X
$C_{eff,comp}$* at mobility compensation stage	1	0.5	1	1
V_{TH} compensation scheme	Source follower	Source follower	Diode connection	Source follower

* Effective capacitance when current flows during mobility compensation
** V_{DS} at mobility compensation stage is dependent on V_{TH} of DRT

for $\Delta\mu_{DRT}$ of +30% and −30%, respectively. The optimal mobility compensation time can be adjusted by considering factors such as the mobility variation characteristics of the panel, the target data current range, and the size of DRT. We believe that the current reduction effect during the mobility compensation stage would be highly applicable to high-PPI mobile displays, where only tens of nA is required to achieve maximum brightness due to the small size of the subpixel.

Meanwhile, the I_{OLED} error is less than 30% even with a t_{comp} of 0 μs, as shown in Fig. 9(a). This is because the detected V_{TH} varies depending on the mobility. The difference in detected V_{TH} can contribute to a certain degree of mobility compensation effect. Even so, the I_{OLED} error in high gray levels is still high, as such mobility compensation effect during V_{TH} compensation is very subtle. Therefore, a separate mobility compensation stage is necessary to supply a uniform current.

Fig. 8(b) shows the compensated OLED current when $\Delta V_{TH,DRT}$ is ±4 V with the corresponding t_{comp} as in Fig. 8(a). The V_{TH} compensation error shows variation depending on t_{comp}; It decreases as t_{comp} increases. Following the theoretical operation described earlier, the mobility compensation stage should not affect V_{TH} compensation. However, in actual operation, differences in mobility compensation can arise due to the non-ideal V_{TH} compensation, which in turn results in improved V_{TH} compensation accuracy. During the mobility compensation stage, a smaller $V_{TH,DRT}$ leads to a slightly faster charging process. This is attributed to imperfect V_{TH} compensation, where smaller $V_{TH,DRT}$ lead to a slightly higher current due to the V_{TH} compensation error. Consequently, the voltage of node C rapidly increases during the mobility compensation stage when $V_{TH,DRT}$ is smaller. This disparity in capacitor charging enhances the V_{TH} compensation effect, so V_{TH} compensation error decreases. Also, as such disparity increases with higher t_{comp}, the longer mobility compensation further strengthens the aforementioned effect and reduces the V_{TH} compensation error as shown in Fig. 9(b). Meanwhile, it is worth noting that the observed large V_{TH} compensation error rate can be attributed to the consideration of significant V_{TH} variation in the employed fabrication process. However, if we adopt the conventional approach of considering a narrower V_{TH} shift range of 0.5 V, the error rate significantly reduces to approximately 2%, indicating precise V_{TH} compensation.

Table 1 compares the operation of the proposed pixel circuit with other works. Although the structure of our circuit is relatively complicated, this structural difference has yielded superior operational stability compared to other circuits [27], [28], [29]. In circuits [27], [28], [29], V_{DS}

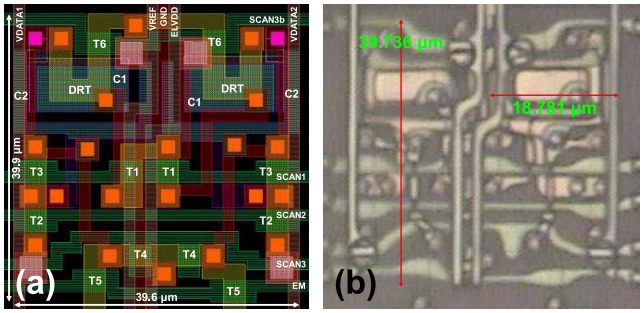

FIGURE 10. **(a) Layout of proposed pixel circuits, and (b) micrograph of the fabricated pixel circuits.**

varies with $V_{TH,DRT}$ when the mobility compensation stage begins, resulting in different compensation levels even for the same gray level. In contrast, our proposed circuit maintains a constant V_{DS}, ELVDD, so precise mobility tendencies can be accurately reflected in the mobility compensation stage for each gray level. This operational stability is particularly noteworthy when substantial variation exists in $V_{TH,DRT}$ or when the saturation characteristic of DRT is suboptimal.

IV. EXPERIMENTAL RESULTS

After verifying the compensation accuracy through simulation, the operation of the proposed pixel circuit is experimentally validated by fabricating pixel circuits. The variations in the fabrication process are consistent with the values mentioned above in the simulation. Fig. 10(a) shows a layout of the proposed circuit. To reduce the layout area, two pixel circuits were designed together using a mirrored structure with shared REF, GND, and ELVDD power lines. The total area of the layout for two pixel circuits is 39.6 μm $\times$ 39.9 μm, so the single pixel circuit only occupies the area of under 19.95 μm $\times$ 39.9 μm. This compact pixel circuit area makes achieving a high resolution of 635 PPI or above possible. The micrograph of the fabricated pixel circuit is shown in Fig. 10(b). To verify the operation of fabricated circuits, signals were applied using an ELP Corporation pattern generator EEC-HT01, and then the OLED current was measured with Keysight B1500A. The t_{comp} was set to 0 μs, and V_{TH} compensation and data input time were set to the same values as in the previous simulation, assuming UHD resolution and 120 Hz refresh rate. The transient waveform of the measured OLED current for several frames is shown in Fig. 11(a). Here, the applied V_{DATA} was ranged from 1 V to 10 V, with 1 V interval. The measured data from three fabricated circuits show a high degree of uniformity among each other as shown in Fig. 11(b). The error rate falls within the range obtained from the simulation, which considers variations in the fabrication process.

V. CONCLUSION

In this paper, we propose a new 7T2C a-IGZO pixel circuit for high-PPI AMOLED mobile displays, which compensates for both V_{TH} and mobility variations. The V_{TH} and mobility compensation accuracy of the proposed circuit

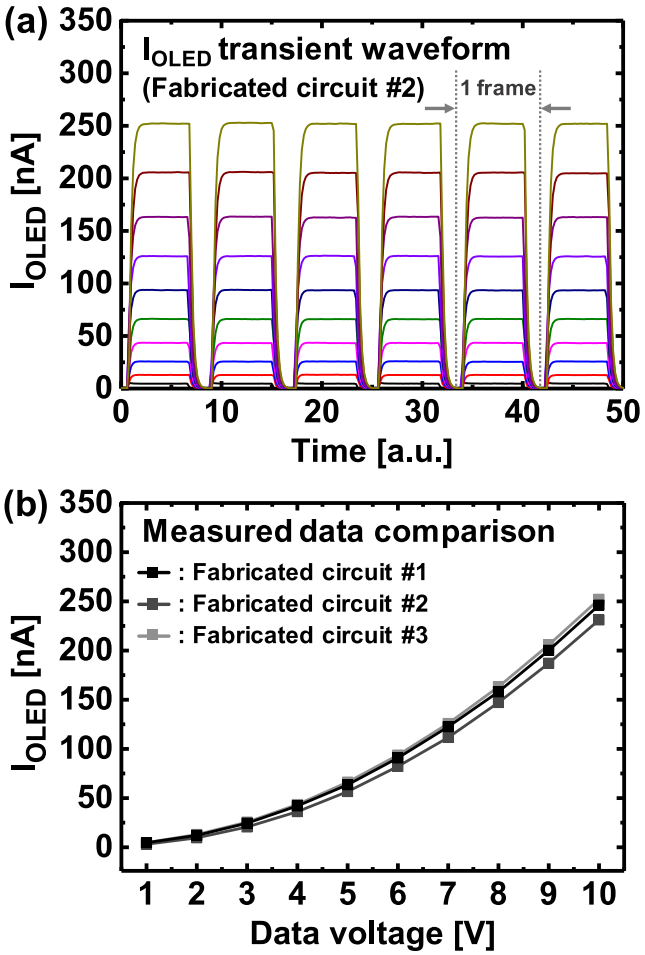

FIGURE 11. **(a) Measured transient waveform of OLED current of fabricated circuit #2, and (b) measured current levels of fabricated circuit #1-3 according to data voltage.**

was verified through simulation. The mobility compensation error decreases as t_{comp} increases, and the maximum current error rate is under 5% when t_{comp} is 0.7 μs. The V_{TH} compensation error is relatively high; however, this is because we considered the significant V_{TH} variation of $\pm$4 V in the simulation. Additionally, we analyzed the reason for decreasing V_{TH} compensation error according to t_{comp}. Meanwhile, we fabricated the proposed pixel circuit with an area of 19.95 μm $\times$ 39.9 μm that can achieve a high resolution of 635 PPI. The circuit operation with 120 Hz refresh rate was verified experimentally by measuring the current of the fabricated circuits, and the data shows relatively consistent levels. Based on the simulation and experimental results, we can conclude that the proposed pixel circuit effectively compensates for both V_{TH} and mobility variations. Therefore, we expect that this circuit will reliably supply a uniform current even under variations in the electrical characteristics of DRTs.

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