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A CMOS-Compatible Gate-Assisted Photonic Demodulator With Contrast Enhancement for Time-of-Flight Sensing

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ABSTRACT This paper presents a CMOS-compatible gate-assisted photonic demodulator with contrast enhancement (GAPD-CE) techniques. To form an asymmetric field inside the substrate that will facilitate the transfer of photogenerated electrons, p-well and channel doping techniques are applied under the polysilicon guides. Modulation contrast (MC) values extracted from TCAD simulation show that the modified structure effectively collects electrons generated deep within the substrate. A prototype of the GAPD-CE is fabricated in a 0.18-μm standard CMOS foundry process. An MC of 83% and 57% at 1 MHz and 30 MHz, respectively, are achieved under 850 nm illumination, demonstrating the potential of the proposed device for time-of-flight (ToF) sensing applications.

INDEX TERMS Gate-assisted photonic demodulator, time-of-flight, high modulation contrast.

I. INTRODUCTION

Depth sensors have found many new applications, such as virtual/augmented reality [1], robotic vision, and autonomous vehicles [2]. Among all the depth sensing methods, the modulation-based indirect time-of-flight (iToF) is the simplest approach for high-resolution depth sensing that can be implemented in low-cost standard CMOS processes. The most important component of modulation-based iToF sensing is that of the photonic demodulator (PD) to mix the electrical signal with the optical signal. Different types of PDs have been demonstrated, including the charge coupled device (CCD) [3], pinned photodiode (PPD) [4], [5], [6], [7], [8], photogate (PG) [9], [10], current-assisted photonic demodulator (CAPD) [11], [12], and gate-assisted photonic demodulator (GAPD) [13].

The most important performance parameter of a PD is the modulation contrast (MC) at high frequency. This parameter evaluates the PD's capability of mixing and separating electrons [14]. To achieve high MC and bandwidth, some electric field to accelerate the carrier movement is needed. This favors electric field-driven devices such as CAPD or GAPD. Between these two, GAPD can achieve lower power consumption as it has no direct current path between the modulating terminals as the electric field is applied through capacitors. However, it also suffers from a lower electric field leading to lower MC. In order to improve the GAPD MC, we proposed a cost-effective modification to the traditional GAPD structure in a standard CMOS process and demonstrated it through theoretical analysis and experimental demonstration.

II. PERFORMANCE LIMITATION OF TRADITIONAL GAPD

Fig. 1 (a) shows the basic structure of a GAPD in a CMOS process, and also a simulation result that will be explained in this section later. In GAPD, the electric field applied in the optical window, with a length of L_p, is through a

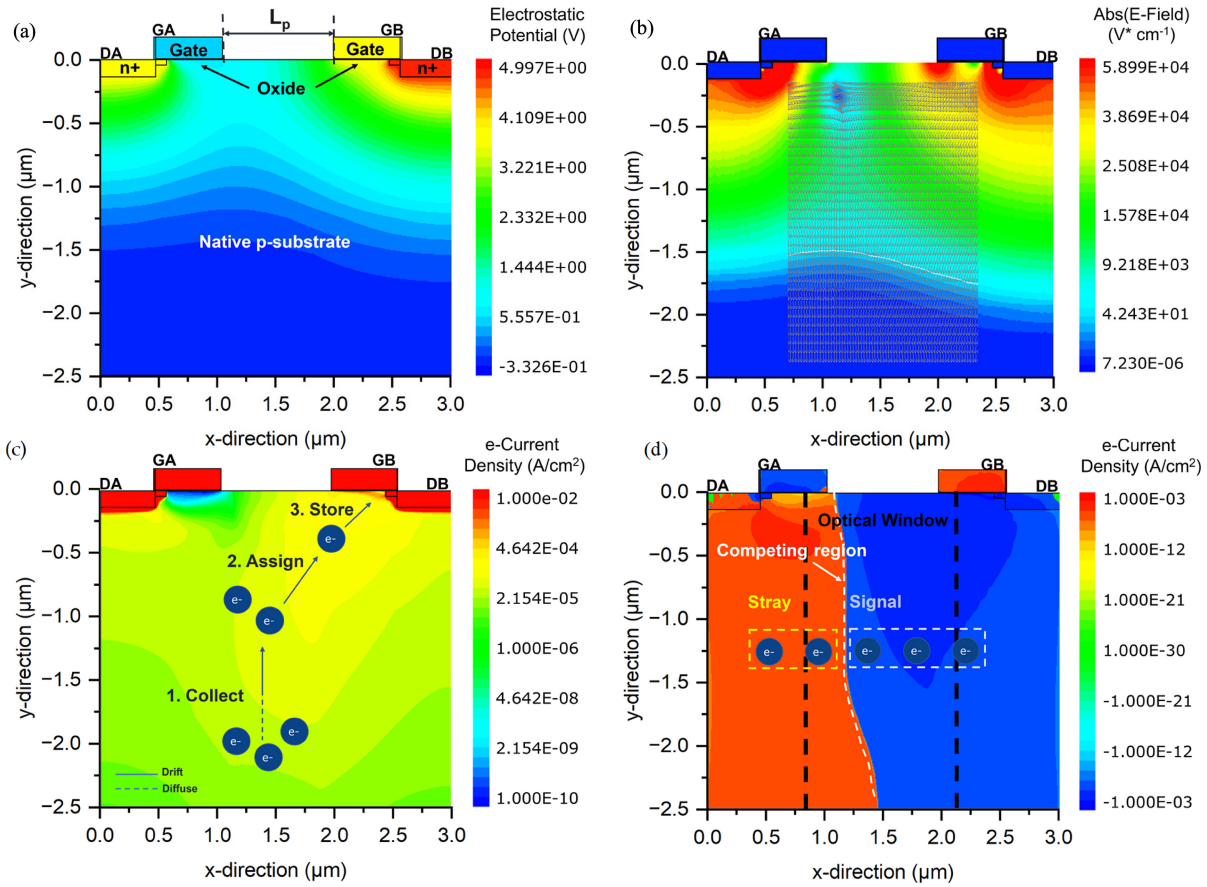

FIGURE 1. **(a) Structure of a GAPD in a CMOS process, with a potential plot when $V_{GA} = 0$ V and $V_{GB} = 3.3$ V. (b)Electric field plot in GAPD, when $V_{GA} = 0$ V and $V_{GB} = 3.3$ V. E-field directions and cutline of the depletion region are only plotted in the center region for clarity. (c) Current density plot in GAPD, when $V_{GA} = 0$ V and $V_{GB} = 3.3$ V. With this gate biasing conditions, the optically generated electrons are driven towards GB and collected in DB. (d) Electron current density plot for a conventional GAPD structure along the lateral direction with the same bias conditions as (a). Because of the high voltage applied to DA, the generated electric field competes with the field in the optical window and left electrons along the competing region cutline become stray.**

capacitor. Through the polysilicon gate electrodes, GA and GB, optically generated electrons are driven towards GA or GB at different time phases. DA and DB are two n-doped regions placed next to the gates to collect the re-directed electrons. Since standard CMOS is considered in this paper, finite small n-type channel regions have been added closed to DA and DB, to mimic the effect of lightly-doped drain (LDD) in the standard CMOS process.

Under normal operation conditions, the collection sites, DA and DB, are first reset to certain voltage by MOSFETs, and then become floating. Different gate voltages, V_{GA} and V_{GB}, are applied to create a strong electric field inside the substrate and preferentially direct electrons to either one of the collection sites. For iToF applications, a light source with a wavelength of around 850 nm is typically used and optically excited electrons are generated deep in the substrate. In order to collect these electrons, a vertical electric field is needed to drive the deep electrons to the surface before they can be collected by the lateral field. Otherwise, the optically generated electrons will either be lost due to recombination or collected by some undesirable terminals which can cause the blurring of an image. To have the vertical electric field reach deep within the substrate and collect the optically generated electrons, a lightly doped substrate is necessary. At the same time, a short L_p is desirable to promote the lateral drift of electrons and avoid recombination in the optical window. It was also proposed that increasing the gate length can lead to high collection efficiency, but the adjustable range is quite limited for small devices within 3 μm. Meanwhile, it causes higher dynamic power due to a higher loading capacitor, and this will not be considered in this work.

To illustrate the operation principle described, TCAD simulations are performed using Sentaurus. Considering a 0.18-μm standard CMOS process, an L_p of 1 μm, a gate length of 0.6 μm, a gate width of 7μm, a gate height of 0.2 μm, an oxide thickness of 7nm, and a substrate doping, NA, of about 10^{15} cm^{-3} are considered in the simulation. For the light source, an illumination intensity of 2.5 mW/cm^2 is considered, which is typically the light intensity of 850 nm lasers used in iToF applications using calculations in [15]. Without a loss of generality, when VGA

is set to 0 V while VGB is set to 3.3 V, the potential distribution is shown in Fig. 1 (a), and the electric field is plotted in Fig. 1 (b). For clarity, E-field directions and cutline of the depletion region are only plotted in the center region. The photo-generated electrons are swept from deep within the substrate (collect), directed towards GB (assign), and, eventually reach DB (store) as shown in the current density plot in Fig. 1 (c).

Given the traditional structure of GAPD, the high voltage from DA competes with the electric field set by the gate electrodes in collecting the photogenerated electrons in the optical window, as shown in Fig. 1 (a) and Fig. 1 (b). This leads to a large value of stray electrons lost due to being collected by the other detector terminal. The modulation contrast, MC, given by the following equation in [16], is a widely adopted benchmark to quantify the effectiveness of carrier collection, and it can be calculated using:

$$MC = \frac{N_{sig} - N_u}{N_{sig} + N_u} \tag{1}$$

where N_{sig} is the number of electrons synchronized with the guide voltage that contributes to the signal, and N_u is the number of stray or unsynchronized electrons.

To highlight the competing mechanism in collecting the generated carriers, the current density plot along the lateral direction, with the same bias conditions as Fig. 1 (a), is shown in Fig. 1 (d). Because of the competing mechanism in collecting the photogenerated electrons, N_u increases and the modulation contrast of the traditional structure significantly degrades. As discussed previously, to effectively collect electrons generated deep within the substrate, i.e., increase N_{sig}, the substrate doping, and optical window length can be reduced. However, even by using these approaches, the modulation contrast can only be improved to around 80%, as shown in Fig. 2 (a). For the lightly doped cases (3×10^{14} cm^{-3}, 7×10^{14} cm^{-3}), the device can fully transfer all the deep electrons caught, maintaining a relatively high MC value. For the densely doped cases (3×10^{15} cm^{-3}, 7×10^{15} cm^{-3}), the device MC value is relatively low but stable because most of the deep electrons are lost. Meanwhile, for the case of 1×10^{15} cm^{-3}, the deep electrons can only be partially transferred in the given time, which leads the MC to drop together with the frequency. In the simulation, square modulating waves with certain frequencies, changing from 3.3 V, to GND, are added to GA and GB, after resetting DA and DB to 3.3 V. The clock diagram is shown in Fig. 2 (b). N_{sig} and N_u are calculated using the voltage drops in DA and DB after certain periods of integrations.

III. GAPD PERFORMANCE ENHANCEMENT TECHNIQUE

To enhance the modulation contrast, it is clear from the previous section that N_u must be reduced and N_{sig} must be increased. To accomplish this, both the lateral and vertical transport of carriers from the window to the desired collection nodes must be improved. As electrons are generated deep within the substrate, the first step is to ensure

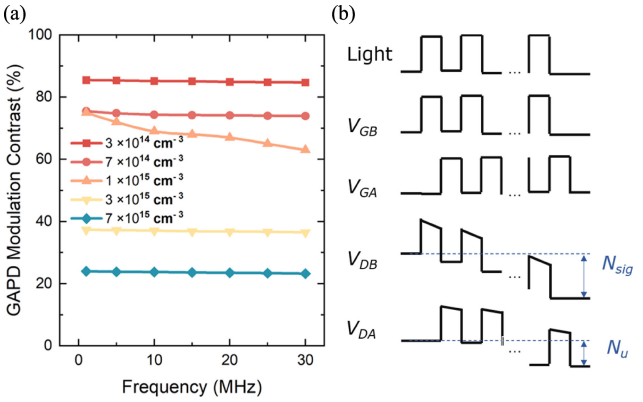

FIGURE 2. (a) Modulation contrast MC, at different operating frequencies, and doping concentrations. With the traditional GAPD structure, even by reducing the substrate doping and using a short L_p, MC can be only improved up to around 80%. (b) Clock diagram. In the simulation, square modulating waves, changing from 3.3 V to GND, are added to GA and GB, after resetting DA and DB to 3.3 V.

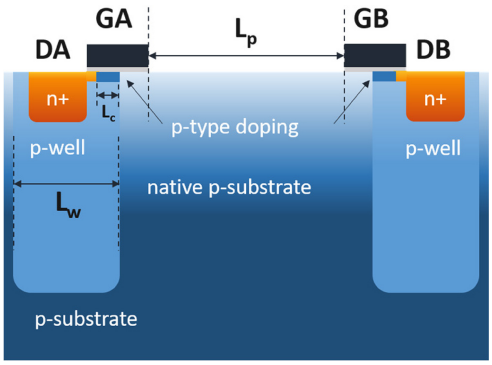

FIGURE 3. GAPD with contrast enhancement (GAPD-CE) physical structure.

that they are not collected by the unwanted detector node. By adding a p-well on the n+ regions, the barrier between the n+/p-well regions can be increased, and electrons will then move preferentially towards the gate electrode with higher potential and eventually be collected by the desired detector node, thereby reducing N_u and increasing N_{sig}. Furthermore, a doping concentration similar to p-channel doping will be applied under a finite region of the gate electrode, which usually occurs in the standard CMOS process together with the p-well. Based on these two modifications, we propose the gate-assisted photonic demodulator with contrast enhancement (GAPD-CE), as shown in Fig. 3.

To verify our idea, we considered the typical values for the p-well and p-channel doping concentrations from the standard CMOS process. We therefore added 10^{16} cm^{-3} p-well doping with 0.7 μm length (L_w), and 10^{18} cm^{-3} p-type channel doping with 0.1 μm length (L_c) in our original simulation deck for GAPD to form GAPD-CE. Different from the designed value of 0.7 μm, the value of 0.1 μm is an estimated length value considering the p-well mask, poly mask, and n+ region mask, since there usually does not have

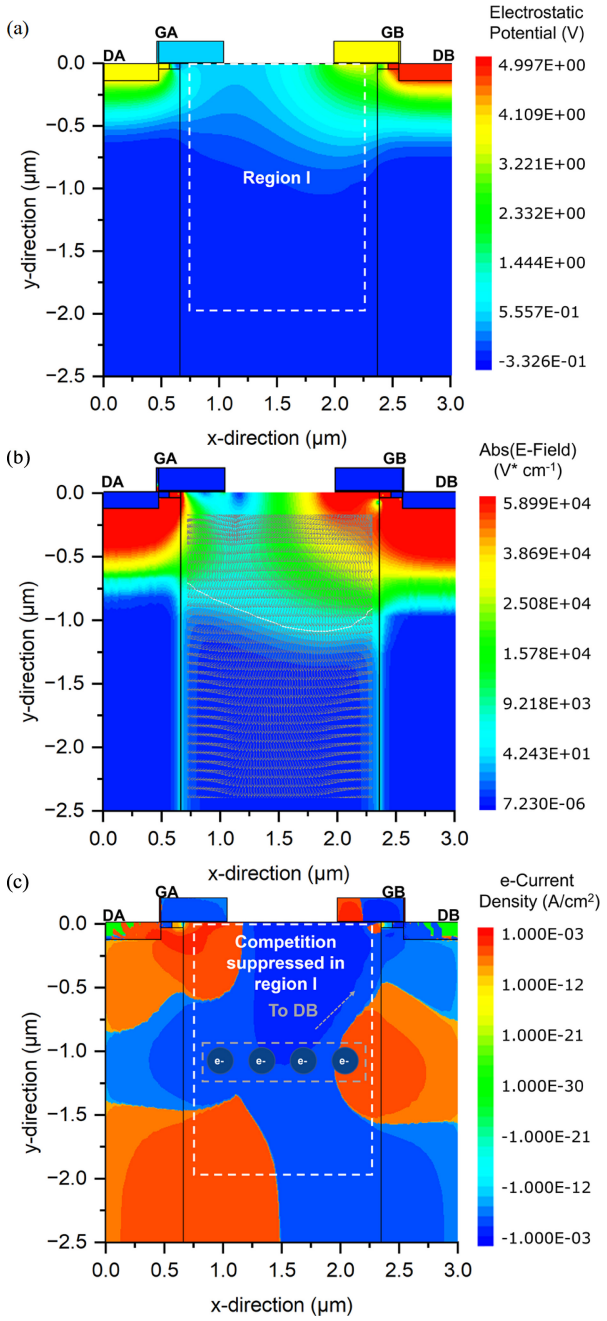

FIGURE 4. (a) Potential (b) Electric field and (c) Electron current density contour plot along the lateral direction in GAPD-CE, when $V_{GA} = 0$ V and $V_{GB} = 3.3$ V. The competing mechanism is suppressed due to the n+/p-well regions and most photogenerated carriers are collected by the desired detector node DB.

a dedicated mask for the p-type channel region. The light intensity, wavelength, biasing conditions are the same as our simulation for the GAPD device. With the GAPD-CE structure, an asymmetric electric field can be generated, as shown in Fig. 4 (a) and Fig. 4 (b), when V_{GB} is 3.3 V and V_{GA} is 0 V. The barrier height, for example, at the edge of Region I in Fig. 4 (a), has been increased 36% compared with the original structure at the depth of 0.5 μm. The competing mechanism is also suppressed due to the n+/p-well regions, and most photogenerated carriers are collected by the desired detector node, as shown in Fig. 4 (c). The signal currents, IDA and IDB, as a function of the VGB, when VGA is 0 V, are given in Fig. 5 (a), which shows that GAPD-CE is better than the traditional GAPD in the DC regime. The calculated MC for GAPD-CE is 86%, while the traditional GAPD is 75% at a 3.3 V gate voltage difference. The MC is calculated by treating IDA and IDB as N_u and N_{sig}, respectively, in equation (1).

The improvement in MC can be attributed to how the proposed GAPD-CE structure can effectively collect the carriers generated deep within the substrate and convert it to N_{sig}. To illustrate this, we vary the depth where the peak generation rate occurs along the substrate and extracted the MC. The generation rate is around 10^{19} cm^{-3}s^{-1} for a general average rate of 2.5 mW/cm^2 light intensity. It can be observed from Fig. 5 (b) that for the traditional GAPD structure, MC is relatively constant when the peak generation is well within 1 μm from the surface, and significantly reduced beyond. In contrast, for GAPD-CE, the MC keeps increasing when the generation depth is smaller than 1μm, and although the trend for MC also decreases beyond the 1μm depth, the extracted MC still outperforms the conventional GAPD in general. In fact, for electrons generated deep within the substrate, say around 2 μm from the surface, the MC for GAPD-CE is around 80%, while for GAPD, it is about 64%. This demonstrates that carriers' lateral and vertical transport is improved due to the improved structure.

On the other hand, to illustrate the tradeoff, an average lateral electric field, $E_{avg-lateral}$, is calculated in the Region I in Fig. 4 (a) using:

$$E_{avg-lateral} = \iint_{Region\ I} E_x\ dxdy \tag{2}$$

The $E_{avg-lateral}$ can be used as a metric of lateral charge transport speed. The $E_{avg-lateral}$ for conventional GPAD in Fig. 1 (a) is -1.64 V$\cdot\mu$m, and for GPAD-CE in Fig. 4 (a) is -1.14 V$\cdot\mu$m. The result indicates that the $E_{avg-lateral}$ in GPAD-CE is sacrificed 30% to form the aforementioned electric field structure. Typically, a lower $E_{avg-lateral}$ means a lower lateral charge transfer speed in the sensing device, leading to a lower N_{sig} and may cause a lower MC. However, from Fig. 5(a) we shall see, although the lower $E_{avg-lateral}$ lowers the I_{DA} and I_{DB} in GAPD-CE, compared to GPAD, a better MC can be obtained in this tradeoff. It may be noted that Quantum Efficiency (QE) has been somehow lowered in this case. However, in a typical iToF sensing system, the storage capacity inside the pixel is always limited, and MC determines the maximum valid signal amount (N_{sig}-N_u) that can be stored in this limited capacity. Therefore, the value of MC is more important than the other parameters, such as QE, integration time, and Fill Factor (FF).

So far, all the analyses for GAPD-CE in Section III are based on static analysis. It is essential to consider the ToF modulation feature in different frequencies. The GA and GB

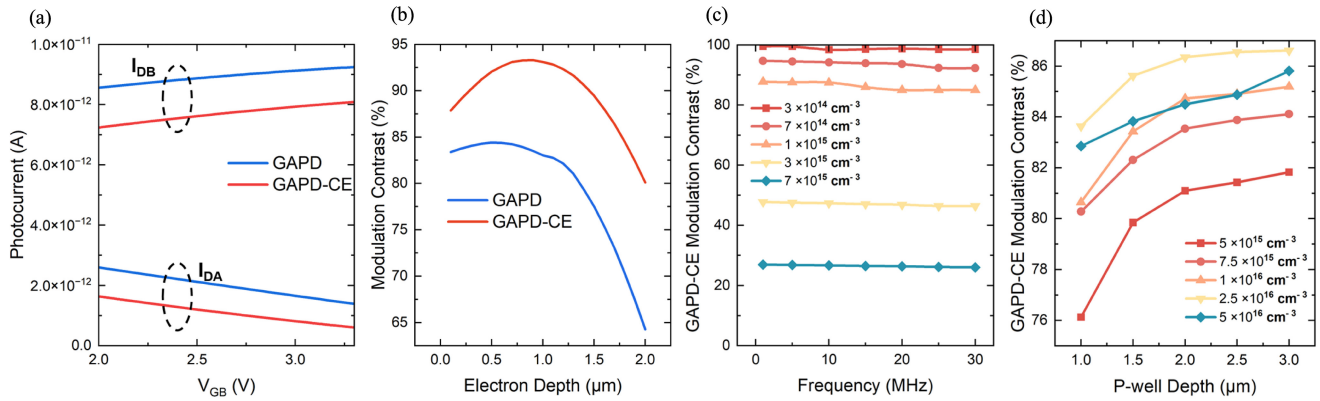

FIGURE 5. **(a) Simulated signal currents, I_{DA} and I_{DB}, at different gate voltage differences for GAPD and GAPD-CE. It shows that GAPD-CE is better than the traditional GAPD in the DC regime. (b) Extracted MC for GAPD and GAPD-CE when different electron generation depths are adopted along the substrate. The carrier lateral and vertical transport is improved due to the improved structure. (c) Simulated GAPD-CE MC values with different substrate doping. A MC more than 85% can be achieved in 30 MHz with a typical process doping. (d) Simulated GAPD-CE MC values with different p-well depth and doping. Within a typical CMOS process range, the performance of GPAD-CE is stable with different p-well conditions.**

will be connected to the gate voltage and GND in a normal modulation process periodically. This serialized nature means the desired terminal will change at a specific frequency. If electrons cannot arrive at the desired terminal in time, contributing to N_{sig}, they will be driven to another terminal, contributing to N_u, or be recombined. For GAPD and GAPD-CE, as the modulating frequency increase, naturally more electrons cannot arrive at the desired terminal in time, so for both GAPD and GAPD-CE, the MC will drop accordingly due to smaller N_{sig}. However, since more recombination is engaged in GAPD-CE, as more and denser p-type doping has been added inside the substrate, these "absent" electrons are less likely to contribute to N_u than the original GAPD. In this case, the MC will drop slower for GAPD-CE compared to the original GAPD as the frequency increases, which is a desirable feature for ToF sensors.

The MC of GAPD-CE at different frequencies with different substrate doping from the simulation is plotted in Fig. 5 (c) with the same light setting as Fig. 2. Under a typical standard native substrate doping such as 1×10^{15} cm^{-3}, the GPAD-CE can achieve an MC value of more than 85% even when the operating frequency is 30 MHz, which is comparable to the aforementioned unmodified GAPD device under a low substrate doping condition such as 3×10^{14} cm^{-3}. The MC result shows the potential for GAPD to achieve a high MC in a CMOS process after structure modification, as adding doping will be much easier than changing the substrate doping. Concurrently, if the substrate doping can be even lighter for GAPD-CE in a desirable process, such as 3×10^{14} cm^{-3}, an MC value of more than 95% can be achieved.

Furthermore, to verify the device performance under different p-well conditions and ensure the device robustness for GPAD-CE. The simulated GPAD-CE MC values with a typical substrate doping of 1×10^{15} cm^{-3} and a working frequency of 30 MHz are given in Fig. 5 (d). The p-well depth and doping are changed from 1 μm to 3 μm, and from 5×10^{15} cm^{-3} to 5×10^{16} cm^{-3}. The result indicates that, with a typical p-well doping depth of 2-3 μm, the p-well depth has a negligible effect on the MC performance. Even when the p-well depth goes lower than 2 μm and becomes 1μm, the MC maintains above 80% if the doping is more than 7.5×10^{15} cm^{-3}.

Regarding different p-well doping, Fig. 5 (d) also demonstrates that the MC maintains stability if the p-well doping becomes denser than a typical process value such as 1×10^{16} cm^{-3}. However, it should be also noted that the MC will drop if the doping is denser than certain value as shown in the 5×10^{16} cm^{-3} case, which means there is a undepleted region between the gates. Meanwhile, if the p-well doping changes to values closer to the substrate doping, such as 5×10^{15} cm^{-3}, the MC will drop more as it becomes more similar to the case of the original GAPD. In conclusion, within a typical CMOS process range, the performance of GPAD-CE is stable with different p-well conditions.

IV. EXPERIMENTAL DEMONSTRATION

A prototype of the GAPD-CE is fabricated in TSMC 0.18-μm mixed-signal standard CMOS process for verification. The pixel layout and photo are given in Fig. 6 (a) and Fig. 6(b). A parallel structure of 5 GAPD-CEs is implemented within a 20 μm pitch pixel, with MOSFETs for resetting and readout. Native block mask, salicide block mask, and N+ implant mask are implemented together with poly guides to build the aforementioned structure. Except for the desired sensing region in the center, all other areas inside the pixel are shielded. The measured MC from 1 MHz to 30 MHz with 3.3 V guide driving voltage using an 850 nm modulating laser is given in Fig. 7. The result is calculated by the average of consecutive measurements with specially aligned modulation phases between the guides and the laser. Fig. 7 demonstrates that the fabricated GAPD-CE reaches an 83% MC at 1 MHz. From 1 MHz to 10 MHz, the measured MC linearly drops to 61%. Beyond 10 MHz, the MC value

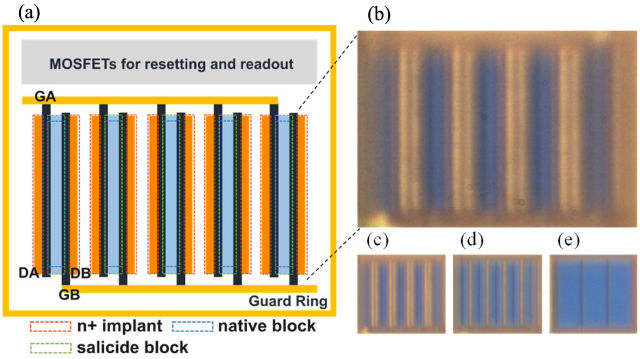

FIGURE 6. (a) Simplified GAPD-CE pixel layout. (b) GAPD-CE device photo. A parallel structure of 5 GAPD-CEs is implemented within a 20 μm pitch pixel. Native block mask, salicide block mask, and N+ implant mask are implemented together with poly guides to build the aforementioned structure. The conventional PPD (c), the native PG with a short optical window (d), and the native PG with a middle gate (PGM) (e) are fabricated in the same round.

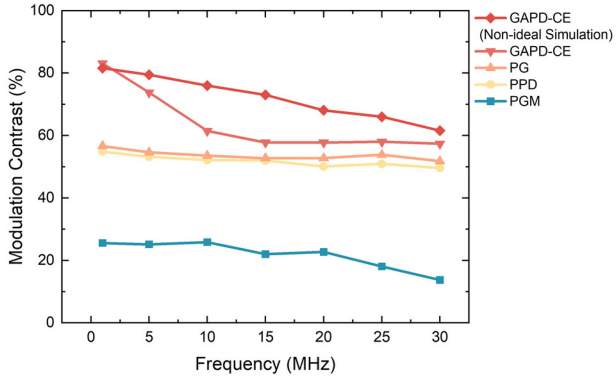

FIGURE 7. Measured MC of devices fabricated in this round, using 850nm laser. The GAPD-CE MC nearly matches the simulation at 1MHz frequency condition and behaves 30% worse than the simulation at a higher frequency range. Among all the fabricated designs in this standard process node, the GAPD-CE is probably the optimal one.

starts to stabilize. The overall MC performance is above 57%. Compared with the simulation result with a doping concentration of 1×10^{15} cm^{-3}, this result nearly matches it at 1 MHz, but drops around 30% in the range between 10 MHz and 30 MHz.

The potential causes can be from the mask offset/mismatch and the unperfect light signal. As some design rules have to be violated to make the device work in the transistor process and the device size is relatively small in this process node, mask offset/mismatch exists during the fabrication, and can lead to undesired modulation features. Although the authors have tried to make the same device as in the simulation at the layout level, it is hard to give out a concise offset/mismatch value in a commercial process. This issue can be addressed with a smaller standard process node with fewer design rule limitations in terms of size. What's more, during the simulation, the ideal square optical wave has been assumed as the signal, and there is no delay between the optical signal and the gates. However, the optical equipment cannot generate a perfect square wave in the actual testing scene. Reference [5] points out that if the optical wave is closer to a sine wave, the maximum number of MC is 64%. At the same time, since the test chip and optical laser are not integrated, and there is no clock circuit, such as Delay-Locked Loops (DLL) inside the chip, a delay that cannot be calibrated always exists. To show the effect of the mask offset and the non-ideal clock, a simulation results with 10% salicide block mask offset and 0.5 V/ns clock slew rate are given in Fig. 7 for comparison.

Besides GAPD-CE, some other devices designed by the authors, with similar layouts and readout circuits, have also been fabricated in the same round, as shown in Fig. 6 (c), Fig. 6 (d), and Fig. 6 (e). They include the conventional PPD, the native PG with a short optical window, and the native PG with a middle gate (PGM). To adapt to the standard CMOS process, the PPD in this paper is implemented with a p+/n-well diode instead of a p+/n- diode that is usually used in a CMOS Image Sensor (CIS) process. The measurement results are shown in Fig. 7 as a reference. The measurement results demonstrate that the GAPD-CE is probably the optimal one among all the fabricated designs in this 0.18-μm standard process node. The potential reasons are considered as follows. In terms of PPD, a smooth charge transfer may not be guaranteed without the optimal n- region and dedicated transfer gate. For PG and PGM, the gate length and gate gap can potentially be further optimized. It is very likely that potential gaps exist between the gates of PGM, since a safe distance of 0.25 μm has been kept between the gates according to the design rules.

In other works [4], [5], [6], [9], [11], that use standard CMOS/standard Front-Side-Illuminated (FSI) CIS process, it tends to be challenging to maintain an MC larger than 50% at 20 MHz or more, while in this work, 83% at 1 MHz and 57% at 30 MHz is achieved. Similar works to optimize the MC are done in [7], [8], mainly focus on PPD in the CIS process, and this work focuses on the standard CMOS process. It is also noted that [12] reaches an MC of 80% at 100 MHz, but the substrate doping and thickness are fully optimized in [12], which is hard to achieve in a normal standard CMOS or FSI CIS process. In summary, this result shows that the CMOS-compatible GAPD-CE proposed in this work is a potentially good candidate in the standard CMOS/standard FSI CIS process for ToF sensing. Due to the fabrication limitation of the customized/Back-Side-Illuminated (BSI) CMOS process, it is potential for the GPAD-CE to be applicable for massive production while still maintaining a relatively large MC.

V. CONCLUSION

A CMOS-Compatible Gate-Assisted Photonic Demodulator with Contrast Enhancement techniques (GAPD-CE) is proposed in this paper. Simulation shows that GAPD-CE forms an asymmetric field pattern inside the substrate, which is beneficial for collecting deep electrons and recombining undesired electrons when the operating frequency increases.

With the contrast enhancement techniques in a typical process doping, an 80% MC performance can be maintained for electrons generated at 2 μm under static conditions, and the overall MC performance can be maintained above 85% at a 30 MHz operating frequency. Simulation verifies that different p-well depths and doping will not influence the MC greatly in a typical process range. A prototype GAPD-CE is fabricated in 0.18-μm standard CMOS process for verification. It achieves an 83% MC at 1 MHz and a 57% MC at 30 MHz. The fabrication device nearly matches the simulation at 1 MHz frequency condition and behaves 30% worse than the simulation results at a higher frequency range, possibly due to the mask offset/mismatch and the unperfect light signal. In addition, the GAPD-CE device also outperforms the PPD, PG, PGM that have been fabricated in the same round. These results make the GAPD-CE potentially a good candidate for ToF sensing products.

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