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Three Temperature Regimes in Subthreshold Characteristics of FD-SOI pMOSFETs From Room-Temperature to Cryogenic Temperatures

YO-MING CHANG (Member, IEEE), TING TSAI, YU-WEN CHIU, HORNG-CHIH LIN (Senior Member, IEEE), AND PEI-WEN LI (Senior Member, IEEE)

Institute of Electronics Engineering, National Yang Ming Chiao Tung University, Hsinchu 30010, Taiwan

CORRESPONDING AUTHOR: P.-W. LI (e-mail: pwli@nycu.edu.tw)

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ABSTRACT We reported three temperature regimes in subthreshold characteristics of 22-nm FD-SOI p-MOSFETs at operation T = 300 K – 4.5 K. Subthreshold swing (*SS*)-plateau at 125 K – 50 K in combination with *SS*-linearity at T = 300 K – 125 K and 50 K – 4.5 K were observed in different types of FD-SOI p-MOSFETs with channel length (L_G) $\leq$ 100 nm, which is possibly attributed to temperature-dependent dopant ionization induced band-to-band and trap-assisted tunneling across the drain-body junction. The phenomenon of *SS* linearly decreasing with temperature at T < 50 K is not observed in neither FD-SOI n-MOSFETs nor 28 nm bulk CMOSFETs.

INDEX TERMS Cryogenic, FDSOI, band-to-band tunneling.

I. INTRODUCTION

Subthreshold-swing (*SS*) of MOSFETs is an important electrical parameter, in particular, for dynamic switching and low-power circuitry. Intuitively, lowering operation temperature is a straightforward approach to improve *SS* that is essentially determined by thermal voltage (k_BT/q). However, extensive measurements in structurally different MOSFETs reveal that the benefit of temperature scaling to *SS* appears to cease at deep-cryogenic temperatures. That is, below a critical temperature (T_C), typically around 50 K, *SS* deviates the linear relationship with temperature and saturates to a temperature-insensitive value. The phenomenon of *SS* saturation is detrimental to cryogenic CMOS electronics, suggesting a lower bound on leakage power and the limit of power-performance benefit. *SS* saturation is always observed in mature and advanced MOSFETs fabricated using various technologies (bulk [1], [2], full-depleted silicon-on-insulator (FD-SOI) [3], [4], nanowires [5], fins [6] and nanosheets [7]). The limited *SS* at cryogenic temperatures has been ascribed to combined mechanisms of high-density interface traps (D_{it}) near band edges and high sensitivity of interface traps to the change of Fermi level ($df(E)/dE_{\mathrm{it}}$) [8], [9], [10], [11].

In this paper, we presented never-before-reported *SS* behaviors of FD-SOI p-MOSFETs at T = 4.5 K-50 K. Studied FD-SOI MOSFETs with L_G of 24 nm – 300 nm were fabricated on conventional and flipped wells using a commercial 22-nm SOI technology. Bulk MOSFETs fabricated using a commercial 28-nm technology were studied for comparison.

II. ELECTRICAL MEASUREMENTS AND SIMULATION

Temperature-dependent electrical characterizations were conducted in a Lakeshore CRX-4K probe station using a semiconductor device analyzer Agilent B1500A. Parameters of V_{th} (V_G at I_D = 1×10^{-6} A/μm) and SS = $(\partial(\log I_D)/\partial V_G)^{-1}$) were extracted from measured transfer characteristics.

A generic 2D TCAD device simulator, Silvaco Atlas, was used to calculate energy band diagram and carrier transport of studied FD-SOI MOSFETs at T = 50 K–300 K. The device schematics for simulation is shown in Fig. 1. Temperature-dependent bandgap energy narrowing, intrinsic carrier concentration, incomplete ionization of dopants, Shockley-Read-Hall recombination, Auger recombination,

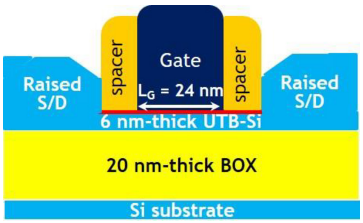

FIGURE 1. Schematics of studied FD-SOI MOSFETs in this work.

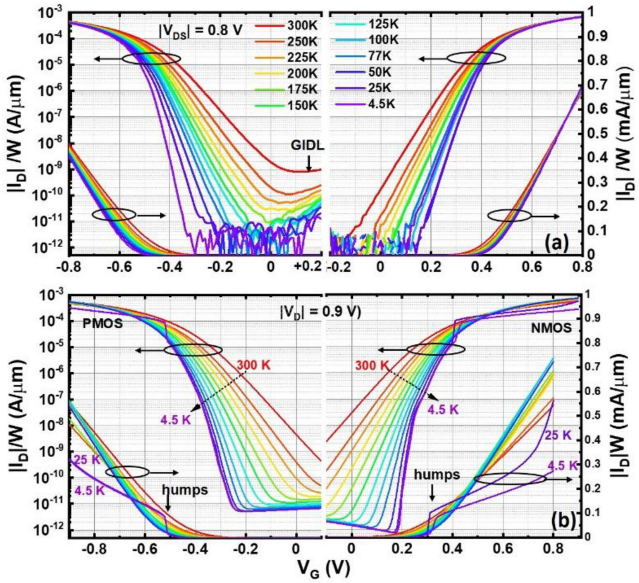

FIGURE 2. Transfer characteristics of (a) 24 nm FD-SOI and (b) 28 nm bulk MOSFETs biased at $|V_D|$ = 0.8 V and 0.9 V, respectively, and measured at T = 4.5 K–300 K.

band-to-band tunneling, and thermionic emission were self-consistently incorporated in the simulations to account for carrier transport.

III. RESULTS

A. SUBSTRATE EFFECT

Figure 2(a) and (b) show transfer characteristics of FD-SOI and bulk MOSFETs, respectively, measured at T = 4.5 K–300 K. It is clearly seen that lowering temperature leads to V_{th} increase in combination with SS reduction for both-type MOSFETs. At $T \leq 25$ K, current humps appear in bulk FETs but are invisible in FD-SOI MOSFETs. Gate-induced drain leakage (GIDL) appears in FD-SOI p-FETs biased at $V_G > 0$ and is suppressed by lowering temperature, whereas FD-SOI n-FETs show invisible GIDL even at room temperature.

Figure 3 compares temperature-dependent SS versus I_D for FD-SOI n- and p-FETs with W_G/L_G = 170 nm/24 nm. At T = 300 K, the SS-I_D curve of p-FETs (SS_{min} = 90 mV/dec in Fig. 2(b)) lands far above that of their counterpart n-FETs (SS_{min} = 65 mV/dec in Fig. 2(a)). The disparity of $SS(T)$ curves between FD-SOI p-FETs and n-FETs quickly reduces with lowering temperature, and the cross-over occurs at $T \approx$ 50 K below which SS-I_D curves of p-FETs reversely stand underneath. This is because n-FETs start to have SS saturation at T = 100 K–150 K, whereas SS of p-FETs continuously decreases with temperature. At T = 4.5 K, SS values of 21–25 mV/dec for FD-SOI p-FETs are even significantly smaller than that of 34–38 mV/dec for FD-SOI n-FETs.

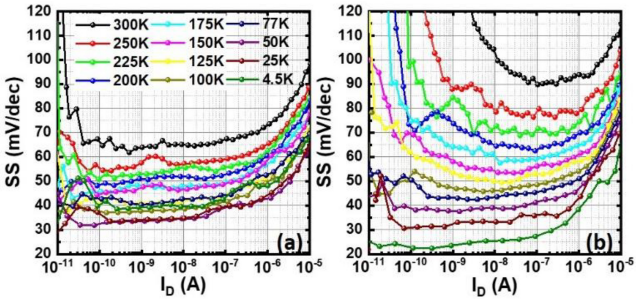

FIGURE 3. Experimental SS-I_D for FD-SOI (a) n- and (b) p-MOSFETs with W_G/L_G = 170 nm/24 nm measured at T = 4.5 K– 300 K.

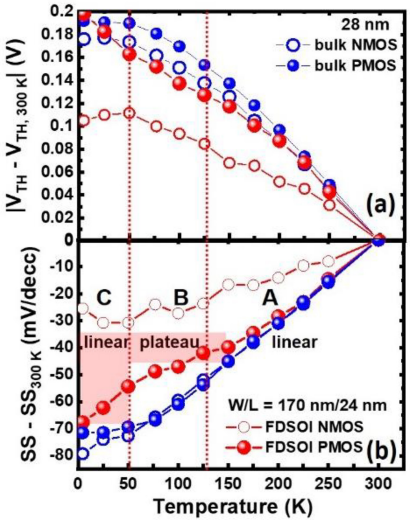

FIGURE 4. Temperature-dependent (a) ΔV_{th} and (b) ΔSS of FD-SOI n-/p-MOSFETs with W_G/L_G = 170 nm/24 nm and 28 nm bulk n-/p-MOSFETs measured at T = 4.5–300 K.

Figure 4(a) summarizes V_{th} shift with respect to room temperature ($\Delta V_{th}(T)$) = $|V_{th}(T)$ - V_{th}(300 K)) of FD-SOI and bulk MOSFETs caused by cooling from 300 K to 4.5 K. It is important to note that p-FETs appear to have stronger temperature effects on V_{th} shift than their counterpart n-FETs, in particular, built on FD-SOI substrates. Compared to the values of ΔV_{th}(4.5 K) = 0.175 V/0.191 V for bulk n-/p-FETs, cooling-induced V_{th} shift (0.11 V) is suppressed in FD-SOI n-FETs. V_{th}-shift saturates at $T \leq$ 50 K for bulk n-/p-FETs and FD-SOI n-FETs due to dopant incomplete ionization and field assisted ionization [1], [4], [12], whereas FD-SOI p-FETs appear to have a monotonic increase in V_{th} shift with decreasing temperature from 300 K to 4.5 K.

Figure 4(b) compares temperature-dependent SS span ($\Delta SS(T)$) = $|SS(T)$ - SS(300 K) at I_D = 10^{-7} A/μm) of FD-SOI and bulk MOSFETs. Cooling-induced

SS improvement ($\Delta SS(T = 4.5K)$) in FD-SOI n-/p-FETs (30 mV·dec^{-1}/68 mV·dec^{-1}) is smaller than that (80 mV·dec^{-1}/72 mV·dec^{-1}) of their counterpart bulk n-/p-FETs. This is because ultra-thin bodies (UTBs) in FD-SOI MOSFETs effectively suppresses bulk punch-through at room temperature. Cooling indeed provides another way to mitigate bulk punch through since the built-in potential of drain/body (DB) junction increases by Fermi-level ($E_{Fn,B} - E_{Fi} = k_BT\ln(N_D/n_i)$ or $E_{Fi} - E_{Fp,D} = k_BT\ln(N_A/n_i)$ approaching the band edges (E_C or E_V) with decreasing temperature.

Fig. 4(b) reveals that bulk n-/p-FETs and FD-SOI n-FETs exhibit typical two-temperature regimes for $SS(T)$ behaviors. That is, *SS* scales linearly with temperature and saturates to a constant value at $T \leq 50$ K and ≤ 125 K, respectively, for bulk n-/p-FETs and FD-SOI n-FETs. Remarkably, three temperature regimes appear for $SS(T)$ of FD-SOI p-FETs. At $T = 50$ K–125 K (denoted by regime **B**), the *SS* curve (denoted by the red line with solid-sphere symbol) of FD-SOI p-FETs clearly deviates the initial linear relationship with temperature ($SS(T) = n(T) \times \ln(10)(kT/q)$) at $T = 150$ K–300 K (regime **A**) and resembles a plateau-like behavior. A striking observation is that at $T = 4.5$ K – 50 K (regime **C**), the *SS* value of FD-SOI p-FETs actually decreases with temperature.

B. CHANNEL-LENGTH EFFECT

Figure 5 shows temperature-dependent *SS* behaviors with three temperature zones observed from $L_G = 100$ nm and 24 nm FD-SOI p-FETs fabricated on N-wells (namely regular-V_{th} (RVT) configuration). It is clearly seen that cooling-induced *SS* improvement is enhanced by downscaling L_G from 100 nm (green lines) to 24 nm (red lines) and by increasing drain bias from $V_D = -0.05$ V (hollow symbols) to –0.8 V (solid symbols).

Cassé et al. [13] have also reported similar temperature dependency of *SS* behaviors from 28 nm FD-SOI p-FETs with an equivalent gate-oxide thickness of 1.1 nm fabricated on p-wells (namely low-V_{th} (LVT) configuration). That is, cooling results in a linear decrease in *SS* at $T = 150$ K–300 K, followed by a *SS* plateau at $T = 77$ K–150 K in combination with a *SS* drop at $T = 4.5$ K–77 K, as seen from the blue line with solid symbol in Fig. 5. In contrast, *SS* curves of peripheral p-FETs (that are designed for peripheral circuitry) with $L_G = 150$ nm and 300 nm in LVT configuration show typical temperature dependency, i.e., *SS* decreases at $T = 100$ K–300 K and then saturates at $T < 100$ K. This is possibly ascribed to a thicker gate-oxide layer and higher doping concentration in the UTB-channels being generally used for peripheral MOSFETs.

IV. DISCUSSION

Our experimental observations from FD-SOI p-FETs reveal several distinctive temperature-dependency of subthreshold characteristics such as GIDL current, V_{th}, and *SS*, which differ from that of bulk MOSFETs and FD-SOI nFETs.

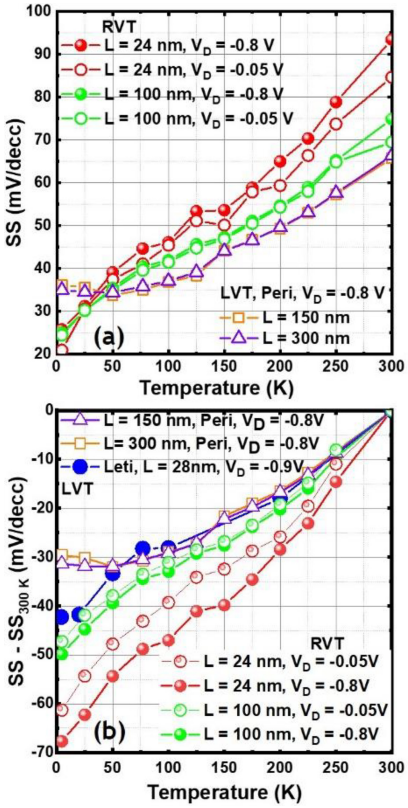

FIGURE 5. Temperature-dependent (a) SS and (b) ΔSS with respect to 300 K of FD-SOI P-FETs with $L_G = 24$ nm/100 nm in RVT configuration and $L_G = 150$nm/300 nm in LVT configuration measured at $T = 4.5$ –300 K and $V_D = -0.05$V/–0.8V. Reference [13] with 28 nm FD-SOI P-FETs in LVT configuration measured at $V_D = -0.9$V is also included for comparison.

The first important finding of notes is that FD-SOI n-FETs have higher T_C (~125 K) for *SS* saturation than bulk n-FETs ($T_C \sim 50$ K) as seen in Fig. 4(b). A higher T_C in FD-SOI FETs is attributable to a larger amount of interface traps at double interfaces of the top gate-oxide/UTB and of the UTB/buried-oxide layers [9], [14].

The second important finding of notes is that FD-SOI p-FETs have larger *SS* values at $T = 50$ K–300 K but smaller *SS* values at $T = 4.5$ K–25 K than their counterpart FD-SOI n-FETs (Fig. 3). Higher *SS* values at $T > 50$ K suggests higher interface trap density (D_{it}) at the n-type UTB-Si/gate oxide interface. Notably, the presence of high localized states (traps) at the n-UTB-Si/gate oxide interface within the gate/p$^+$-drain overlap region also activates trap-assisted tunneling (TAT) processes, contributing GIDL current at low *E*-field (V_G) [15], [16], [17]. Cooling reduces TAT-GIDL current due to a large reduction in intrinsic carrier concentration (n_i) at cryogenic temperatures since TAT-GIDL is proportional to n_i ($\mathbf{I}_{TAT\_GIDL} \propto n_i(T)$) [17]. This explains why the GIDL current in our studied FDSOI p-FETs is significantly reduced at cryogenic temperatures (Fig. 2(a)), in particular, at low V_G (~0 V). Similar temperature and electric-field dependences of GIDL current, involving band-to-band tunneling (BTBT) at high field (> 1 MV/cm)

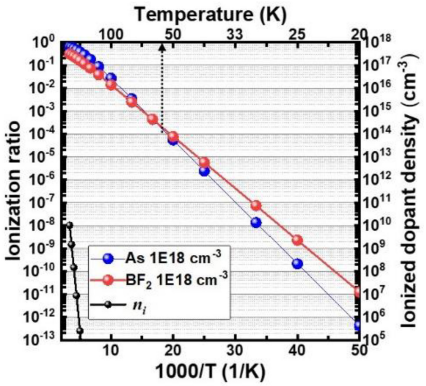

FIGURE 6. Temperature-dependent ionization ratio and carrier density of Arsenic and Boron with dopant concentrations of 10^{18} cm^{-3} in Si.

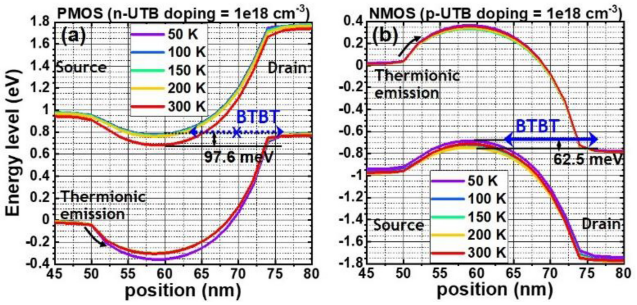

FIGURE 7. Energy band diagram along the channel-length direction of 24 nm FD-SOI (a) p- and (b) n-FETs simulated at $|V_D| = 0.8V$ at T = 50 K–300 K. The subthreshold current comprises components of thermionic emission across source/UTB junction and BTBT/TAT across drain/UTB junction.

and TAT at low field, have been reported in sub-20-nm FinFETs [17] and 22 nm FD-SOI MOSFETs at cryogenic temperatures [18].

Our experimental observation of smaller SS values of FD-SOI p-FETs at $T = 4.5$ K–25 K signifies enhanced incomplete ionization of donors in n-UTB-Si than that of acceptors in p-UTB-Si for FD-SOI n-FETs. It is a known fact that carrier concentration relies on dopant ionization that is highly dependent on dopant concentration [1], ionization energy, and temperature. Assuming the same dopant concentration of 10^{18} cm^{-3} in UTBs of p-FETs and n-FETs, temperature-dependent ionization ratios of arsenic and boron are calculated using ionization energies of $E_D = 53.76$ meV and $E_A = 45$ meV, respectively. Fig. 6 shows that at $T >$ 100 K, arsenic has a higher ionization ratio than boron by a factor of ~2 due to combined effects of effective density of states, degeneracy factor, and ionization energy. However, a larger E_D for arsenic results in a stronger decline in dopant ionization ratio at $T < 50$ K, which in turn leads to electron concentration contributed by arsenic ionization considerably lower than hole concentration arising from boron ionization.

The experimental observation (Fig. 4(a)) of a larger and even continuous V_{th} shift of p-FETs, instead of the V_{th} saturation in n-FETs, is a strong testament to enhanced incomplete ionization of donors in n-UTB-Si than acceptors in p-UTB-Si. Beckers et al. [1], [4], [12] and Dhao et al. [19] have reported a stronger temperature dependency of V_{th} shift in bulk and FD-SOI p-FETs with $L_G = 28$ nm^{-1} $\mu m/W_g = 80$ nm^{-1} μm and in bulk p-FETs with $L_G = 0.35$ μm^{-10} $\mu m/W_g = 10$ μm, respectively, as compared to their counterpart n-FETs. Their discovery shows that at cryogenic temperatures, V_{th} shift (ΔV_{th}) gets smaller and SS improvement ($\Delta SS(T)$) becomes enhanced for MOSFETs with shorter channel-lengths and narrower channel-widths. Dhao et al. [19] proposed that donors in the p-channel suffer stronger freeze-out than acceptors in the n-channel at cryogenic temperatures. Consequently, enhanced field-assisted ionization of trapped carriers is required for the p-channel formation at cryogenic temperatures, leading to a continuous V_{th} shift for pMOSFETs. Beckers et al. [12] further proposed a physical model using an effective gate-oxide capacitance to explain the non-saturating temperature behavior of the V_{th} in 28 nm bulk MOSFETs. Their modeling results suggest that a pMOS specific phenomenon in the gate stack (including strain, different gate-stack, a quantum-mechanical or band-structure-related effect of the holes) is responsible for the rising trend of threshold voltage at $T < 50$ K in pMOSFETs.

The third striking observation from FD-SOI p-FETs with $L_G \leq 100$ nm in both RVT and LVT configurations is that at $T = 4.5$ K – 50 K, $SS(T)$ linearly scales with temperature rather than saturates to a constant value. In general, subthreshold current comprises components of (1) thermionic emission across source/body junction (I_{th}), (2) DB BTBT ($I_{DB,BTBT}$), (3) DB TAT ($I_{DB,TAT}$), and (4) source-to-drain direct tunneling ($I_{SD,DT}$). In this work, $I_{SD,DT}$ contribution is neglectable since studied channel-lengths of 24 nm–100 nm are too long to enable source-to-drain direct tunneling [7]. Our experimental observation of a continuous drop in $SS(T)$ at $T < 50$ K suggests the predominance of thermal-assisted processes.

DB-BTBT process is essentially determined by the UTB potential energy and DB junction width, which are dependent on carrier concentration within the UTB, channel length, drain bias, and gate-oxide thickness. A considerable carrier freeze-out within n-UTBs of p-MOSFETs at $T < 50$ K reduces the subthreshold current and thus improves SS values significantly due to (1) a large reduction in E_C lowering (> 97.6 meV) of n-UTBs and (2) an enlargement in DB junction width with respect to that at $T = 300$ K, as shown in calculated energy band diagrams of Fig. 7(a). At $T \leq 50$ K, the minimum E_C of n-UTB is higher than E_V of p^+-Drain, deactivating DB-BTBT process. In contrast, a smaller barrier lowering in p-UTB of n-MOSFETs (Fig. 7(b)) arising from a higher ionization ratio of boron keeps DB-BTBT process active at $T \leq 50$ K, contributing $I_{DB,BTBT}$ and leading to SS saturation. In addition to DB-BTBT at large V_D, DB-TAT plays a pivotal role for reduced subthreshold current and thus the linear decrease in SS values at $T < 50$ K when FETs is biased at small V_D, as seen in Fig. 5.

V. CONCLUSION

We presented a cryogenic study of 22-nm FD-SOI MOSFETs and 28-nm bulk MOSFETs at T = 4.5 K – 300 K operation. Our first important observation is that in comparison to 28 nm planar CMOSFETs, cooling induced V_{TH} increase in combination with *SS* decrease are much suppressed in FD-SOI MOSFETs. Another important finding of notes is that larger SS values at $T = 50$ K–300 K but smaller *SS* values at $T = 4.5$ K–25 K are observed from FD-SOI p-FETs than their counterpart FD-SOI n-FETs. The most intriguing observation is that *SS* saturation of FD-SOI p-MOSFETs occurs only to the mid-cryogenic regime at $T = 50$ K–125 K, below which *SS* again linearly decreases with temperatures down to 4.5 K. These distinctive temperature-dependency of subthreshold swings in FD-SOI p-FETs are associated with hole BTBT and TAT across the drain-body junction due to enhanced freeze-out or incomplete ionization of donors at cryogenic temperatures.

ACKNOWLEDGMENT

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